JW5513

20V, 15A, High Efficiency Synchronous Step-up Regulator

Preliminary Specifications Subject to Change without Notice

DESCRIPTION

The JW5513 is a synchronous high-efficiency, step-up boost converter. The device adopts constant-off-time (COT) control topology. The integrated low $R_{DS(ON)}$ switches minimize the conduction loss.

The JW5513 supports the selection of pulse-skip mode (PFM), forced continuous conduction mode (PWM), and ultrasonic mode(USM) in light-load condition. The device features cycle by cycle peak current limit up to 15A. The low output voltage ripple, the small external inductor and the capacitor size are achieved at programmable pseudo-constant frequency.

JW5513 guarantees robustness with over voltage protection and over temperature protection.

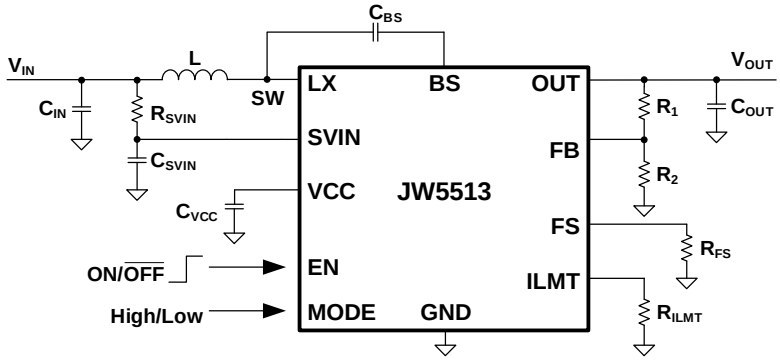
FEATURES

- Input Voltage Range: 2.6V to 20V
- Output Voltage Range: up to 20V
- Programmable Switch Peak Current: up to 15A
- Low $R_{DS(ON)}$ for FETs Integrated: Low-Side FET: 7.5mΩ, High-Side FET: 16mΩ
- Adjustable Switching Frequency: 300kHz to 2MHz
- PFM/USM/PWM Selectable Light Load Operation Mode
- Internal Loop Compensation
- Internal Soft-start Limit the Inrush Current
- Over Temperature Protection
- Over Voltage Protection
- RoHS Compliant and Halogen Free
- Compact Package: QFN3x3-20

APPLICATIONS

- High Power AP
- Bluetooth Speaker
- Power Banks
- E-cigarette

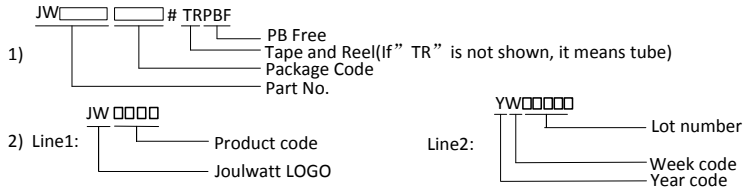
TYPICAL APPLICATION



ORDER INFORMATION

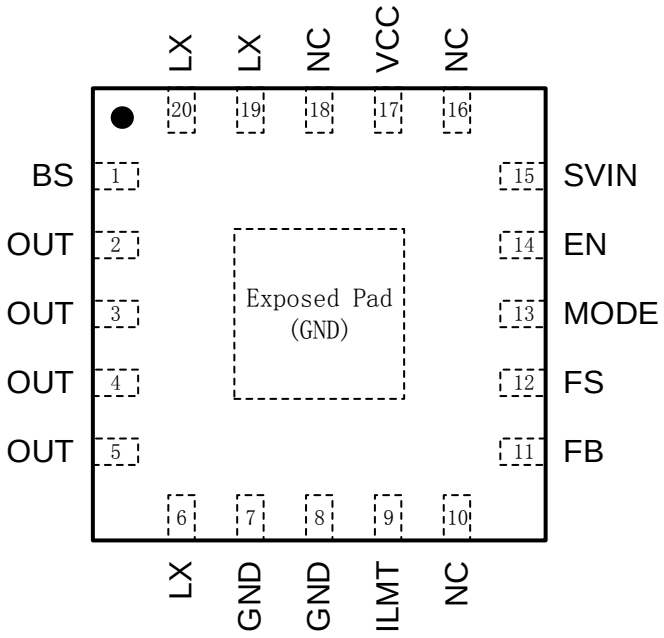
DEVICE[1)]	PACKAGE	TOP MARKING[2)]
JW5513QFNAV#TRPBF	QFN3x3-20	JW5513 YW□□□□□

Notes:



PIN CONFIGURATION

TOP VIEW



QFN3×3-20

ABSOLUTE MAXIMUM RATING[1)]

SVIN, LX, OUT, ILMT, FS, MODE, EN ..... -0.3V to 24V
FB, VCC ..... -0.3V to 4V
BS-LX ..... -0.3V to 4V
Dynamic LX Voltage in 10ns Duration ..... -3.5V to 27V
Junction Temperature Range[2)] ..... -40ºC to +150ºC
Power Dissipation, P_D @ (T_A = 25ºC) [3)] QFN3×3-20 ..... 3.1W
Lead Temperature (Soldering, 10 sec.) 260ºC

Storage Temperature Range ..... -65ºC to +150ºC

RECOMMENDED OPERATING CONDITIONS[4)]

SVIN ..... 2.6V to 20V
Junction Temperature Range …..... -40ºC to +125ºC
Ambient Temperature Range …..... -40ºC to +85ºC

THERMAL PERFORMANCE[5)]

	θ_{JA}	θ_{JC}
QFN3×3-20	32	4ºC/W

Note:

1) Exceeding these ratings may damage the device. These stress ratings do not imply function operation of the device at any other conditions beyond those indicated under RECOMMENDED OPERATIONF CONDITIONS

2) The JW5513 includes thermal protection that is intended to protect the device in overload conditions. Continuous operation over the specified absolute maximum operating junction temperature may damage the device.

3) The maximum allowable continuous power dissipation at any ambient temperature is calculated by PD (MAX) = $(T_J(MAX)-T_A)/\theta_{JA}$.

4) The device is not guaranteed to function outside of its operating conditions.

5) Measured in the natural convection at T_A = 25℃ on a four-layer JoulWatt Evaluation Board.

ELECTRICAL CHARACTERISTICS

VIN=5V, V_{OUT}=12V, I_{OUT}=100mA, T_A=25°C, unless otherwise specified.
Advance Information, not production data, subject to change without notice.

Item	Symbol	Condition	Min.	Typ.	Max.	Units
POWER SUPPLY						
VIN Under Voltage Lockout (UVLO) Threshold	V_{SVIN_UVLO}	V_{SVIN} rising	2.25	2.4	2.6	V
VIN UVLO Hysteresis	V_{SVIN_HYS}			400		mV
Quiescent Current	I_Q	V_{FB}=1.1V		70	85	uA
Shutdown Current	I_{SHDN}	EN=0		0.75	3.5	uA
POWER SWITCHES						
Low Side N-FET(LS-FET) R_{ON}	$R_{DS(ON)\_L}$			7.5		mΩ
High Side N-FET(HS-FET) R_{ON}	$R_{DS(ON)\_H}$			16		mΩ
VOLTAGE REFRENCE						
Feedback Reference Voltage	V_{REF}	T_A=25°C	0.99	1	1.01	V
Feedback Reference Voltage	V_{REF}	T_A=-40°C~85°C	0.985	1	1.015	V
FB Leakage Current	I_{FB}	V_{FB}=3.3V		0	50	nA
CURRENT LIMIT						
LS-FET Current Limit	I_{LMT}	R_{ILMT}=100kΩ	13	15	17	A
LS-FET Current Limit Program Range	I_{LMT_RNG}		4		15	A
ILMT Reference Voltage	V_{ILMT}			0.6		V
ENABLE						
EN Input Voltage High	V_{EN_H}		1.2			V
EN Input Voltage Low	V_{EN_L}				0.4	V
MODE SELECTION						
PFM MODE tri-state region	V_{MODE_PFM}				0.4	V
USM MODE tri-state region	V_{MODE_USM}		0.7		0.95	V
PWM MODE tri-state region	V_{MODE_PWM}		1.2		VIN	V
USM MODE switching frequency	F_{SW_USM}		24	32		kHz
SWITCHING CHARACTERISTICS						
Switching Frequency Program Range	f_{SW_RNG}		300		2000	kHz
Switching Frequency Accuracy	f_{SW}	R_{FS}=360kΩ	400	500	600	kHz
Minimum ON Time(6)	T_{ON_MIN}			120		ns
Minimum OFF Time(6)	T_{OFF_MIN}			110		ns
SOFT START						
Soft Start Time	T_{SS}			3		ms

PROTECTION						
Output OVP threshold	V_{OUT_OVP}		21.5	22.3	23.8	V
Output OVP hysteresis	$V_{OUT\_OVP\_HYS}$			0.8		V
Feedback Overvoltage with Respect to Reference Voltage	V_{FB_OVP}	V_{FB} rising	115	120	125	%
Feedback Overvoltage with Respect to Reference Voltage Hysteresis	$V_{FB\_OVP\_HYS}$			10		%
Thermal shutdown temperature(6)	T_{SD}			150		ºC
Thermal shutdown hysteresis(6)	T_{HYS}			15		ºC

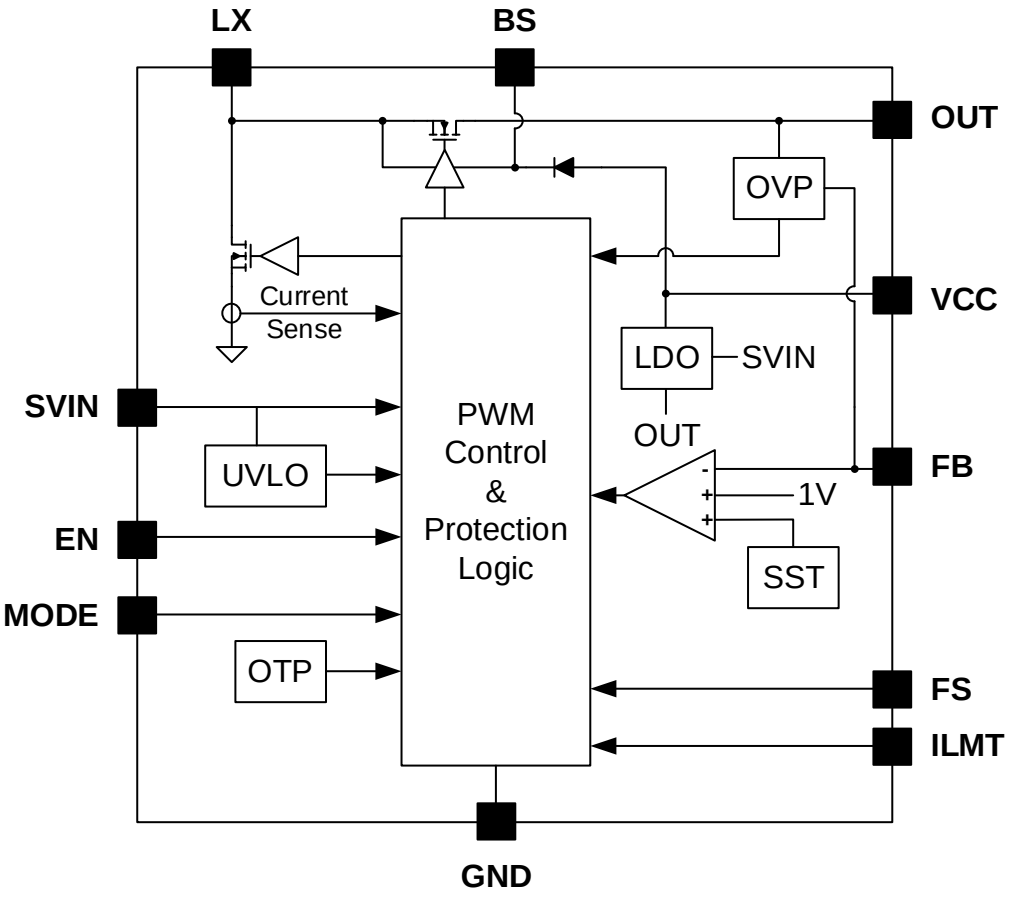
Note:

6) Guaranteed by design.

PIN DESCRIPTION

Pin No.	Name	Description
1	BS	Boot-strap pin. Supply rectifier FET's gate driver. Connect a 0.1μF ceramic capacitor between BS and LX.
2,3,4,5	OUT	The Boost converter output pin.
6,19,20	LX	Inductor node. Connect an inductor from power input to the LX pin.
7,8,EP	GND	Ground pin of IC.
9	ILMT	Switch peak current limit setting. Connect a resistor from this pin to GND.
10,16,18	NC	Not connected and must float.
11	FB	Feedback pin. Connected to the center of the resistor voltage divider to program the output voltage: $V_{OUT}=1V\times(R_1/R_2+1)$
12	FS	Switching frequency setting pin. Connect a resistor from this pin to ground to program the switching frequency.
13	MODE	MODE selection. If MODE is floating or high (>1.2V), the device works in forced continuous conduction mode (PWM). If MODE is low (<0.4V), the device works in pulse frequency modulation (PFM). If MODE is between 0.65V and 0.95V, the device works in ultrasonic mode (USM).
14	EN	Enable control. Pull high to turn on the IC. Do not leave it floating.
15	SVIN	IC power supply input pin. Decouple this pin to the GND pin with a 1μF ceramic capacitor at least.
17	VCC	Output of the internal LDO regulator. Decouple this pin to the GND pin with a 1μF ceramic capacitor at least.

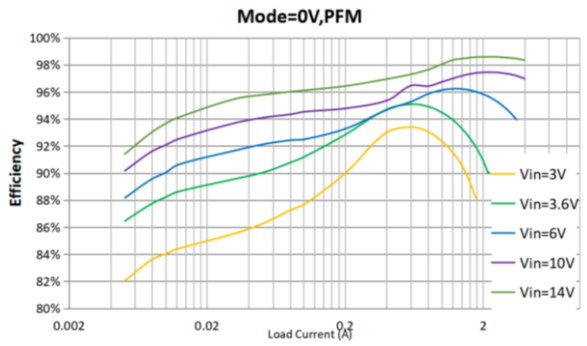
BLOCK DIAGRAM



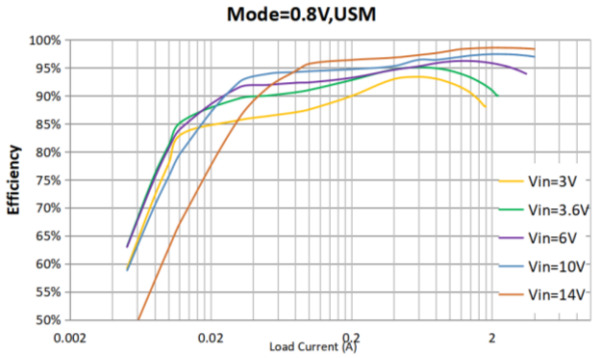
TPICAL PERFORMANCE CHARACTERISTICS

V_{IN}=2.7V~14V, V_O=16V, L=2.2uH, C_O=5x22uF+100nF, F_{SW}=500kHZ, T_A = +25°C, unless otherwise noted

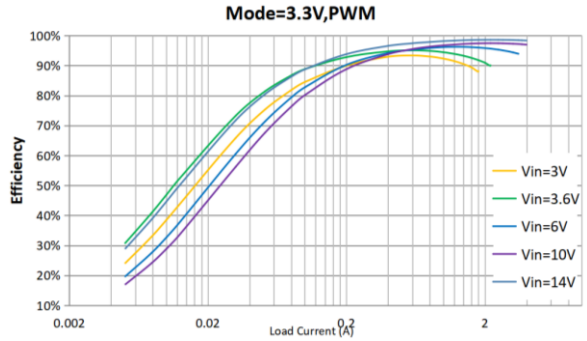
Efficiency vs. Load Current



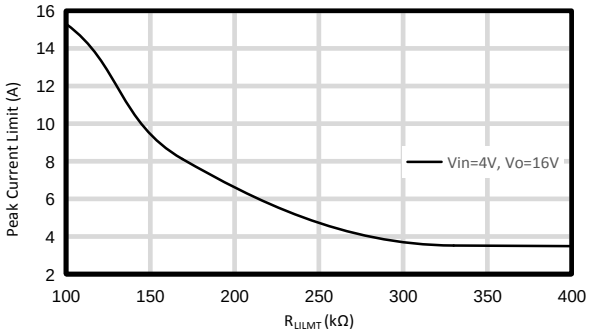
Efficiency vs. Load Current



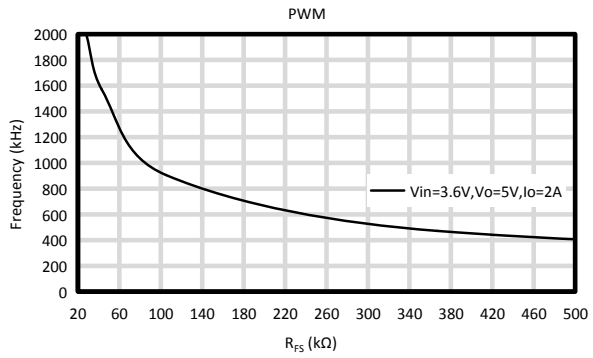
Efficiency vs. Load Current



Switching Current Limit vs. R_{ILMT}

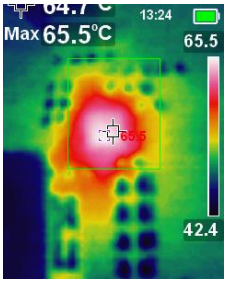


Switching Frequency vs. R_{FS}



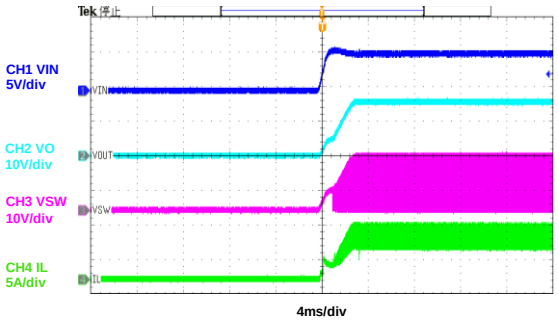
Temperature Rising

V_{IN}=7.2V, V_O=16V, I_O=3A



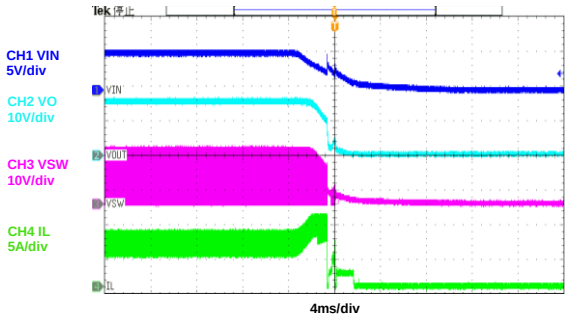
VIN Power On

V_{IN}=6V, V_O=16V, I_O=2A



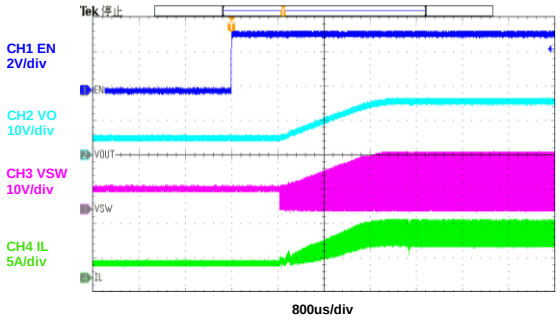
VIN Power off

V_{IN}=6V, V_O=16V, I_O=2A



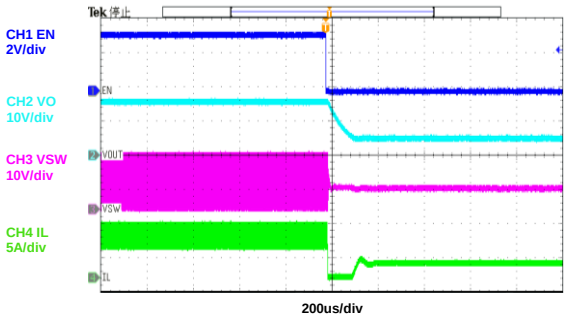
EN Power On

V_{IN}=6V, V_O=16V, I_O=2A



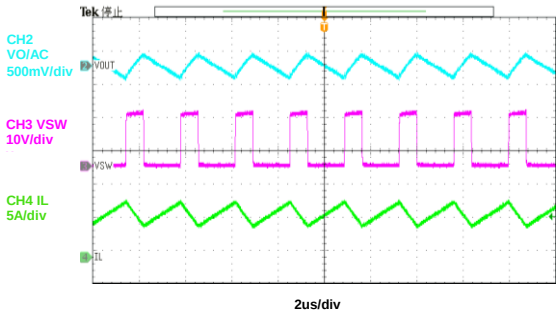
EN Power off

V_{IN}=6V, V_O=16V, I_O=2A



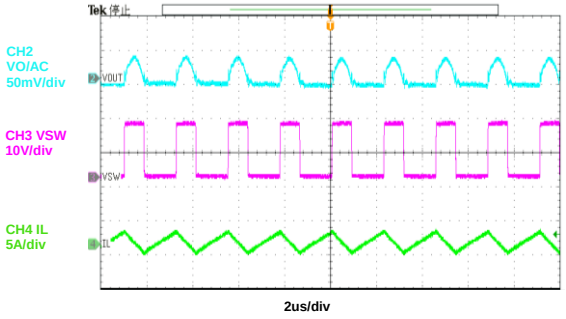
Steady State

V_{IN}=6V, V_O=16V, I_O=2A



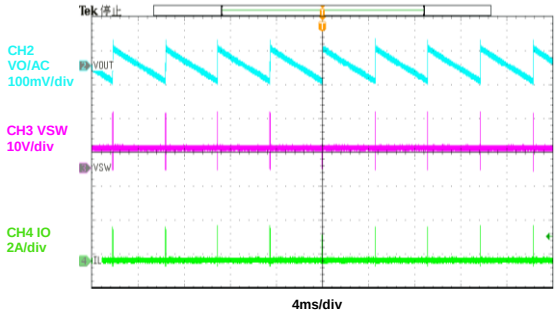
Steady State (PWM)

V_{IN}=6V, V_O=16V, I_O=0A



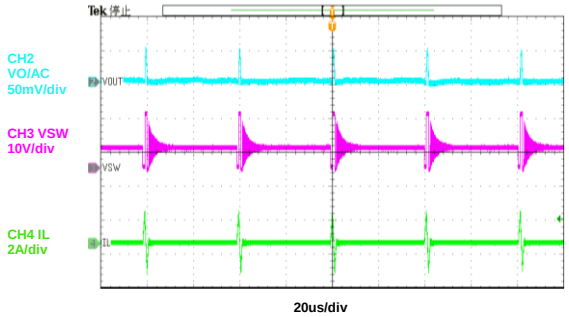
Steady State (PFM)

V_{IN}=6V, V_O=16V, I_O=0A



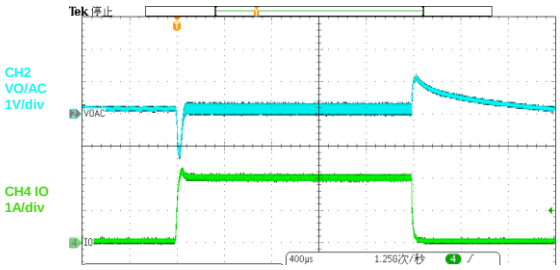
Steady State (USM)

V_{IN}=6V, V_O=16V, I_O=0A



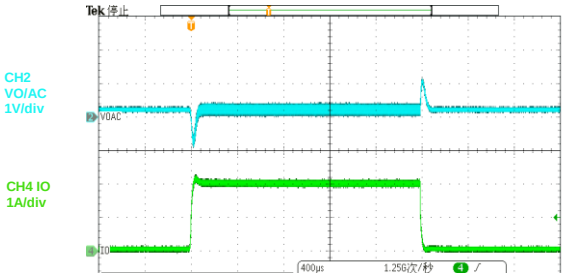
Load Transient (PFM)

V_{IN}=6V, V_O=16V,I_O=0A ⇔ 2A, I_{RAMP}=200mA/us



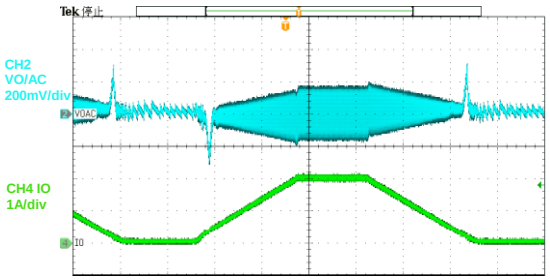
Load Transient (PWM)

V_{IN}=6V, V_O=16V,I_O=0A ⇔ 2A, I_{RAMP}=200mA/us



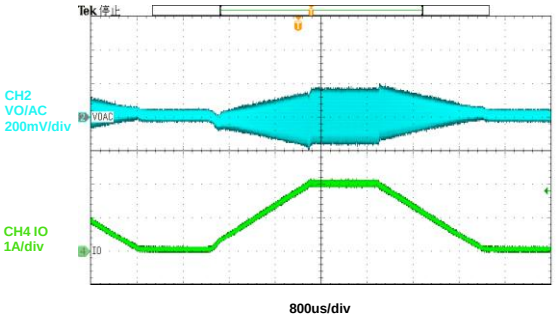
Load Sweep (PFM)

V_{IN}=6V, V_O=16V,I_O=0A ⇔ 2A, I_{RAMP}=1mA/us



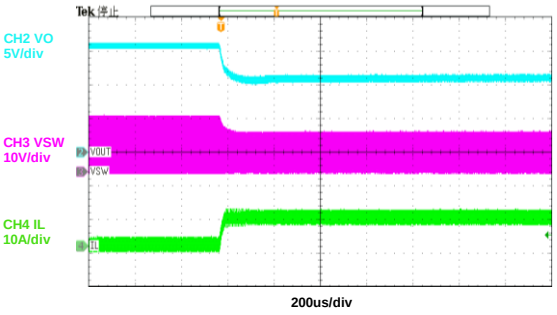
Load Sweep (PWM)

V_{IN}=6V, V_O=16V,I_O=0A ⇔ 2A, I_{RAMP}=1mA/us



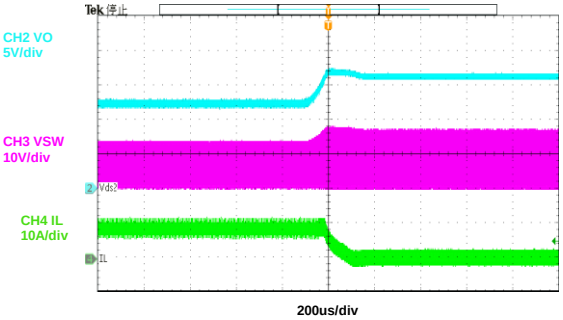
Over-Current Enter

I_O=0A→4A



Over-Current Recovery

I_O=4A→0A



FUNCTIONAL DESCRIPTION

The JW5513 is a synchronous, high-efficiency, step-up boost converter. It is designed to operate from an wide input voltage range between 2.6V and 20V with up to 15A peak switch current limit.

The device adopts adaptive constant off time and current mode control. The pseudo-constant switching frequency in CCM can be programmed. PFM/USM/PWM light load operation is selected by the MODE pin.

The JW5513 guarantees robustness with over voltage protection and over temperature protection.

Start-Up

When EN is high logic, the JW5513 can start up from a voltage as low as 2.4V typical. If the input voltage rises above $V_{SVIN,UVLO}$, the chip begins to operate and starts in PFM mode. The internal soft-start time can limit the inrush current during start-up. When the input voltage drops below 2.0V typical, the chip stops working.

Device Enable

The JW5513 starts operation when EN pin is pulled high and starts up with a soft-start process. Pulling EN pin low can force the device into shutdown mode. In shutdown mode, the chip stops switching and all the internal control circuit is off.

Output Voltage

The output voltage is set by an external feedback resistive divider. The feedback signal is compared with internal precision 1V voltage reference by an error amplifier. The output voltage can be given by the equation:

$$V_o(V) = \frac{1V \times (R_1 + R_2)}{R_2}$$

Where R_1 and R_2 are defined in the typical application figure.

Adjustable Switch Peak Current Limit

To prevent the device from being damaged by a large inductor peak current, a cycle-by-cycle current limit is adopted in JW5513. The low side switch is turned off immediately, as soon as the switch current touches the setting limit, which is programmed by a resistor from the ILIM pin to ground. The peak current limit can be given by the formula below:

$$I_{LMT}(A) = \frac{1700}{R_{ILMT}(k\Omega)} - 2$$

where I_{LMT} is the switch peak current limit, R_{ILMT} is the resistor between ILMT pin and ground.

Adjustable Switching Frequency

The switching frequency of the JW5513 in CCM can be programmed by adjusting the external resistor R_{FS} connected between FS pin and ground.

$$F_{SW}(kHz) = \frac{1}{\frac{1}{\frac{73565}{R_{FS}(k\Omega)} + 300} + 0.0001}$$

Light Load Operation Mode Selection

During light load operation, PFM, USM or PWM can be selected by the MODE pin.

When the MODE pin is pulled logic high (V_{MODE}>1.2V), the JW5513 operates in PWM(FCCM). In this condition, the off time is determined by the internal circuit to achieve the programmable frequency based on the V_{IN}/V_{OUT} ratio. When the load decreases, the average input current drops, and the inductor current from V_{IN} to

V_{OUT} may become negative during the off time (Low side FET is off, and high side FET is on). This forces the inductor current to work in continuous conduction mode (PWM) with a fixed frequency, producing a lower V_{OUT} ripple than in PFM.

When the MODE pin is pulled logic low (V_{MODE}<0.4V), the device operates in PFM. PFM is engaged to maintain high efficiency at light load when Mode pin is pulled low. In PFM mode, switching frequency is continuously controlled in proportion to the load current. Switch frequency decreases when load current drops to increase power efficiency at light load by reducing switching loss and minimizing the circuit power dissipation.

To prevent audible noise with a switching frequency lower than 20kHz in PFM, the JW5513 implements ultrasonic mode (USM) by setting MODE in the USM range (0.65V < V_{MODE} < 0.95V). In USM, the inductor current works in DCM, and the frequency stretches as if in PFM when the load decreases to a moderate level. The JW5513 continues decreasing the switching frequency if the load is still decreasing. Once the JW5513 detects that the switching cycle lasts for 31μs, it forces the LS-FET on.This limits the frequency, avoiding audible frequency in a light-load or no-load condition.

USM has more power loss than PFM if the frequency is clamped at the typical 32kHz, but USM does not introduce audible noise caused by the group pulse in PFM and has the higher efficiency than in PWM.

Protection

Over Voltage Protection

If output voltage is higher than V_{OUT_OVP} (Typ. 22.3V) or V_{FB} exceed 1.2V typical, the device stops switching immediately. Until the output voltage drops below 21.5V typical and V_{FB} drops below 1.1V typical, the device resumes switching automatically.

Over Temperature Protection

When the junction temperature of the device rises above T_{SD}, the device is forced into shut down mode. When the temperature drops by T_{HYS}, the device can be resumed with soft start.

APPLICATION INFORMATION

The JW5513 is designed for outputting voltage up to 20V with 15A switching current capability to deliver more than 40W power. The JW5513 operates at a quasi-constant frequency pulse-width modulation (PWM) in moderate to heavy load condition. In light load condition, the converter can either operate in the PFM mode or in the forced PWM mode according to the mode selection. The PFM mode brings high efficiency over entire load range, but the PWM mode can avoid the acoustic noise as the switching frequency is fixed. The converter uses the adaptive constant off-time peak current control scheme, which provides excellent transient line and load response with minimal output capacitance. The internal loop compensation and soft-start time minimize the external component count. It also supports adjustable switching frequency ranging from 300kHz to 2MHz for different inductor and output capacitor combination.

Typical Application Circuit

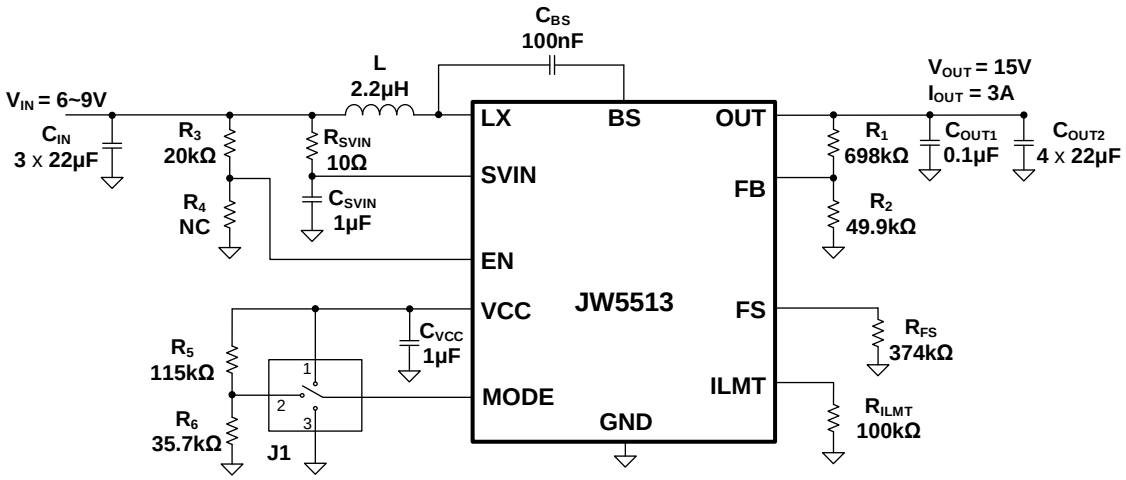


Figure 1: Typical Application Circuit with 15A Peak Current Limit

Design Requirements

Table 1. Design Parameters

DESIGN PARAMENTERS	EXAMPLES VALUES
Input voltage range	6.0V ~ 9.0V
Output voltage	15V
Output current	3A
Operation switching frequency	500kHz
Operation mode at light load	PFM/USM/PWM

Setting the Output Voltage

The external resistor divider is used to set the output voltage. Typically, choose R_1 to be between 300 - 800kΩ. Then calculate R_2 with the equation listed below:

$$R_2(k\Omega) = \frac{V_{REF}}{V_{OUT} - V_{REF}} \times R_1(k\Omega)$$

Where V_{REF} is 1V, R_1 is the top feedback resistor, an R_2 is the bottom feedback resistor.

Selecting the Input Capacitor

The input capacitor (C_{IN}) is used to maintain the DC input voltage. Low ESR ceramic capacitors are recommended. The input voltage ripple can be estimated with the following equation:

$$\Delta V_{IN}(V) = \frac{V_{IN}}{8 \cdot f_S^2 \cdot L \cdot C_{IN}} \times (1 - \frac{V_{IN}}{V_{OUT}})$$

Where f_S is the switching frequency, and L is the inductor value.

The SVIN capacitor must be close to the SVIN and GND pins to minimize the potential noise problem. In this case, a RC filter circuit (R_{SVIN}=10Ω,C_{SVIN}=1μF) is recommended.

Selecting the Output Capacitor

The output current of the boost converter is discontinuous and therefore requires an output capacitor (C_{OUT}) to supply AC current to the load. For the best performance, low ESR ceramic capacitors are recommended. The output voltage ripple can be estimated with the equation listed below:

$$\Delta V_{OUT}(V) = \frac{V_{OUT}}{f_S \cdot R_L \cdot C_{OUT}} \times (1 - \frac{V_{IN}}{V_{OUT}})$$

Where R_L is the value of the load resistor. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients.

Selecting the Inductor

An inductor is required to transfer the energy between the input source and the output capacitors. An inductor with a larger value results in less ripple current and a lower peak inductor current, reducing stress on the power MOSFET. However, the larger value inductor has a larger physical size, a higher series resistance, and a lower saturation current. For the smaller value inductor, larger current ripple generates higher DCR and ESR conduction losses and higher core loss. Usually, a data sheet of an inductor does not provide the ESR and core loss information. If needed, consult the inductor vendor for detailed information.

For most designs, the inductance value can be calculated with the following equation:

$$L = \frac{V_{IN}(V_{OUT} - V_{IN})}{f_S \cdot V_{OUT} \cdot \Delta I_L}$$

Where ΔI_L is the inductor ripple current. Choose the inductor ripple current to be approximately 20% ~ 50% of the maximum inductor peak current. Ensure that the inductor does not saturate under the worst-case condition. The inductor should have a low series resistance (DCR<10mΩ) to reduce the resistive power loss. The following table lists recommended inductors for this example application.

Table 2. Recommended Inductors for the example application

PART NUMBER	L (μH)	DCR MAX (mΩ)	SATURATION CURRENT (A)	SIZE MAX (L x W x H: mm)	VENDOR
7447707022	2.2	6.8	20.5	12.5 x 12.5 x 8.0	Wurth
SPM10065VT-1R5M-D	1.5	3.41	34.4	10.9 x 10.4 x 6.5	TDK
CMLE105T-2R2MS-99	2.2	4.5	26	10.3 x 11.5 x 5.0	Cyntec

For other different output powers, we recommend different inductor, input and output capacitors as below chart shows (it also shows the detail descriptions of the capacitors below the recommended value):

Table 3. Recommended L, C_{IN}, C_{OUT} for the different output power rating application

Input Voltage (V_{IN})	Output Power (V_{OUT}/I_{OUT})	Input Capacitor (C_{IN})	Output Capacitor (C_{OUT})	Inductor (L)
3.0V~8.4V	9V/3A	Ceramic: 2 x 22μF	Ceramic: 0.1μF+3 x 22μF	1.5μH
6.0V~9V	12V/3A	Ceramic: 2 x 22μF	Ceramic: 0.1μF+4 x 22μF	1.5μH
6.0V~14V	15V/3A	Ceramic: 3 x 22μF	Ceramic: 0.1μF+4 x 22μF	2.2μH
8V~17V	20V/3A	Ceramic: 3 x 22μF	Ceramic: 0.1μF+5 x 22μF	2.2μH

Switching Peak Current Limit Setting

The ILIM resistor (R_{ILMT}) is used to set the inductor switching peak current limit. Calculate R_{ILMT} with the following equation:

$$R_{ILMT}(k\Omega) = \frac{1700}{I_{LMT}(A) + 2}$$

For example, if the required peak current limit is 15A, then R_{ILMT} is 100kΩ.

Switching Frequency Setting

The switching frequency of the JW5513 in CCM can be programmed by adjusting the external resistor R_{FS} connected between FS pin and GND.

$$F_{SW}(kHz) = \frac{1}{\frac{1}{\frac{73565}{R_{FS}(k\Omega)} + 300} + 0.0001}$$

For example, if the required switching frequency is 500kHz, then R_{FS} is 374kΩ.

VCC Capacitor Selection

The JW5513 integrates the VCC power at about 3.4V, which powers the internal MOSFET gate driver and internal control circuit, typically. One ceramic bypass capacitor (C_{VCC}) 1μF or higher is necessary for the internal regulator. Do not connect the external load to the VCC power.

BST Capacitor Selection

The JW5513 uses one bootstrap circuit to power the output N-channel MOSFET. One external bootstrap capacitor (C_{BS}) for the charge pump power. A 0.1μF ceramic capacitor between BS and LX is recommended.

MODE Selection

The JW5513 can work in forced continuous conduction mode (PWM), pulse-skip mode (PFM), or ultrasonic mode (USM) based on the MODE setting. Pull MODE to VCC directly for PWM; pull MODE to GND for PFM; pull the MODE voltage to 0.65 - 0.95V to make the JW5513 work in USM. Without appropriate voltage for the USM threshold, a resistor divider

from VCC to GND can be used (see the following figure).

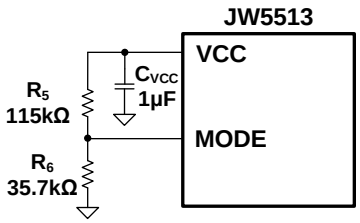


Figure 2: Operation Mode Setting

The typical VCC voltage range is 3.0V to 3.4V. Set R_5 to 115kΩ and R_6 to 35.7kΩ to achieve a 710 - 805mV voltage on MODE.

PCB Layout Guidelines

Efficient PCB layout is critical for high-frequency switching power supplies. A poor layout can result in reduced performance, excessive EMI, resistive loss, and system instability. Use a 4-layer PCB for high-power applications. For best results, refer to the following figure and follow the guidelines below.

1. Place the output capacitor (C_{OUT2}) as close to OUT and GND as possible, place a 0.1uF capacitor (C_{OUT1}) close to the IC to reduce the PCB parasitical inductance.
2. NC pin must be floating.
3. Keep the connection of OUT and GND to the output capacitor short and wide with copper.
4. Place this copper, the IC, and C_{OUT} on the same layer. Consider flooding empty areas with GND and place a PCB middle layer as GND plane to minimize inter-plane coupling.
5. Place the FB divider R_1 and R_2 as close to FB as possible.
6. Keep the FB trace far away from noise source, such as the LX node (switching node).
7. Place the current limit setting net (R_{ILMT}) close to ILMT pin.
8. Connect the VCC capacitor to GND with a short loop.
9. Keep the input loop (C_{IN},L,LX pin and GND) as small as possible.
10. Place enough GND vias close to the JW5513 for good thermal dissipation.

Layout Example

The PCB middle layer-1 is a large ground plane connected to the GND on top layer by vias. The signals route on the middle layer-2 by vias. The layout example shows as the follow figures.

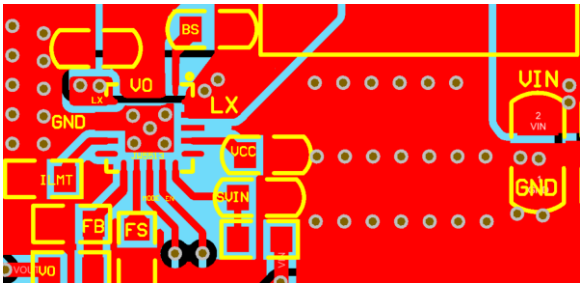
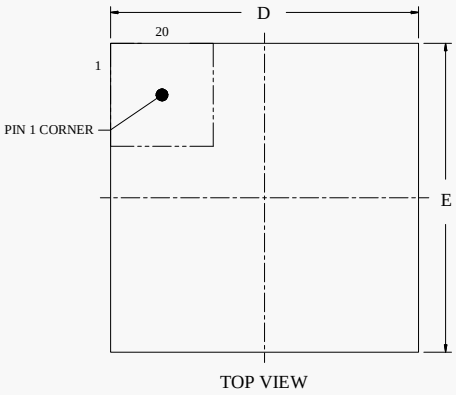


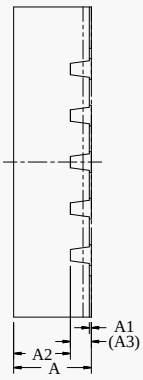
Figure 3: Layout Recommendation

PACKAGE OUTLINE

QFN3x3-20 UNIT: mm

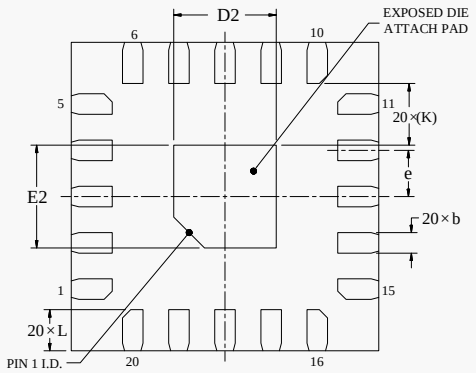


TOP VIEW

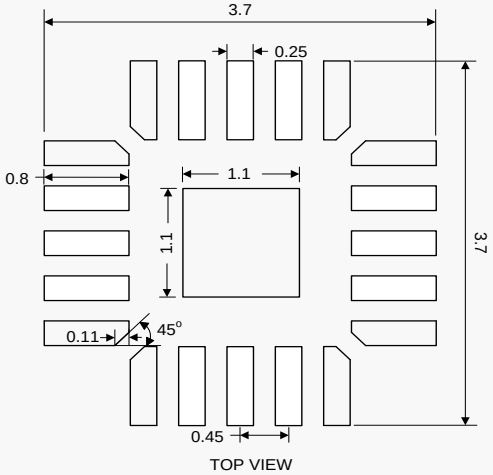


SIDE VIEW

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A2	—	0.55	—
A3		0.203 REF	
b	0.15	0.20	0.25
D	2.90	3.00	3.10
E	2.90	3.00	3.10
e		0.45 BSC	
D2	0.90	1.00	1.10
E2	0.90	1.00	1.10
L	0.30	0.40	0.50
K		0.60 REF	



BOTTOM VIEW

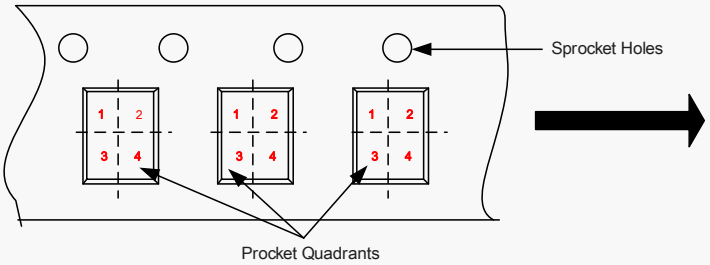


TOP VIEW

Recommended PCB layout

(Reference only)

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPAE



Package Type	Pin1 Quadrant
QFN3x3-20	1

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