JW1571

Offline Boost PFC CV Controller

Preliminary Specifications Subject to Change without Notice

DESCRIPTION

The JW®1571 is a constant voltage controller with high voltage accuracy which applies to single stage boost power factor correction (PFC) applications. Constant on time control strategy ensures high power factor, and the input voltage detection circuit is not needed, which simplifies the system design and saves the loss.

Critical conduction mode operation reduces the switching losses, improves the EMI performance and largely increases the efficiency.

JW1571 has multi-protection functions which largely enhance the safety and reliability of the system, including VCC UVLO, CS over voltage protection, FB over voltage protection and over temperature protection.

The JW1571 is available in SOP8 package.

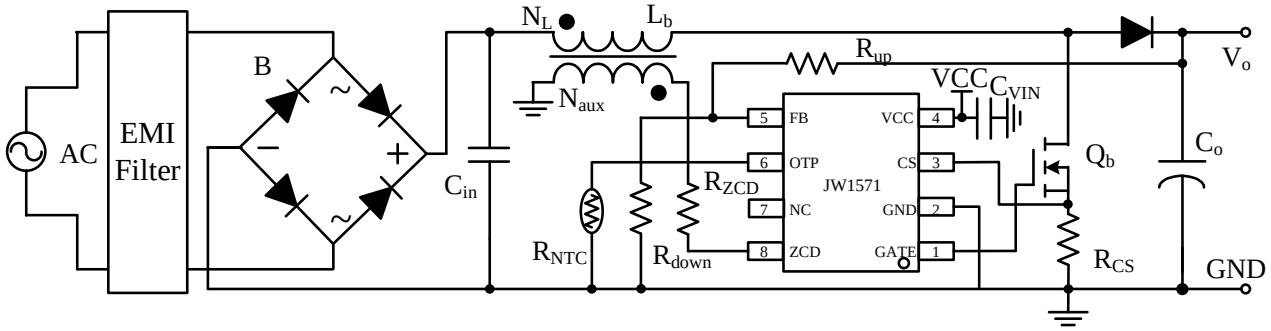
FEATURES

- Low Quiescent Current
- +0.6A/-1.4A Peak Gate Drive Current
- High Power Factor and Low THD
- Critical Conduction Mode
- High Reference Voltage Accuracy
- High Efficiency over Wide Operating Range
- Reduce Frequency at Light Load
- Open Feedback Protection
- Disable Function
- Pulse by Pulse Current Limit by CS Voltage
- External Over Temperature Protection
- 2nd OVP
- SOP8 Package

APPLICATIONS

- SMPS
- AC-DC Adapter
- Flat TV

TYPICAL APPLICATION

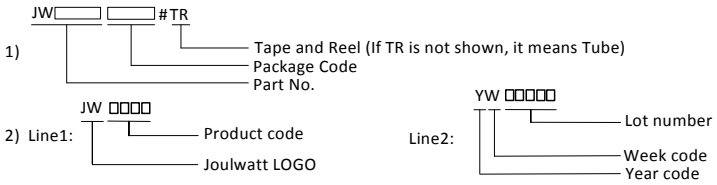


JW1571 PFC Application

ORDER INFORMATION

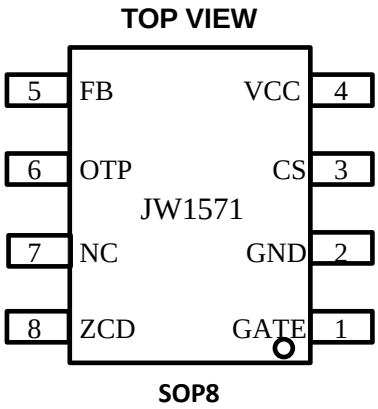
DEVICE[1)]	PACKAGE	TOP MARKING[2)]	ENVIRONMENTAL3)
JW1571SOPB#TR	SOP8	JW1571 YW□□□□□	Green

Notes:



3) All Joulwatt products are packaged with Pb-free and Halogen-free materials and compliant to RoHS standards.

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATING[1)]

VCC..... -0.3 to 45V
ZCD..... -0.6 to 45V
CS, OTP, FB.....-0.3 to 5V, 5 to 5.5V<10us
GATE.....-0.3 to 13V
Junction Temperature[2)]..... 150ºC
Lead Temperature..... 260ºC
Storage Temperature..... -65ºC to +150ºC
ESD Susceptibility (Human Body Model).....2kV

RECOMMENDED OPERATING CONDITIONS

VCC..... 12 to 40V

Operating Junction Temperature (T_J) [3]…..... -40ºC to 125ºC

THERMAL RESISTANCE[4)]

	θ_{JA}	θ_{JC}
SOP8	120	60ºC/W

Note：

1) Exceeding these ratings may damage the device. These stress ratings do not imply function operation of the device at any other conditions beyond those indicated under RECOMMENDED OPERATING CONDITIONS.

2) The JW1571 includes thermal protection that is intended to protect the device in overload conditions. Continuous operation over the specified absolute maximum operating junction temperature may damage the device.

3) The device is not guaranteed to function outside of its operating conditions.

4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

T_A=25℃, *unless otherwise noted*

Item	Symbol	Condition	Min.	Typ.	Max.	Units
Supply Voltage Management						
VCC Start-up Voltage	V_{CC_ST}			13		V
VCC Under Voltage Lockout	V_{CC_UVLO}			8.2		V
VCC Operation Current	I_{VCC_OP}	f_{sw}=25kHz, GATE floating		300		μA
VCC Start-up Supply Current	I_{VCC_ST}	V_{CC}= V_{CC_ST}-1V		21.5		μA
VCC Supply Current during Green Mode	I_{VCC_GM}	VCC=13V+0.5V, V_{FB}<0.4V		50		μA
Current Limit(CS Pin)						
CS Cycle by Cycle Limit Voltage	V_{CS_MAX}			0.4		V
Leading Edge Blanking Time	T_{LEB2}	0.4V<V_{CS}<1.5V		400		ns
SCP Voltage	V_{CS_SCP}			1.5		V
Leading Edge Blanking Time of SCP	T_{LEB1}	V_{CS}>1.5V		250		ns
Feedback and OVP(FB Pin)						
FB Reference Voltage	V_{FB_REF}			2.5		V
OVP Threshold of FB	V_{FB_OVP}			2.7		V
FB OVP Hysteresis	$V_{FB\_OVP\_HYST}$		/	0.2	/	V
FB Start-up Voltage	V_{FB_ST}			0.4		V
PFC on Timer and Frequency Foldback						
Maximum On Time of GATE	T_{MOT}			33		μs
Maximum Switching Frequency	F_{MAX}			130		kHz
Minimum Switching Frequency	F_{MIN}	V_{FB}=2.6V, V_{CS}=1V		25		kHz
External OTP(OTP Pin)						
Sourcing Current at OTP	I_{OTP}			100		uA
OTP Threshold	V_{OTP}			2		V
OTP Hysteresis	V_{OTP_HYST}		/	0.2	/	V
Driver(GATE Pin)						
Gate High Voltage	V_{GS_H}			11		V
Maximum Source Current[5)]	I_{SRC_GATE}	GBD, GATE=0V		0.6		A
Maximum Sink Current[5)]	I_{SINK_GATE}	GBD, GATE=4V		1.4		A
Demagnetization Sense(ZCD Pin)						

T_A=25℃，unless otherwise noted						
Item	**Symbol**	**Condition**	**Min.**	**Typ.**	**Max.**	**Units**
Demagnetization Time-out	T_{DEM_MAX}			44		μs
Valley Sense(ZCD Pin)						
Valley sense threshold[5)]	dvdt	GBD	/	1.7	/	V/us
Valley sense time-out time[5)]	Tvalley	GBD		3.8		us
2nd OVP threshold	I_{OVP2}			1.3		mA
Fault Reset Delay Time	T_{FRD}			730		ms
Internal OTP						
Internal Over Thermal Protection Threshold[5)]	T_{OTP}	GBD		140		℃
Internal Over Thermal Protection Hysteresis[5)]	T_{OTP_HYST}	GBD	/	30	/	℃

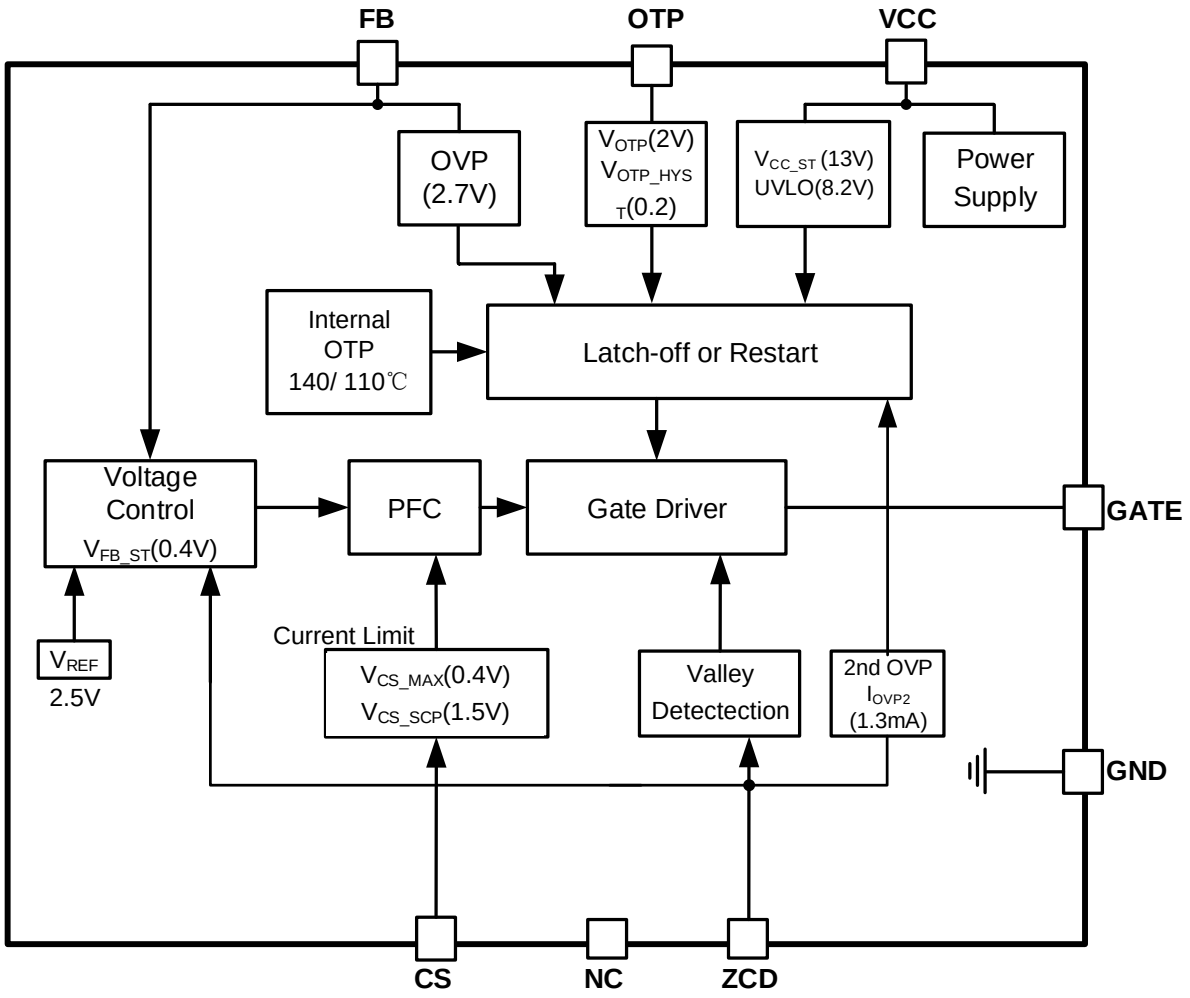
Note：

5) Guaranteed by design.

PIN FUNCTIONS

Pin SOP8	Name	Description
1	GATE	Gate driver for PFC MOSFET.
2	GND	Chip ground.
3	CS	Current sensing pin.
4	VCC	Power supply of the controller.
5	FB	Output voltage feedback pin.
6	OTP	Over temperature protection pin.
7	NC	
8	ZCD	Input from auxiliary winding for demagnetization timing and valley detection for PFC

BLOCK DIAGRAM



FEATURE DESCRIPTION

The JW1571 is a constant voltage (CV) controller which applies to non-isolation boost system with PFC. JW1571 can achieve excellent line and load regulation, high efficiency and low system cost with few peripheral components.

1. Start-Up

When VCC is charged to VCC Start-Up Voltage(VCC_ST)13V，the GATE driver begins to switch. When VCC is lower than VCC under voltage lockout (VCC_UVLO) 8.2V, the chip stops switching.

2. Constant Voltage Control

The JW1571 controls the output voltage from the information of FB pin. The output voltage is

$$V_O = V_{FB\_REF} \times (R_{FB1}+R_{FB2}) / R_{FB2}$$

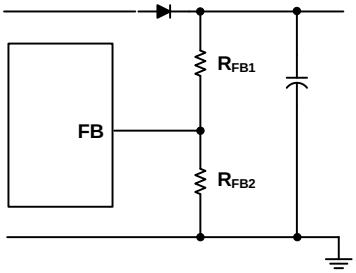


Fig.1 Output sense

Where

V_{FB_REF}– The FB Reference Voltage;

R_{FB1}, R_{FB2}– FB divide resistors.

3. Critical Conduction Mode Operation

JW1571 works in the critical conduction mode of the inductor current. When the power MOSFET is turned on, the inductor current increases from zero. The turn on time of the MOSFET can be calculated as:

$$T_{ON} = I_{PK} \times L / V_{IN}$$

Where,

L– Inductance.

V_{IN}– Input voltage.

I_{PK} is the peak current in one switch period and the maximum value (I_{PK_MAX}) is limited by the MOS current sensing resistor (R_{CS}).

$$I_{PK\_MAX}=V_{CS\_MAX}/R_{CS}$$

V_{CS_MAX}– CS Cycle by Cycle limit Voltage.

When the power MOSFET is turned off, the inductor current begins to decrease. The power MOSFET turns on again when the inductor current is zero. The turn off time of the MOSFET can be calculated as:

$$T_{OFF} = I_{PK} \times L / (V_{OUT}-V_{IN})$$

Where,

V_{OUT} – output voltage.

The power inductance can be calculated as:

$$L = V_{IN} \times (V_{OUT} - V_{IN}) / (f \times I_{PK} \times V_{OUT})$$

Where, f is the frequency of the boost system.

4. Frequency Fold back

Maximum switching frequency is limited at 130 KHz. At light load, switching frequency would fold back to 25 KHz.

If the load further decreases, IC will enter into skip mode to minimize standby loss. Skip mode is realized by OVP and OVP restart to skip some duty cycles.

5. Protection

JW1571 has multi-protection functions which largely enhance the safety and reliability of the system, including VCC UVLO, CS over voltage protection, FB over voltage protection and over temperature protection.

5.1 Over Voltage Protection

The over voltage protection is triggered if the following conditions is satisfied. V_{FB} is over than

FB over voltage protection threshold (V_{FB_OVP}). The internal comp will be reset and the power MOSFET gate driver stops switching unless FB voltage is decreased to V_{FB_OVP}-$V_{FB\_OVP\_HYST}$.

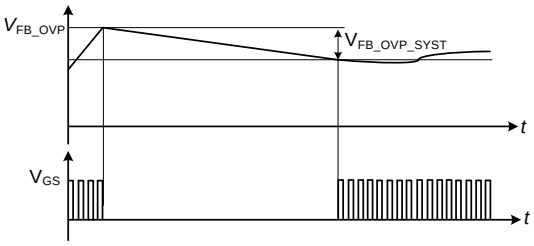


Fig.2 OVP

5.2 2nd OVP

The input voltage V_i is detected by the sink current of ZCD pin during main MOSFET on period, and the difference between output voltage V_o and input voltage V_i can be detected by the source current of ZCD pin during main MOSFET off.

$$I_{sink}=(Vi*N_{aux}/N1)/R_{ZCD}$$

$$I_{source}=(V_o-Vi)*N_{aux}/N1/R_{ZCD}$$

The output voltage V_o can be calculated by the threshold $I_{OVP2}=I_{sink}+I_{source}$.

$$V_{OVP2}=I_{OVP2}*N1*R_{ZCD}/N_{aux}$$

If the voltage sample exceeds I_{OVP2} for 3 consecutive switching cycles, a 2nd OVP fault is asserted, and then the device shuts down, and re-start after T_{FRD}.

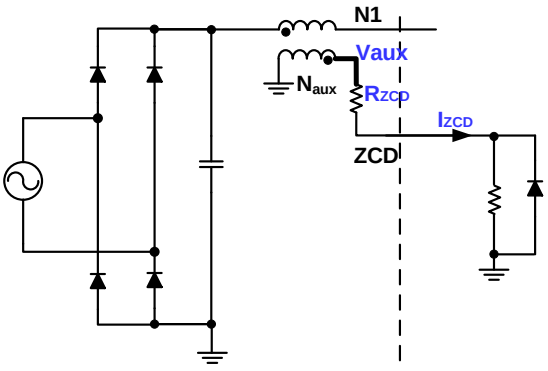


Fig.3 ZCD and Valley detection

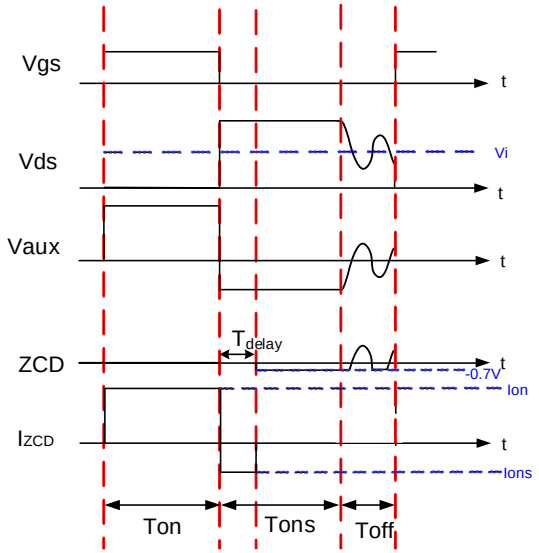


Fig.4 ZCD pin current sense waveform

5.3 Disable Function

The FB pin can also be used for device disabling. If V_{FB} is pulled down and lower than FB start up voltage (V_{FB_ST}), JW1571 stops switching and enters in green mode which reduces the power consumption. JW1571 will restart if V_{FB}>V_{FB_ST}.

5.4 Over Temperature Protection

JW1571 provides both Inner Over Thermal Protection and External Thermal Protection.
When internal temperature of the chip exceeds the Over Thermal Protection Threshold (T_{OTP}), JW1571 stops switching unless the junction temperature is decreased to T_{OTP}-T_{OTP_HYST}.

The OTP pin sources I_{OTP} and detects the voltage of the OTP pin. When the voltage decreases to the Over Thermal Protection Level (V_{OTP_TH}), JW1571 stops switching unless the voltage returns to V_{OTP_TH}+V_{OTP_HYST}.

5.5 Short Current Protection

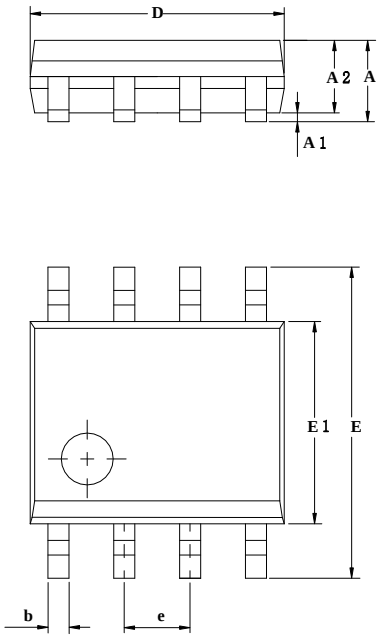
If the PFC inductor or MOSFET short during the working period that brings the CS pin voltage

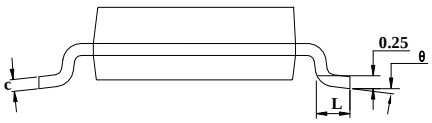
above the 1.5V, JW1571 will stop switching after 250ns leading edge blanking time. This causes the SCP fault.

When the voltage on CS pin over 0.4V after 400ns leading edge blanking time with output load increasing, JW1571 will work as Cycle by Cycle mode.

PACKAGE OUTLINE

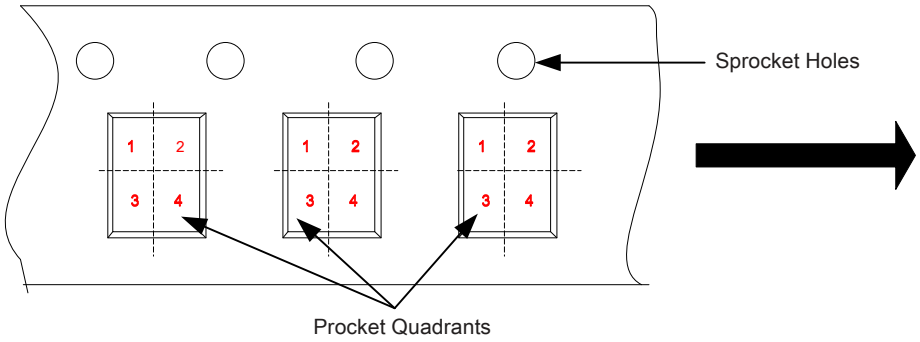
SOP8 UNIT: mm





Symbol	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.75
A1	0.05	0.15	0.25
A2	1.25	1.40	1.65
b	0.32	0.42	0.52
c	0.10	0.20	0.30
D	4.50	5.00	5.50
E	5.50	6.00	6.50
E1	3.50	3.90	4.30
e	1.27TYP		
L	0.40	—	1.27
θ	0°	—	8°

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPAE



Package Type	Pin1 Quadrant
SOP8	1

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