

DESCRIPTION

JWQ7821 is a 1A high accuracy, low noise, high PSRR linear regulator with 200mV maximum dropout voltage. JWQ7821 supports input voltage ranges from 2.2 V to 5.5 V and adjustable output voltage range from 0.8 V to 5V.

Low noise, high PSRR and high current capability makes JWQ7821 ideal power supply for noise sensitive applications, such as VCO, PLL, ADC and CMOS sensor. Accurate output voltage tolerance and excellent transient response ensures JWQ7821 optimal power supply for processors and digital loads, such as ASIC, FPGA, CPLD and DSP.

JWQ7821 provides 3mmx3mm DFN-8 package with guaranteed operating junction temperature range (T_J) from -40°C to $+125^{\circ}\text{C}$.

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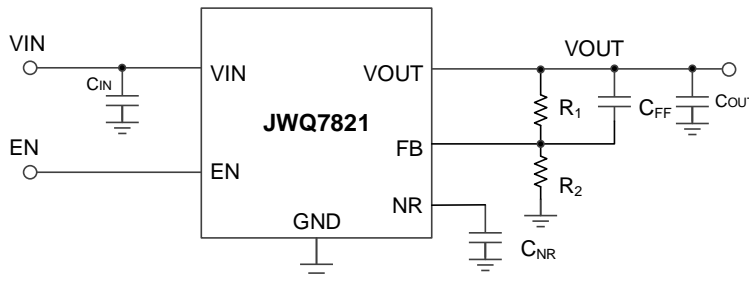
FEATURES

- AEC-Q100 Grade1 Qualified
- Input Voltage Range 2.2V to 5.5V
- Output Voltage Range 0.8V to 5V
- Low Dropout: 200mV Maximum at 1A
- High PSRR
 - 78dB at 1kHz
 - 42dB at 100kHz
 - 30dB at 1MHz
- 3% Accuracy over Line Regulation, Load Regulation and Operating Temperature Range
- 35.6uV_{RMS} Output Noise (100Hz - 100kHz)
- Stable with 4.7μF Ceramic Output Capacitors
- Over Temperature and Overcurrent Protection
- Offer DFN3x3-8 Package

APPLICATIONS

- Automotive ADAS Domain Control Unit
- Automotive Body Control Unit
- Automotive Telematics Control Unit
- Automotive Infotainment and Cluster system

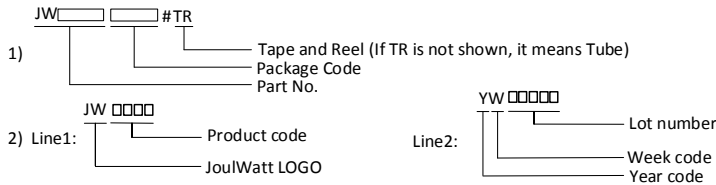
TYPICAL APPLICATION



ORDER INFORMATION

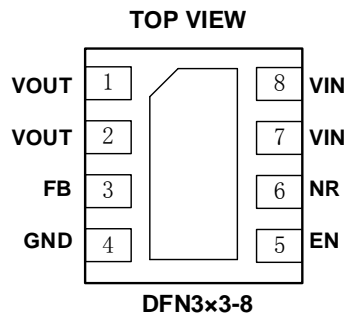
DEVICE1)	PACKAGE	TOP MARKING2)	ENVIRONMENTAL3)
JWQ7821DFNA#TR	DFN3x3-8	JWQ7821 YW□□□□□	Green

Notes:



3) All JoulWatt products are packaged with Pb-free and Halogen-free materials and compliant to RoHS standards.

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATING¹⁾

VIN, EN,OUT Pin	-0.3V to 7V
Other Pins	-0.3V to 7V
Junction Temperature ²⁾	150°C
Lead Temperature	260°C
Storage Temperature Range	-65°C to 150°C
ESD Susceptibility (Human Body Model)	±2kV
ESD Susceptibility (Charged Device Model)	±1kV
MSL	MSL1
Continuous Power Dissipation(TA=+25°C)DFN3x3-8	2.6W

RECOMMENDED OPERATING CONDITIONS³⁾

Input Voltage VIN	2.2V to 5.5V
Output Voltage VOUT	0.8V to 5V
Output Current	0A to 1A
Junction Temperature Range	-40°C to 125°C

THERMAL PERFORMANCE⁴⁾

	θ_{JA}	θ_{JC}
DFN3X3-8.....	38	6°C/W

Note:

- 1) Exceeding these ratings may damage the device. These stress ratings do not imply function operation of the device at other conditions beyond those indicated under RECOMMENDED OPERATING CONDITIONS.
- 2) The JWQ7821 includes thermal protection that is intended to protect the device in overload conditions. Continuous operation over the specified absolute maximum operating junction temperature may damage the device.
- 3) The device is not guaranteed to function outside of its operating conditions.
- 4) Measured on JESD51-7, 4-layer PCB

ELECTRICAL CHARACTERISTICS

$V_{IN}=V_{OUT(NOM)}+0.5V$ or $2.2V$, $V_{EN}=2V$, $I_{OUT}=1mA$, $C_{IN}=10\mu F$, $C_{OUT}=10\mu F$, $C_{NR}=10nF$, $T_J=-40^\circ C$ to $125^\circ C$, Unless otherwise stated.

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input Voltage	V_{IN}	$T_A=25^\circ C$	2.2		5.5	V
Undervoltage Lockout	UVLO	V_{IN} rising	1.86	2	2.2	V
Undervoltage Lockout Hysteresis	$UVLO_{HYST}$	V_{IN} falling		200		mV
Output Voltage Accuracy	ΔV_{OUT}	$V_{IN}=(V_{OUT(NOM)}+1V)$ to 5.5V $I_{OUT}=100mA$ to 1A $V_{IN}\geq 2.2V$	-3%		3%	V_{OUT}
Line Regulation	$\Delta V_{OUT}/\Delta V_{IN}$	$V_{IN}=(V_{OUT(NOM)}+1V)$ to 5.5V $I_{OUT}=100mA$		150		$\mu V/V$
Load Regulation	$\Delta V_{OUT}/\Delta I_{LOAD}$	$I_{OUT}=100mA$ to 1A		2		$\mu V/mA$
Load Current	I_{LOAD}		0		1	A
Maximum Output Current	I_{LOAD_MAX}		1			A
Ground Current	I_Q	$I_{OUT}=1mA$		350		μA
		$I_{OUT}=1A$		700	1200	
Shutdown Current (I_{GND})	I_S	$V_{EN}=0.4V$, $R_{LOAD}=1k\Omega$			2.5	μA
Dropout Voltage ⁵⁾	V_{DO}	$V_{IN}\geq 2.2V$, $I_{OUT}=500mA$			100	mV
		$V_{IN}\geq 2.5V$, $I_{OUT}=750mA$			150	
		$V_{IN}\geq 2.5V$, $I_{OUT}=1A$			200	
Current Limit	I_{CL}	$T_A=25^\circ C$	1.1	1.5	2	A
Feedback Pin Current	I_{FB}	$V_{IN}=5.5V$, $V_{FB}=0.8V$			1	μA
Power-Supply Rejection Ratio ⁶⁾	PSRR	$V_{IN}=4.3V$ $V_{OUT}=3.3V$ $I_{OUT}=750mA$	$f=100Hz$		70	dB
			$f=1kHz$		78	
			$f=10kHz$		70	
			$f=100kHz$		42	
			$f=1MHz$		30	
Output Noise Voltage ⁶⁾	V_{NO}	$BW=100Hz$ to $100kHz$ $V_{IN}=3.8V$, $V_{OUT}=3.3V$ $I_{OUT}=100mA$, $C_{NR}=C_{FF}=470nF$		35.6		μV_{RMS}
High Input Threshold	V_{ENH}	$V_{IN}=2.2V$ to $5.5V$, EN rising	1.2			V
Low Input Threshold	V_{ENL}	$V_{IN}=2.2V$ to $5.5V$, EN falling			0.4	V
EN Leakage Current	I_{EN_LKG}	$V_{EN}=5.5V$, $V_{IN}=5.5V$			1	μA
		$V_{EN}=0V$, $V_{IN}=5.5V$		0.001		
Rising Time	T_R	$V_{OUT(NOM)}=3.3V$, $V_{OUT}=0\% \sim 90\% V_{OUT(NOM)}$, $C_{OUT}=10\mu F$, $R_{LOAD}=3.3k\Omega$,		33		ms

$V_{IN}=V_{OUT(NOM)}+0.5V$ or $2.2V$, $V_{EN}=2V$, $I_{OUT}=1mA$, $C_{IN}=10\mu F$, $C_{OUT}=10\mu F$, $C_{NR}=10nF$, $T_J=-40\text{ }^\circ C$ to $125\text{ }^\circ C$, Unless otherwise stated.

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
		$C_{NR}=470nF$				
Thermal Shutdown ⁶⁾	T_{TSD}			160		$^\circ C$
Thermal Shutdown Hysteresis ⁶⁾	T_{TSD_HYST}			20		$^\circ C$

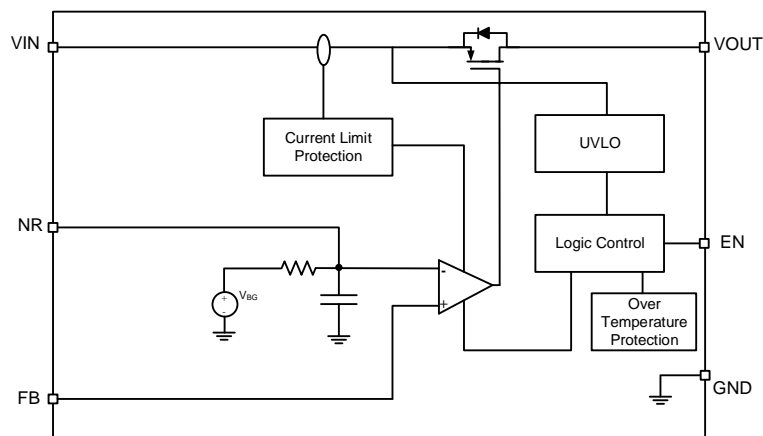
Note:

- 5) Dropout voltage is the voltage difference between input and output at which the output voltage drops to 100mV below its nominal value.
- 6) Guaranteed by design.

PIN DESCRIPTION

Pin DFN3X3-8	Name	Description
1	VOUT	Output of the regulator. A 4.7μF or larger output capacitor is recommended
2		
3	FB	Feedback pin. Connected to error amplifier. The FB reference voltage is 0.8V
4	GND	Ground
5	EN	Enable pin. Active high. Driving this pin to logic high enables the device; driving this pin to logic low disables the device. If enable functionality is not required, this pin must be connected to VIN.
6	NR	Noise-reduction and soft-start pin. Connecting an external capacitor between this pin and ground reduces reference voltage noise and also enables the soft-start function. Although not required, a 10nF or larger capacitor is recommended to be connected from NR/SS to GND (as close to the pin as possible) to maximize ac performance.
7	VIN	Input supply voltage pin. A 2.2μF or larger ceramic capacitor from IN to ground is required to reduce the impedance of the input supply. Place the input capacitor as close to the input as possible.
8		
Exposed Pad	-	The exposed pad should be connected to a large ground plane to maximize thermal performance.

BLOCK DIAGRAM

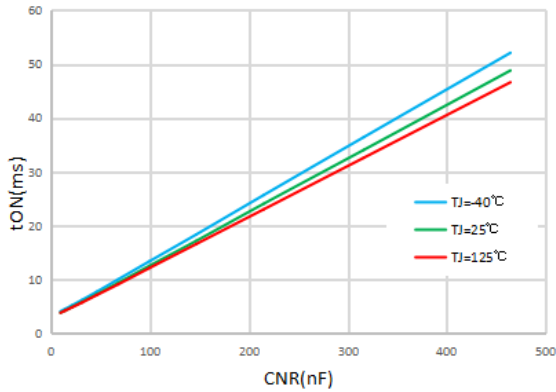


TYPICAL PERFORMANCE CHARACTERISTICS

At $V_{Onom} = 3.3\text{ V}$, $V_{IN} = V_{Onom} + 0.5\text{ V}$ or 2.2 V (whichever is greater), $I_o=100\text{ mA}$, $V_{(EN)} = V_{IN}$, $C_{(IN)} = 2.2\text{ }\mu\text{F}$, $C_{(OUT)} = 4.7\text{ }\mu\text{F}$, and $C_{(NR)} = 0.01\text{ }\mu\text{F}$, $T_A=25^\circ\text{C}$, unless otherwise noted

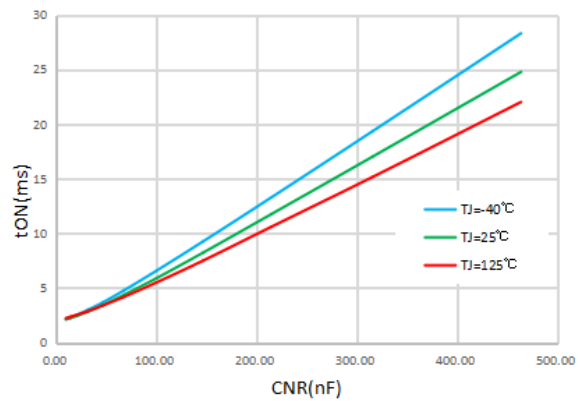
Turn-on time(EN high to 90%Vout) vs.CNR

$V_{IN}=4.3\text{V}, V_{OUT}=3.3\text{V}, C_{FF}=10\text{nF}$



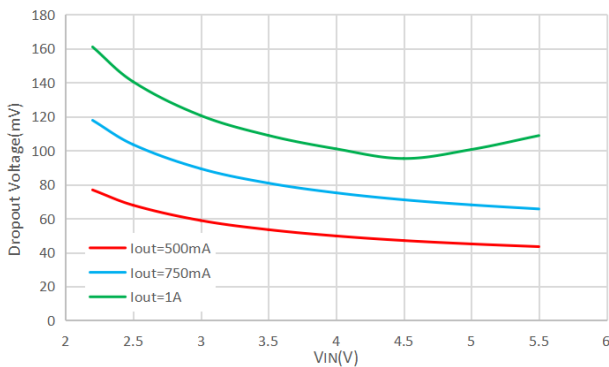
Rising time(10%Vout to 90%Vout) vs.CNR

$V_{IN}=4.3\text{V}, V_{OUT}=3.3\text{V}, C_{FF}=10\text{nF}$



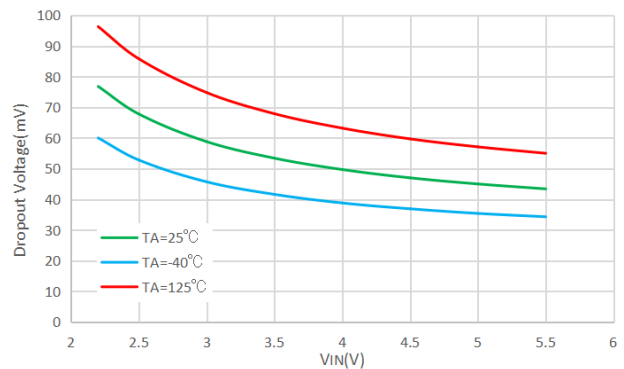
Dropout voltage vs Input voltage

$T_A=25^\circ\text{C}$



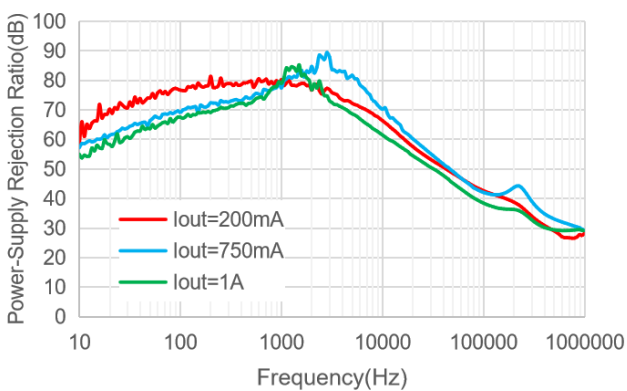
Dropout voltage vs Load current

$I_{OUT}=500\text{mA}$



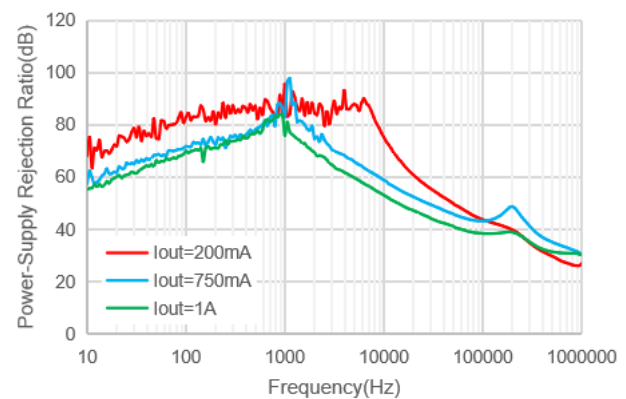
PSRR vs Frequency

$V_{OUT}=V_{IN}-1\text{V}, C_{IN}=0\text{F}, C_{OUT}=10\text{ }\mu\text{F}, C_{NR}=470\text{nF}, C_{FF}=470\text{nF}$



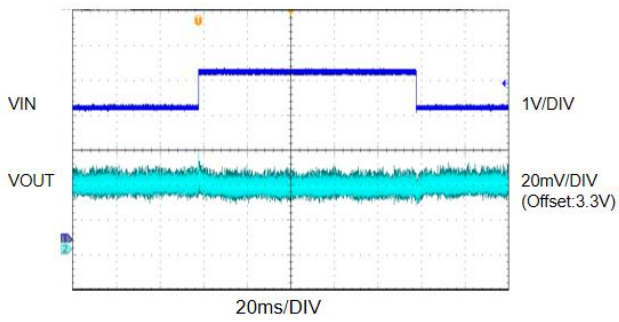
PSRR vs Frequency

$V_{OUT}=V_{IN}-0.5\text{V}, C_{IN}=0\text{F}, C_{OUT}=10\text{ }\mu\text{F}, C_{NR}=470\text{nF}, C_{FF}=470\text{nF}$



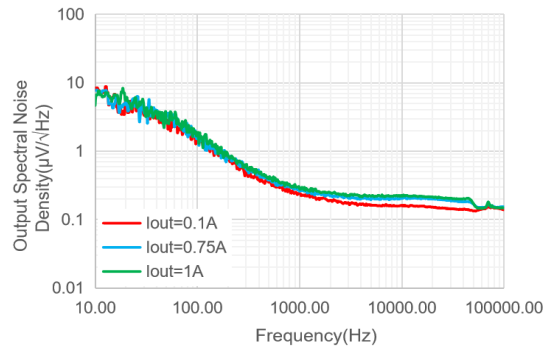
Line transient

$V_{IN}=3.8V$ to $4.8V$ to $3.8V$, $I_{OUT}=500mA$



Output spectral noise density vs Frequency

$V_{OUT}=V_{IN}-0.5V$, $C_{IN}=10\mu F$, $C_{OUT}=10\mu F$, $C_{NR}=470nF$, $C_{FF}=470nF$



FUNCTIONAL DESCRIPTION

The JWQ7821 is a low noise, low quiescent current linear regulator. The input voltage range is from 2.2V to 5.5V, and the output current is up to 1A. The minimum required output capacitance for stable operation is 4.7 μ F effective capacitance after consideration of the temperature and voltage coefficient of the capacitor.

Output Transistor

The JWQ7821 builds in a P-MOSFET output transistor which provides a low switch-on resistance for low dropout voltage applications.

Error Amplifier

The Error Amplifier (EA) compares the internal reference voltage V_{REF} with the output feedback voltage V_{FB} through the internal divider. Output of the error amplifier (EA) is used to control the gate voltage of P-MOSFET and ensures that the device provides good line and load regulation at output voltage.

Enable

The device is active when EN pin is set to high. For proper operation, this pin must be terminated and must not be left floating. With EN pin set to low, the device enters shutdown mode with less than 1 μ A current consumption.

Current Limit Protection

JWQ7821 provides current limit function to prevent the device from damages during the over load or shorted-circuit condition. The current is detected by a sensing transistor,

which monitors and controls the pass transistor's gate voltage, limiting the output current to 1.1A (TYP.). The PMOS pass transistor dissipates $(V_{IN} - V_{OUT}) \times I_{LIMIT}$ until thermal shutdown is triggered and the device turns off. When the device cools, the internal thermal shutdown circuit turns the device back on. If the fault condition continues, the device cycles between current limit and thermal shutdown.

Low Output Noise

Any internal noise at the JWQ7821 reference voltage is reduced by a first order low-pass RC filter before it is passed to the output buffer stage. The low-pass RC filter has a -3dB cut-off frequency of approximate 0.1Hz.

Transient Response

As with any regulator, increasing the size of the output capacitor reduces overshoot and undershoot magnitude but increases the duration of the transient response. Using a larger noise-reduction capacitor C_{NR} , bypass capacitor C_{FF} , or both types of capacitors can improve line transient performance

Thermal Protection

When the temperature of the JWQ7821 rises above T_{TSD} , it is forced into thermal shut-down. When the junction temperature cools to approximately $T_{TSD} - T_{TSD_HYST}$ the output circuitry is again enabled.

APPLICATION INFORMATION

The JWQ7821 is a new generation LDO regulators that use innovative circuitry to achieve wide bandwidth and high loop gain, resulting in extremely high PSRR (over a 1-MHz range) at very low headroom ($V_{IN} - V_{OUT}$). A noise reduction capacitor (CNR) at the NR pin and a bypass capacitor (CFF) bypass noise generated by the bandgap reference to improve PSRR, while a quick-start circuit fast-charges the noise reduction capacitor. This regulator offers sub-bandgap output voltages, current limit, and thermal protection, and is fully specified from -40°C to 125°C .

Dropout Voltage

The JWQ7821 uses a PMOS pass transistor to achieve low dropout. When ($V_{IN} - V_{OUT}$) is less than the dropout voltage (VDO), the PMOS pass device is in its linear region of operation and the input-to-output resistance is the $R_{DS(ON)}$ of the PMOS pass element. VDO scales approximately with output current because the PMOS device in dropout behaves the same way as a resistor.

Input and Output Capacitor Selection

The JWQ7821 is designed to support low ESR (Equivalent Series Resistance) ceramic capacitors. It is recommended to use ceramic capacitors with X7R, X5R, and COG-rated ceramic capacitors to get good capacitive stability across different temperatures.

A $4.7\mu\text{F}$ or greater output ceramic capacitor is suggested to ensure stability. Input capacitance is selected to minimize transient input drop during load current steps. For general applications, an input capacitor of at least $2.2\mu\text{F}$ is highly recommended for minimal input impedance. If the trace inductance between the

JWQ7821 input pin and power supply is high, a fast load transient can cause V_{IN} voltage level ringing above the absolute maximum voltage rating which damages the device. Adding more input capacitors is available to restrict the ringing and keep it below the device absolute maximum ratings.

Output Voltage Setting

For the JWQ7821, the voltage on the FB pin sets the output voltage and is determined by the values of R1 and R2. The values of R1 and R2 can be calculated for any voltage using the formula given in Equation :

$$V_{out} = \frac{R1 + R2}{R2} \times 0.8$$

Using lower values for R1 and R2 is recommended to reduce the noise injected from the FB pin. Note that R1 is connected from VOUT pin to FB pin, and R2 is connected from FB to GND.

Output Noise

In general, the dominant noise source is from the internal bandgap for most LDOs. If a noise reduction capacitor (CNR) is used with the JWQ7821, the bandgap does not contribute significantly to noise. Instead, noise is dominated by the output resistor divider and the error amplifier input. If a bypass capacitor (CFF) across the high-side feedback resistor (R1) is used with the JWQ7821 in addition to CNR, noise from these other sources can also be significantly reduced.

Adjustable Rise Time

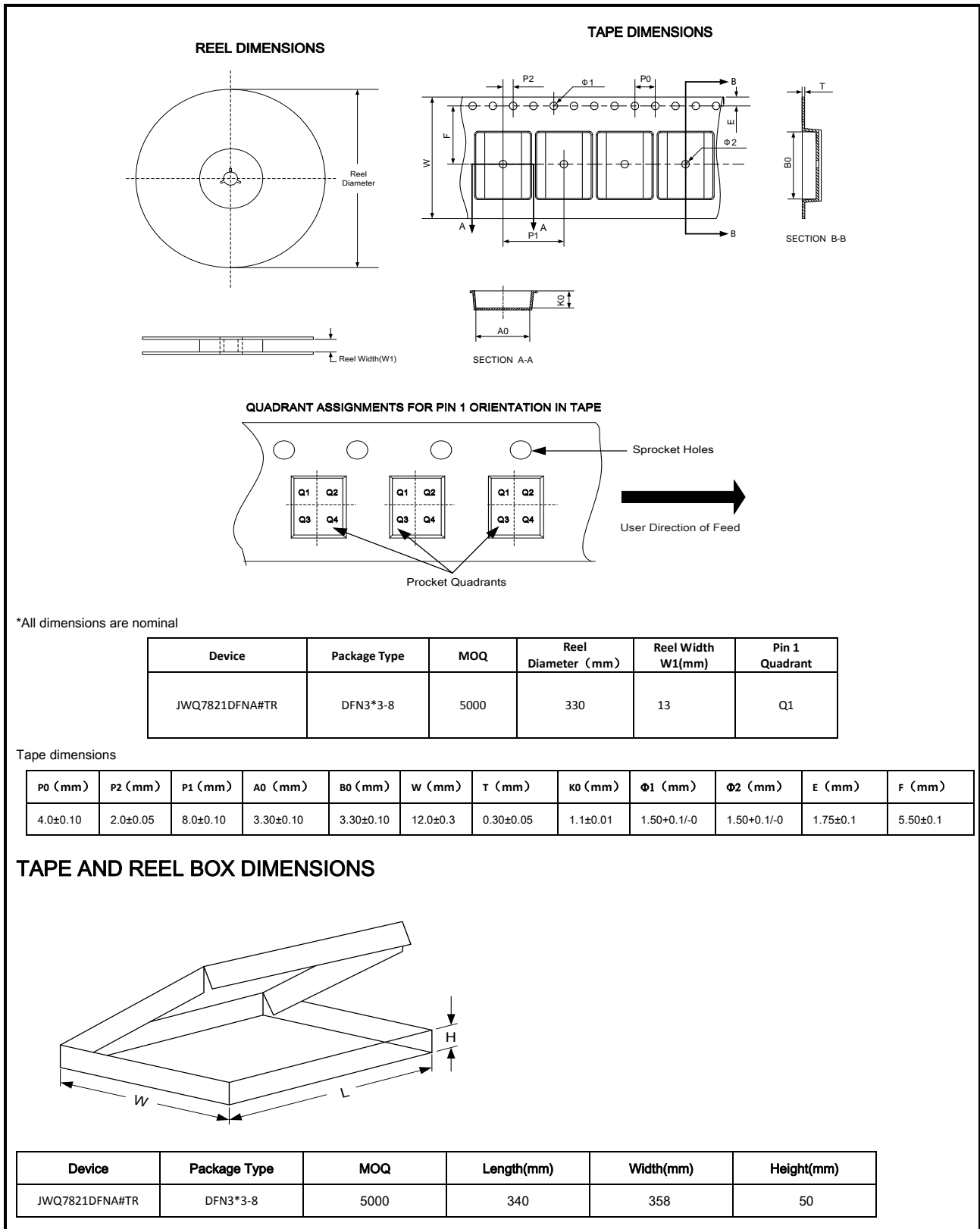
The rise time of JWQ7821 can be adjusted individually by CFF (connected between VOUT

pin and FB pin) and CNR (connected between NR/SS and GND pins). The approximate rise time of VOUT measured on a typical device at VOUT = 3.3V is shown in table 1.

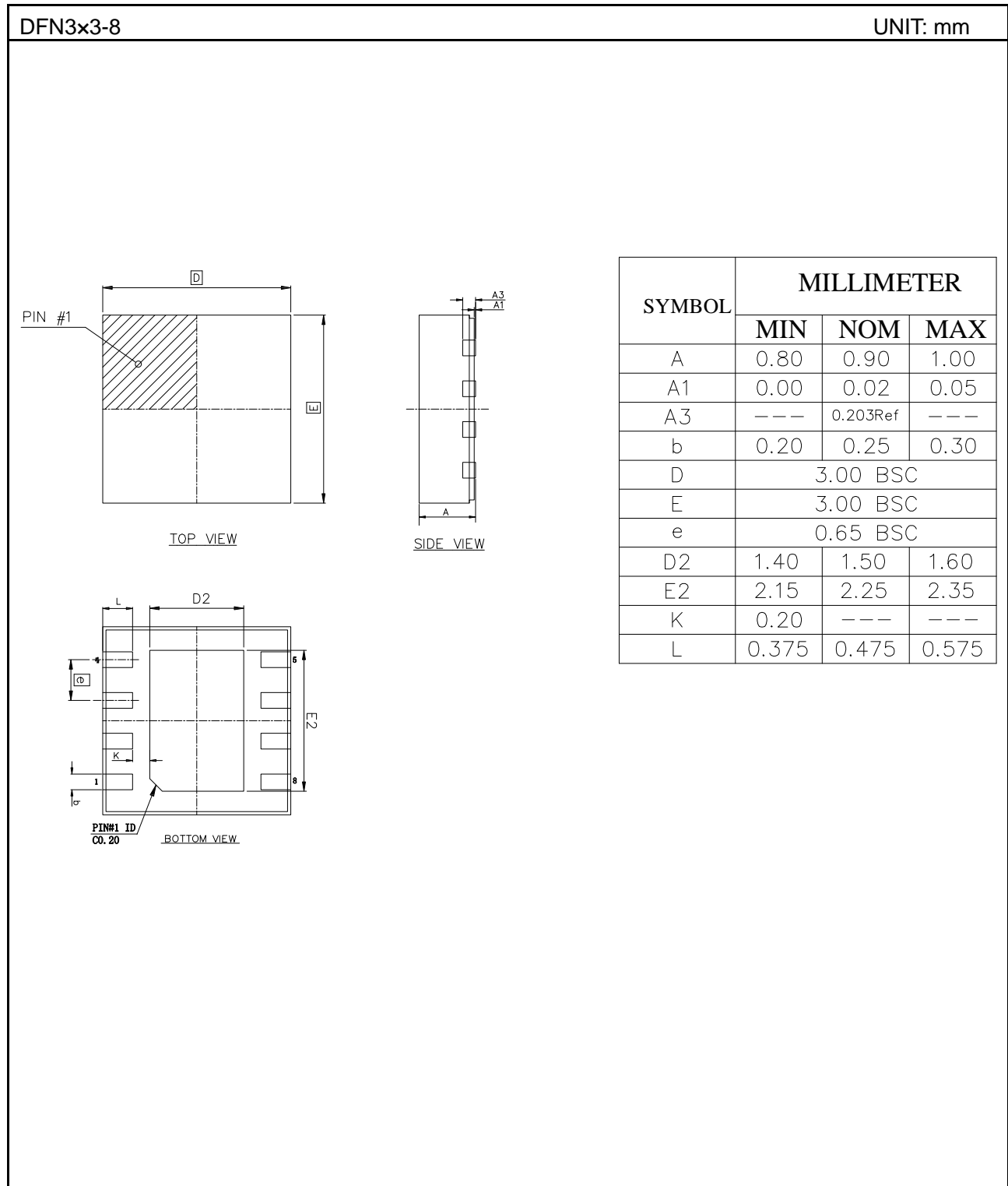
Table 1:

CNR (nF)	Rising time, Tr(ms) 10%-90% of VOUT, COUT=4.7µF, CIN=2.2µF, Typical values at 25°C, VIN=4.3V, VOUT=3.3V, RLoad=3.3kohm		
	CFF=NC	CFF=10nF	CFF=470nF
0	2.1	2.24	33.7
10	2.37	2.58	34.4
100	6.8	7.24	37.8
470	30.3	30.6	53.8

TAPE AND REEL INFORMATION



PACKAGE OUTLINE



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