JW3371

4~10 Series Cell Battery Monitor and Protection IC

DESCRIPTION

JW3371 is a multi-cell battery stack monitoring and protection IC that includes a 14-bit ADC for battery voltage and temperature sense, a 16-bit ADC for charge/discharge current sense.

JW3371 provides passive balance function for each cell and allows at most 3 consecutive cells being discharged simultaneously.

JW3371 communicates with external control unit via SPI interface. More JW3371 can operate in series to monitor long string battery.

JW3371 integrates complete protection function including over/under voltage, over/under temperature, over charge/discharge current, short-circuit and open wire detection. When fault(s) happen, JW3371 will send alarm signal to inform host and shutdown CHG or DSG.

JW3371 integrated pre-charge and pre-discharge drivers for the deep discharge battery or some big capacitor load startup.

JW3371 supports both Sleep mode and Ship mode to achieve high efficiency with low power when charge/discharge current is minor.

FEATURES

- Monitor 10 Series Cell Battery and Support Series Operation
- 14-bit ΔΣ ADC Samples Battery Voltage and Accuracy is ±3mV typ.@ (2.3~4.3V, T_A=25ºC)
- Provide Filtering 3 Channels Thermal Sense and Accuracy is ±1℃(No Considering NTC Resistor Offset)
- Battery Over/Under Voltage Protection
- Battery Over/Under Temperature Protection
- Open Wire Connection Detection
- 10 Cells Passive Balance
  On-Chip Passive Cell Balancing Switches
  Provide Off-Chip Passive Balancing
- 16-bit ΔΣ ADC Senses Charge/Discharge Current and Accuracy is
  ±75μV typ.@ (-100 mV ~100mV, T_A=25ºC)
  ±100μV typ.@ (-190 mV ~190mV, T_A=25ºC)
- Over Charge/Discharge Current Protection
- Discharge Short Protection
- Reliable SPI Communication (Mode3)
- 3.3V LDO Output for External Application
- External Protection N-MOSFETs
- Integrated Pre-charge/discharge Function
- Low Power Consumption

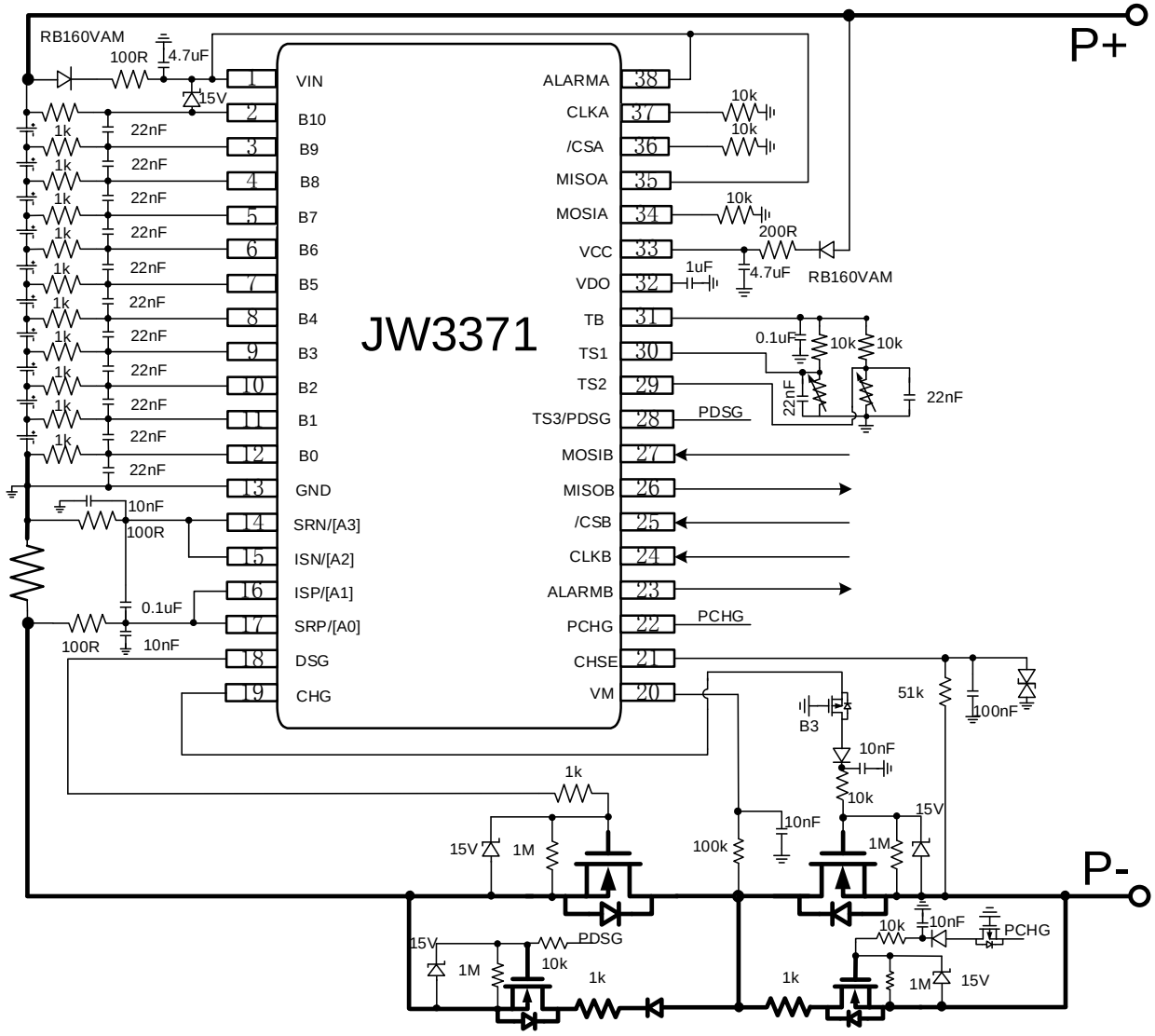
During Operation	1.5mA typ. 1.8mA Max
During Sleep	18μA typ. 20μA Max
During Ship	3.2μA typ. 5μA Max

- Package: TSSOP38

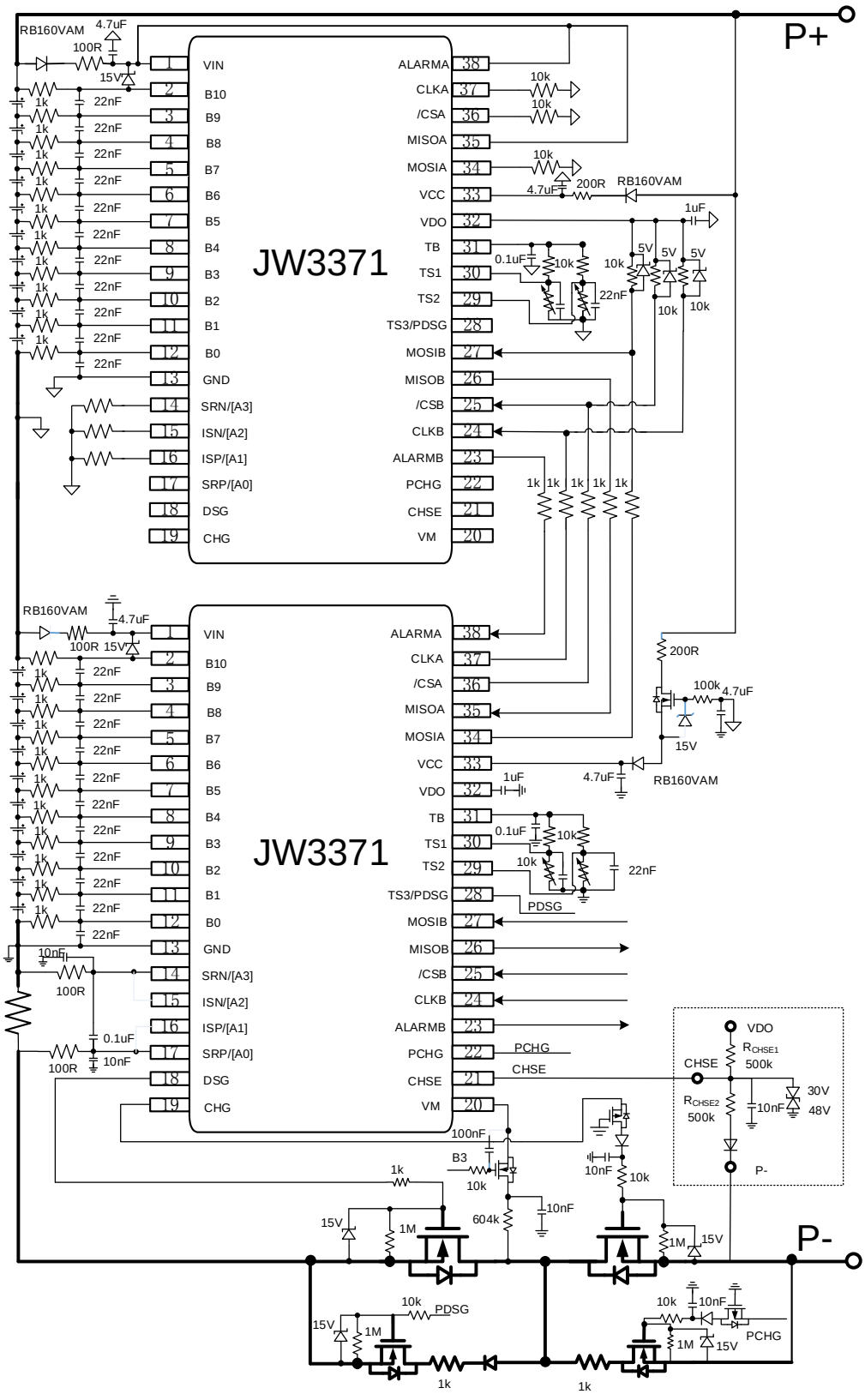
APPLICATIONS

- Electric Bicycles, Motorcycles.
- Backup Battery Systems
- Hybrid Electric Vehicle

TYPICAL APPLICATION



10 Cells Low Side Driver



20 Cells Low Side Driver

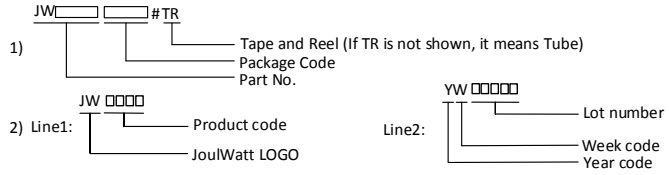
Note: When the charger voltage is 30V higher than the battery voltage, there will be leakage current during charging.

$$I_{Leakage}(A) = \frac{V_{charger}(V) - V_{BAT}(V) - V_{TVS}(V)}{51k\Omega}$$

ORDER INFORMATION

DEVICE[1)]	PACKAGE	TOP MARKING[2)]	ENVIRONMENTAL[3)]
JW3371TSSOPF#TR	TSSOP38	JW3371 YW□□□□□	Green

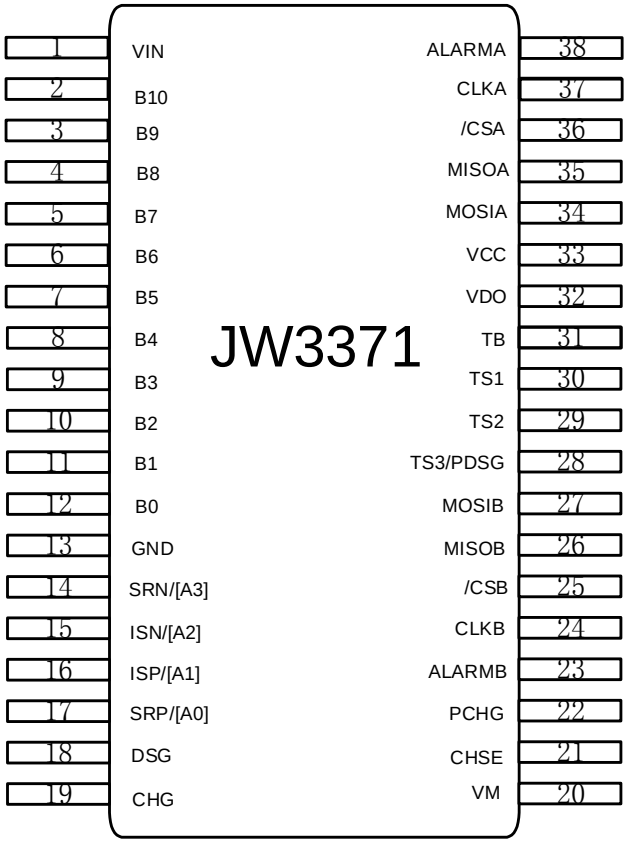
Notes:



3) All JoulWatt products are packaged with Pb-free and Halogen-free materials and compliant to RoHS standards.

PIN CONFIGURATION

TOP VIEW



TSSOP38

ABSOLUTE MAXIMUM RATING[1)]

VIN-GND, VCC-GND ..... -0.3V to 60V
B(N)-GND N=0..4.....-0.3V to 40V
B(N)-GND N=5..10 .....-0.3V to 60V
B(N)-B(N-1) N=1..10..... -0.3V to 20V
B10-VIN.....-20V to 0.6V
SRP..... -5V to 40V
CHSE……..... GND-40V to 60V
VM, CHG……..... -0.3V to 60V
DSG ..... -0.3V to 20V
/CSB, CLKB, MOSIB.....-5V to 6.5V
MOSIA, /CSA, CLKA, MISOA, ALARMA…….....-0.3V to 60V
All Other Pins..... -0.3V to 6.5V
Junction Temperature[2)]..... 150ºC
Lead Temperature 260ºC
Storage Temperature..... -40ºC to +125ºC

RECOMMENDED OPERATING CONDITIONS[3)]

B(N)-B(N-1) N=1..10.....0V to 5V
VIN-GND .....8V to 50V
Operating Junction Temperature..... -40ºC to +85ºC

THERMAL PERFORMANCE[4)]

	θ_{JA}	θ_{JC}
TSSOP38	86	19°C/W

Note:

1) Exceeding these ratings may damage the device. These stress ratings do not imply function operation of the device at any other conditions beyond those indicated under RECOMMEND OPERATION CONDITIONS.
2) The JW3371includes thermal protection that is intended to protect the device in overload conditions. Continuous operation over the specified absolute maximum operating junction temperature may damage the device.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARATERISTICS

VIN=VCC=36V, T_A = 25ºC, unless otherwise stated.

ITEM	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNITS
Power Supply						
Operation voltage on VIN	V_{IN}		8		50	V
Startup voltage of VIN and VCC	V_{IN_START}			5.5	6	V
Operation current of VIN and VCC	I_{IN_O}	T_A=-40℃[5)]	1.2	1.45	1.8	mA
		T_A=25℃	1.3	1.5	1.8	mA
		T_A=85℃[5)]	1.4	1.64	1.9	mA
Sleep current of VIN and VCC	I_{IN_L}	T_A=-40℃[5)]	17	18	20	μA
		T_A=25℃, VDO no load, CHG & DCHG off	17	18	20	μA
		T_A=85℃[5)]	19	20	24	μA
Ship current of VIN	I_{IN_S}	T_A=-40℃[5)]	2.3	2.6	4	μA
		T_A=25℃	2.4	3.2	5	μA
		T_A=85℃[5)]	3.4	3.8	6	μA
LDO output voltage	V_{DO}	No Load	3.2	3.3	3.4	V
		I_{LOAD}=50mA	3.2	3.3	3.4	V
Thermal bias voltage (3.3V)	V_{TB}	No Load	3.26	3.3	3.31	V
		I_{LOAD}=2mA	3.26	3.3	3.31	V
LDO output current limit	I_{LMT_LDO}		70	100		mA
LDO turn off delay time	t_{LDO_OFF}[5)]			1		s
TB output current limit	I_{LMT_TB}			12		mA
LDO/TB over thermal warning threshold	T_{LDO_WAR}[5)]			125		ºC
LDO/TB over thermal protection threshold	T_{LDO_PRO}[5)]			150		ºC
Thermal shutdown threshold	T_{SHUTD}[5)]			150		ºC
Thermal hysteresis	T_{HYS}[5)]			25		ºC
14-BIT ADC (for cell voltage and temperature monitor)						
Resolution of ADC	V_{VREV}[5)]			0.305		mV
Measurement range of ADC	V_{RANGEV}[5)]		0		5.0	V
Offset voltage of measurement	$V_{OFFSETV}$[5)]		-0.5	0	0.5	mV

Error voltage of measurement	V_{ERR}	V_{CELL}=2.3V~4.3V T_A=25ºC		±3	±6	mV
		V_{CELL}=2.3V~4.3V T_A= - 20ºC ~65ºC[5)]		±4	±10	mV
		V_{CELL}=2.3V~4.3V T_A= - 40ºC ~85ºC[5)]		±5	±15	mV
Frequency of ADC clock	f_{CLK}	Normal mode T_A=25ºC	0.9	1	1.1	MHz
		Normal mode T_A= - 40ºC~85ºC[5)]	0.85	1	1.15	MHz
Measure time of single cell	t_{UNITV}[5)]	Fast mode， Setting: Control Parameter Set: bit [49:48]=0x0		0.64		ms
Measure time of 10 cells	t_{CYCLE}[5)]	Fast mode， Setting: Control Parameter Set: bit [49:48]=0x0		6.4		ms
Cell balancing relaxation time before cell voltage measured	t_{CB_RELAX}[5)]	Fast mode， Setting: Control Parameter Set: bit [49:48]=0x0		0.64		ms
Temperature measurement interval	t_{TEMP}[5)]	Fast mode， Setting: Control Parameter Set: bit [49:48]=0x0		64		ms
16-BIT ADC (for current monitor)						
Resolution of ADC	V_{VREC}[5)]			6		μV
Measurement range of ADC	V_{RANGEC}[5)]		-190		190	mV
Error voltage of measurement	V_{ERRC}	$V_{SRP-SRN}$ = - 100mV~100mV T_A=25ºC	-150	±75	150	μV
		$V_{SRP-SRN}$ = - 190mV~190mV T_A=25ºC	-300	±100	300	μV
		$V_{SRP-SRN}$ = - 100mV~100mV T_A=-20~65ºC[5)]	-180	±80	180	μV
		$V_{SRP-SRN}$ = - 190mV~190mV T_A=-20~65ºC[5)]	-360	±110	360	μV

			$V_{SRP-SRN}$ = -100mV~100mV T_A=-40~85ºC[5]	-300	±100	300	μV
			$V_{SRP-SRN}$ = -190mV~190mV T_A=-40~85ºC[5]	-600	±200	600	μV
Current measure time cycle		t_{UNITC}[5]			132		ms
Protection							
Over charge/ Over discharge	Threshold Range	V_{OC}/V_{OD}		0		5	V
	Step				19.53		mV
Over charge delay time	Threshold Range	t_{OC}[5]		0.128		1.92	s
	Step				128		ms
	Threshold Range	t_{OC}[5]		0.512		7.68	s
	Step				512		ms
	Accuracy			75%*t_{OC}-Step	t_{OC}	125%*t_{OC}	
Over discharge delay time	Threshold Range	t_{OD}[5]		0.512		7.68	s
	Step				512		ms
	Threshold Range	t_{OD}[5]		1		15.36	s
	Step				1024		ms
	Accuracy			75%*t_{OD}-Step	t_{OD}	125%*t_{OD}	
Temperature protection	Threshold Range	V_{OT}		0		3.3	V
	Step				19.53		mV
Temperature protection delay	Threshold Range	t_{OT}[5]		0.512		7.68	s
	Step				512		ms
				75%*t_{OT}-Step	t_{OT}	125%*t_{OT}	
Discharge over current 1st Grade	Threshold Range	V_{DOI1}		0		190	mV
	Step				0.781		mV
	Accuracy			-2		2	mV
Discharge over current 1st Grade protection delay time	Threshold Range	t_{DOI1}[5]		0.128		8.064	s
	Step				256		ms
	Accuracy			75%*t_{DOI1}-Step	t_{DOI1}	125%*t_{DOI1}	
	Threshold Range	V_{DOI2}		0		190	mV
	Step				0.781		mV

Discharge over current 2nd Grade	Accuracy			-2		2	mV
Discharge over current 2nd Grade protection delay time	Threshold Range	t_{DOI2}[5]		32		992	ms
	Step				32		ms
	Threshold Range	t_{DOI2}[5]		4		124	ms
	Step				4		ms
Discharge over current 2nd Grade protection delay time	Threshold Range	t_{DOI2}[5]		32		992	ms
	Step				32		ms
	Threshold Range	t_{DOI2}[5]		4		124	ms
	Step				4		ms
	Accuracy			75%*t_{DOI2}-Step	t_{DOI2}	125%*t_{DOI2}	
Short circuit protection	Threshold Range	V_{SHT}		42.5		500	mV
	Step				7.5		mV
	Accuracy			-10		10	%
Short circuit protection delay	Threshold Range	t_{SHT}[5]		64		2048	μs
	Step				64		μs
	Accuracy			75%*t_{SHT}-Step	t_{SHT}	125%*t_{SHT}	
Charge over current	Threshold Range	V_{COI}		0		200	mV
	Step				0.781		mV
	Accuracy			-2		2	mV
Charge over current protection delay time	Threshold Range	t_{COI}[5]		0.64		960	ms
	Step				64		ms
	Accuracy			75%*t_{COI}-Step	t_{COI}	125%*t_{COI}	
Open wire detection current[5]				40	85	130	μA
Open wire detection threshold[5]					200		mV
Balance							
R_{DSON} of balance switch		R_{DSON_BSW}			50		Ω
Watchdog timer range for balance	Programmable	t_{WD}[5]		0.512		120	s
	Step				512		ms
	Accuracy			75%*t_{WD}-Step	t_{WD}	125%*t_{WD}	
Balance over thermal protection threshold		T_{BALAN}[5]			150		ºC

Balance over thermal protection hysteresis	T_{BALAN_HYST} [5]			25		ºC
Charge and Discharge Drivers						
The high voltage of external MOSFET driver	V_{DRIV}	CHG, DSG,	10	12	14	V
The high voltage of external MOSFET driver	V_{PDRIV}	PCHG, PDSG	4.5	6	6.5	V
The sink current of external MOSFET driver	I_{SINK}	CHG	9	10		mA
		DSG	76	95		mA
The source current of external MOSFET driver	I_{SOURCE}	CHG, DSG	5	10		mA
The sink current of Pre-charge and Pre-discharge	I_{PD}	PCHG, PDSG	4	5		mA
The source current of Pre-charge	I_{PUCHG}	PCHG	2.8	4		mA
The source current of Pre-discharge	I_{PUDSG}	PDSG	2.8	5		mA
Load State Detection and Charger Detection and Wakeup						
Load detection voltage threshold	V_{VM}		0.7	1	1.6	V
Load detection pull down resistor	R_{VMS}			40		kΩ
Charger detection voltage threshold	V_{CHSE}		0.15	0.3	0.45	V
Charger detection pull up current	I_{CHSE}		0.5	1	1.7	μA
Charger detection falling edge deglitch time	t_{CHSE} [5]				30	ms
Low Current Wakeup Threshold	V_{LC}	Programmable	0.05	0.35	0.65	mV
			0.1	0.4	0.7	
Low current wakeup time	t_{LC} [5]				30	ms
/CSB falling edge wake up deglitch time	$t_{/CSB}$ [5]				30	ms
Input Current						
B10~B0 pin leakage current	I_{LK}		-1.0	0	1.0	μA
ALARMB (except device address=1) Open Wire and Interrupt Detection						
ALARMB open wire detection	Cycle [5]			8		s
	High level time [5]			4		ms
ALARMB interrupt detection	Cycle [5]			100		ms
	High level time [5]	Interrupt off CHG	5		14	ms
	High level time [5]	Interrupt off DSG	15		25	ms

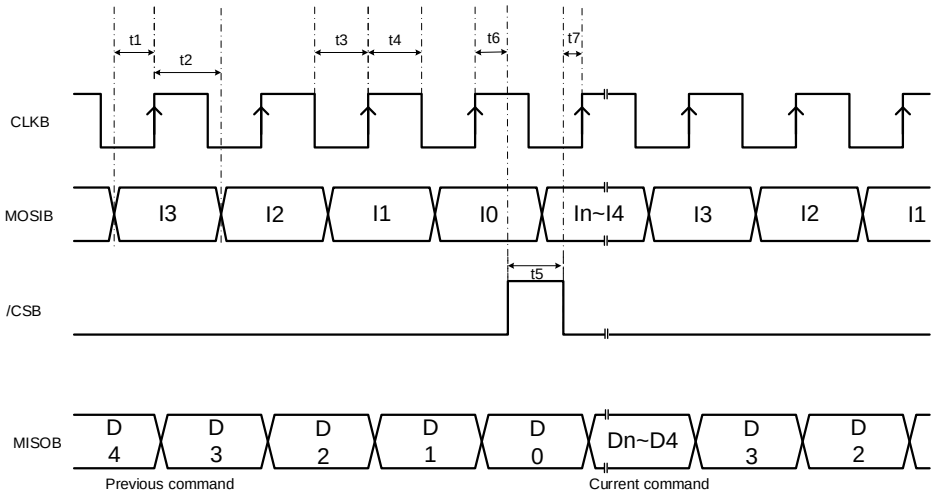
	High level time[5]		Interrupt off CHG and DSG	30		50	ms
SPI Voltage Specifications							
Internal clock frequency at normal mode		f_{SCLU}		0.9	1	1.1	MHz
Internal clock frequency at Sleep mode or idle mode		f_{SCLD}		20	40	60	kHz
Threshold of logic “L” of MOSIB, /CSB, CLKB		V_{ILB}				0.8	V
Threshold of logic “H” of MOSIB, /CSB, CLKB		V_{IHB}		2			V
Output voltage of logic “L” of MISOB, ALARMB		V_{OLB}			0		V
Output voltage of logic “H” of MISOB, ALARMB		V_{OHB}			3.3		V
Threshold of logic “L” of ALARMA, MISOA		V_{ILA}				VIN+0.5	V
Threshold of logic “H” of ALARMA, MISOA		V_{IHA}		VIN+2.2			V
Output voltage of logic “L” of MOSIA, /CSA, CLKA		V_{OHA}			VIN		V
SPI Current Specifications							
The sink current of MISOB, ALARMB when output “L”		I_{SINKB}		18	30	52	mA
The source current of MISOB, ALARMB when output “H”		$I_{SOURCEB}$		8	13	21	mA
The pull up resistor of MOSIB, /CSB, CLKB		R_{PULLUP}		0.9	1.75	2.6	kΩ
The sink current of MOSIA, /CSA, CLKA when output “L”		I_{SINKA}		3	4	6	mA
SPI Timing Specifications							
Clock operating frequency		f_{SCL}[5]				1	MHz
MOSIB, MISOB valid to CLKB rising setup		t1[5]		10			ns
MOSIB, MISOB valid to CLKB rising hold		t2[5]		250			ns

CLKB low	t3[5)]		400			ns
CLKB high	t4[5)]		400			ns
/CSB rising edge to /CSB falling edge	t5[5)]	Normal mode	5			µs
		Low power mode	125			
CLKB rising edge to /CSB rising edge	t6[5)]	Normal mode	3			
		Low power mode	75			
/CSB falling edge to CLKB rising edge	t7[5)]	Normal mode	3			
		Low power mode	75			
Stack Device Address Configuration						
Threshold of logic "L" of SRN, SRP, ISP, ISN for device address configuration					1.4	V
Threshold of logic "H" of SRN, SRP, ISP, ISN for device address configuration			3.2			V
The pull up current of SRP to internal 5V	I_{SRP}			11		µA
The pull down resistor of ISP, ISN， SRN	$R_{ADDRESS}$			200		kΩ

Note:

5) Guaranteed by design.

TIMMING DIAGRAM



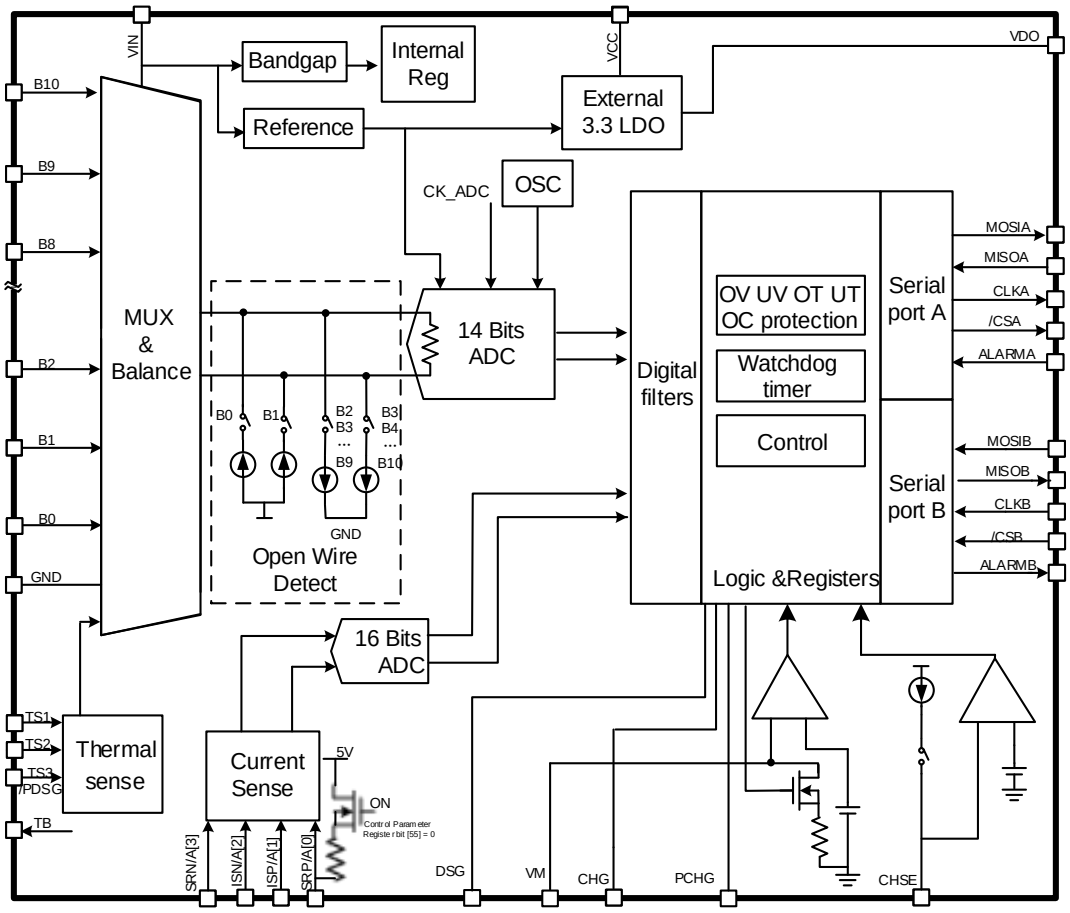
SPI Communication Timing Waveforms

PIN DESCRIPTION

PIN No.	NAME	DESCRIPTION
1	VIN	Maximum Voltage Input. The typical VIN is the same potential as B10.
2	B10	Cell 10 +. Sense voltage for 10th cell positive terminal.
3	B9	Cell 9 +. Sense voltage for 9th cell positive terminal.
4	B8	Cell 8 +. Sense voltage for 8th cell positive terminal.
5	B7	Cell 7 +. Sense voltage for 7th cell positive terminal.
6	B6	Cell 6 +. Sense voltage for 6th cell positive terminal.
7	B5	Cell 5 +. Sense voltage for 5th cell positive terminal.
8	B4	Cell 4 +. Sense voltage for 4th cell positive terminal.
9	B3	Cell 3 +. Sense voltage for 3rd cell positive terminal.
10	B2	Cell 2 +. Sense voltage for 2nd cell positive terminal.
11	B1	Cell 1 +. Sense voltage for 1st cell positive terminal.
12	B0	Cell 1 -. Sense voltage for 1st cell negative terminal.
13	GND	Ground
14	SRN/[A3]	This is a dual-purpose pin. 1) Short detect Negative Input. 2) Device address configuration input for cascade application
15	ISN/[A2]	This is a dual-purpose pin. 1) Negative Current Sense Input. 2) Device address configuration input for cascade application
16	ISP/[A1]	This is a dual-purpose pin. 1) Positive Current Sense Input. 2) Device address configuration input for cascade application
17	SRP/[A0]	This is a dual-purpose pin. 1) Short Detect Positive Input. 2) Device address configuration input for cascade application
18	DSG	Discharge Switch Gate Driver.
19	CHG	Charge Switch Gate Driver.
20	VM	Pin for detecting load connection.
21	CHSE	Pin for charger detection.
22	PCHG	Pre-charge MOSFET Driver.
23	ALARMB	Alarm Output. ALARMB send data to below unit or host processor in the daisy chain.
24	CLKB	Serial Clock Input. CLKB receive data from below unit or host processor in the daisy chain. See serial port in the typical application section.
25	/CSB	Chip Select Input (Active Low). /CSB receives data from below unit or host processor in the daisy chain. See serial port in the typical application section.
26	MISOB	Serial Data Output. MISOB sends data to below unit or host processor in the daisy chain. See serial port in the typical application section.

27	MOSIB	Serial Data Input. MOSIB receives data from below unit or host processor in the daisy chain. See serial port in the typical application section.
28	TS3/PDSG	This is a dual-purpose pin. (1) Thermal Sensor Input 3. The details refer to the TS1 pin. (2) Pre-discharge MOSFET Driver Configuration by MCU
29	TS2	Thermal Sensor Input 2. The details refer to the TS1 pin.
30	TS1	Thermal Sensor Input 1. A simple thermal resistance and resistor combination connected to the TB pin can be used to monitor temperature. The ADC measures the voltage on TS1 pin and stores the result in the registers. Any voltage from 0V to 3.3V referenced to GND can be measured.
31	TB	Thermal bias 3.3V output.
32	VDO	3.3V LDO Output. This pin should be by passed with a 1μF capacitor. The VDO pin is capable of supplying up to 50mA to an external load.
33	VCC	Input source for VDO, MOSFET driver and CHSE.
34	MOSIA	Serial Data Output. The MOSIA pin is an NMOS open drain output, and send data to the above unit in the daisy chain. See serial port in the typical application section.
35	MISOA	Serial Data Input. MISOA receives data from above unit in the daisy chain. See serial port in the typical application section.
36	/CSA	Chip Select Output (Active Low). The /CSA pin is an NMOS open drain output, and send data to the above unit in the daisy chain. See serial port in the typical application section.
37	CLKA	Serial Clock Output. The CLKA pin is an NMOS open drain output, and send data to the above unit in the daisy chain. See serial port in the typical application section.
38	ALARMA	Alarm Input. ALARMA receives data from above unit in the daisy chain. See serial port in the typical application section.

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

JW3371 is a monitor and protection IC capable of measuring the voltage, the temperature and current by an internal 14-bit ΔΣ ADC and 16-bitΔΣ ADC, and integrates complete protection functions including over/under voltage, over/under temperature, over charge / discharge current, short and open wire. Two voltage ADC operation modes are provided to well satisfy multiple different application fields.

JW3371 has two built-in FET drivers, CHG and DSG, which controls NMOS FETs in the charge/discharge loop. Under alarm condition, the FETs could be set to response the alarm condition. Additionally, JW3371 provides passive balance for each battery cell. It is controlled by the host processor. The host processor writes values to configuration register inside the JW3371 to control the switches. And the balance could be disabled by the host processor.

JW3371 communicates with external control unit by a SPI serial interface. Two or more JW3371 can operate in series when the total voltage of battery stack is higher than 50V, or the total quantity of battery cells exceeds 10. JW3371 can pass the data up and down a stack of devices by the external resistor.

Over View of Operation Mode

JW3371 supports three modes of operation: Sleep, Ship, and Normal. Sleep mode is a power saving state where all circuits except the serial interface, LDO and driver are turned off. Ship mode is lowest possible power state, which only charger wakeup and /CSB wakeup circuit is enabled. Normal mode is the full operation state. The three modes key distinctions are shown in the below table.

Figure 1 shows three modes entry and exit conditions.

Normal	Sleep	Ship
Fully operation state. Voltage ADC is on. Over or under voltage protection, over temperature or under temperature is enabled. Current ADC is on and the over current protection and short protection is enabled. All the registers could be configured by host processor	Lower power state. Voltage ADC, current ADC and TB are all off. Mainly Serial Interface, LDO, Driver are on. And low current wakeup and charger wakeup function is active. Short circuit is on. In this state CHG and DSG enable registers can't be set on.	Lowest power state. All circuits are shutdown except charger wakeup and /CSB wakeup function is enabled.

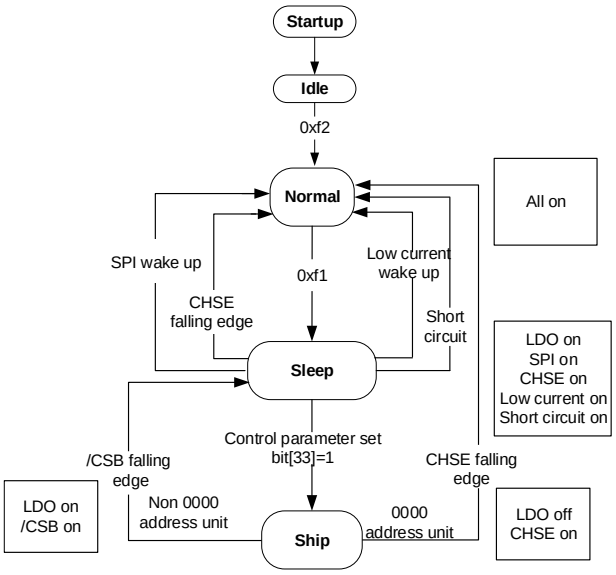


Figure 1. Operation Mode State Diagram

Ship Mode

When 0000 address unit enter ship mode, LDO off, CHSE on. Non 0000 address unit enter ship mode, LDO on, which is used for /CSB wake up.

Ship mode is the lowest power state, which can be used for shipping or long-term storage. For the lower power saving, it may be entry ship mode by the host command. When the device exits ship mode, it will boot and read parameters stored in register (if that has been written). If the register has not been written, the device will power up with default settings, and then settings can be changed by the host writing device registers.

It takes 1s delay to enter ship mode from sleep mode.

- Charger Detection and Wakeup

Charger detection circuit is always on. When a falling edge is detected in CHSE pin, the IC enters to normal mode from ship mode. And the ALARMB pin sends high signal to MCU. It's only applicable to address unit 0000.

- /CSB Wakeup

/CSB wakeup function is always on. When a falling edge is detected in /CSB pin, the IC enters to sleep mode from ship mode. It's only applicable to non 0000 address unit.

Sleep Mode

JW3371 enters or exits Sleep Mode by MCU. In this mode, the CHG and DSG MOSFET status is keep as the previous states and the Low Current Wakeup function could be selected on. Once the charge / discharge current is over the Low Current Wakeup Threshold (V_{LC}) setup by host processor and this status remains for 30ms, JW3371 informs host processor and wakes up itself.

And the Low Current Wakeup operation can be disabled by host processor configuration registers.

- Charger Detection and Wakeup

Charger detection circuit is always on. When a falling edge is detected in CHSE pin, the IC enters to normal mode from ship mode. And the ALARMB pin sends high signal to MCU and wakeup MCU.

- SPI Wakeup

In the sleep mode, SPI circuit is on. MCU could send wakeup command to entry normal mode.

- Low Current Wakeup and Short Circuit Wakeup

In the sleep mode, when the low current or short current is detected, the IC enters to normal mode from sleep mode, and the ALARMB pin sends high signal to MCU.

Normal Mode

Normal mode represents the fully operation mode where all blocks are enabled and the device sees its highest current consumption.

JW3371 can monitor each cell voltages for over voltage and under voltage conditions. Internal 14-bit ΔΣ ADC enables high-accuracy measuring for battery voltage and temperature. Two 1k resistors and a 22nF capacitor are recommended to make up the front differential filtering network, which are enough for filtering transient voltage spikes. When the IC starts up, it's in sleep mode. And then enters normal mode through the MCU configuration. Figure 2 simply shows the MCU task.

It should be noted before "system control set", "voltage set", "current set", MCU should send "clear interrupt" command to clear bit [23-20] in "current ADC read". After sending "system control set", "voltage set", "current set" command, if the command pass CRC verification i.e. command successfully send from MCU to AFE, the [23-20] bit will all set. Any bit of 0 indicates this command is not sent successfully. So, the command should sent again.

Besides, after AFE wakeup successfully, the bit [4] of "Detail Alarm Info. Get" should clear. If this bit is still 1, it indicates AFE is still in sleep mode. Then wakeup command should send again.

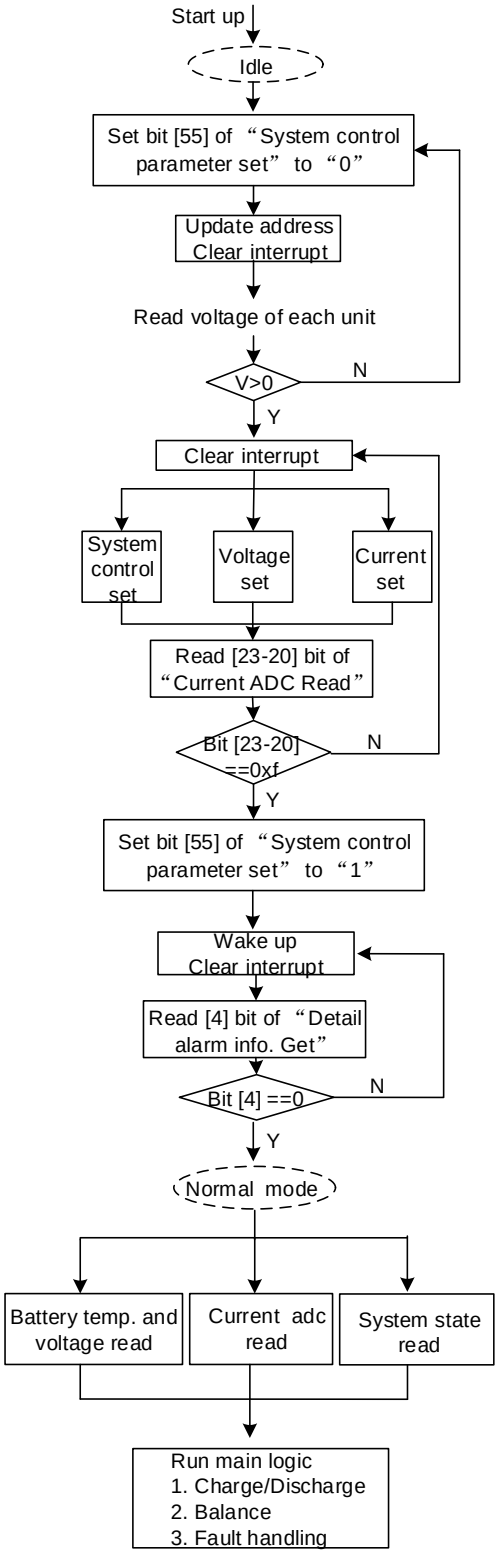


Figure2. Task Handling Flow Chat

JW3371 can typically be used with as few as four cells, which is guaranteed by the low enough VIN start-up voltage. When JW3371 is used to

monitor less than 10 cells, 8 cells for example, B0~B2 pins are all shorted and the above B2~B10 pins are connected to the monitored cells. The unused inputs could result in a 0V reading for those channels. Figure 3 shows the example of JW3371 when used to monitor 8 cells.

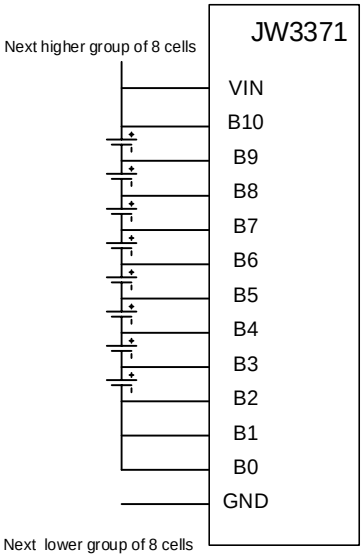


Figure 3. Monitoring 8 Cells with JW3371

In the normal case, the ADC senses the 10 voltage channels circularly, the 3 thermal channels are sensed after 10 times voltage sensing. The ADC can be commanded to measure any individual channel by host processor.

Considering the accuracy of ADC measurement, it is recommended to wait for 100ms delay before measures cell voltages and temperatures when waking from sleep mode to normal mode.

Monitor

The monitoring subsystem ensures that all cell voltages, temperatures, and pack current easily measured by the host. All ADCs are trimmed by Joulwatt.

JW3371 has a fully digital interface: All information is transferred through SPI, simply by reading or writing to the appropriate register(s) storing the relevant data. Block reads and writes, buffered by an 8-bit CRC code per byte, ensure a fast and robust transmission of data.

Cell Voltage Measurement

Each JW3371 measures cell voltages and temperatures using a 14-bit ADC. This ADC measures all differential cell voltages, thermistors with a nominal full-scale unsigned range of 0–5.0 V and LSB of 0.305mV. It should be noted ***control parameter set [41] bit*** should set 0 and ***voltage parameter set [58] bit*** should set 1 to ensure voltage sampling accuracy.

The ADC is on automatically whenever the device enters normal mode. Once ADC is on and the protection thresholds are set, the integrated OV, UV, battery temperature and over current protections are functional.

Each cell measured time is about 0.64ms and a complete update is available every 6.4ms.

Each differential cell input is factory-trimmed for gain and offset, except that the first cell requires the host processor to add 2.5mV offset in case of any cell number configuration. The cell voltage measurement accuracy is ±3mV typ.@2.3V~4.3V, T_A=25ºC.

The ADC transfer function is a linear equation defined as follows:

$$V_{CELL}(\mathrm{V}) = ADC_{CELL} * GAIN$$

ADC_{CELL} is the measurement results of each cell.

GAIN is fixed 0.305mV/LSB.

An example cell voltage calculation is provided in the table below.

14bit ADC Result	ADC Result in Decimal	GAIN (mV/LSB).	Cell Voltage(mV)

0x92e	2350	0.305	717

Cell Temperature Measurement

Cell temperature and voltage monitor use same ADC. To convert the thermistor resistance into temperature, please refer to the thermistor component manufacturer's datasheet.

Note: In JW3370 cascaded application, for Ts1~3 sampling, the /CSB should drive low for 103 VADC sampling cycles firstly, then send ***"Voltage ADC Read" command*** by MOSIB & CLKB and receive data and MISOB pin. And Ts value should add 18mV for offset compensation.

Pack Current Measurement

A 16bit integrating ADC, commonly referred to as the coulomb counter provides measurements of accumulated charge across the current sense resistor.

The current ADC is always on and the integration period for this reading is 132ms.

The full scale range of the CC is ±190 mV, with a max recommended input range of ±190 mV, thus yielding an LSB of approximately 6 µV.

The following equation shows how to convert the 16-bit current ADC reading into an analog voltage:

$$V_{ISP-ISN}(mv) = ADC_{CURR} * GAIN - 200$$

ADC_{CURR} *is the measurement results of current sense.* GAIN is fixed 0.0061mV/LSB.

An example cell voltage calculation is provided in the table below.

16bit ADC Result	ADC Result in Decimal	GAIN (mV/LSB).	$V_{ISP-ISN}$ (mV)
0x1e82	7810	0.0061	-152.33

Protection

Over/Under Voltage Protection

The JW3371 monitor each cell voltage. If one cell voltage is over the Over Voltage Threshold (V_{OVP}) or under the Under Voltage Threshold (V_{UVP}) and this status lasts for an adjustable delay time, JW3371 turns off charge MOSFET or discharge MOSFET and sends alarm signal to inform host processor.

If fewer than 10 cells are connected to the JW3371 then it is necessary to set the useful series battery numbers by configuration registers. If the number is set to 8, then the input for cells 1 and 2 are automatically masked.

Over/Under Temperature Protection

JW3371 provides 3 temperature sensing PINs for detecting the temperature of battery cells. A NTC resistor is placed nearby battery cells. When the temperature of battery cells increases, the divided voltage input to TS pin is increases. Once the battery temperature is over the Over Temperature Threshold (T_{OTP}) or under the Under Temperature Threshold (T_{UTP}) and this status lasts for an adjustable delay time, JW3371 turns off charge MOSFET or discharge MOSFET and sends alarm signal to inform host processor. Sensors can be powered directly from TB as shown in Figure 4.

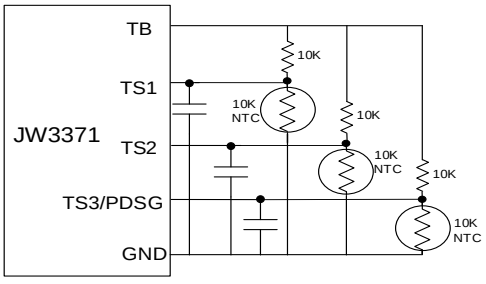


Figure 4. Driving Thermistors Directly from TB

If only one temperature sensing channel is used, it is strongly recommended to use the connection method shown in Figure 5.

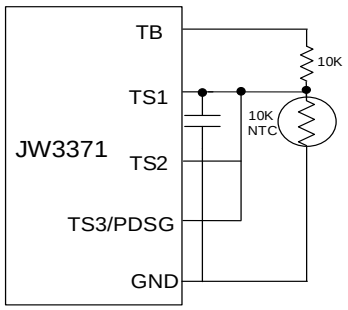


Figure 5. Single channel temperature sensing

The T_{OTP} / T_{UTP} and delay time can be setup by configuration registers. For charging process, the T_{OTP} / T_{UTP} is recommended to be set as 45ºC / 0ºC. For discharging process, the T_{OTP} is recommended to be set as 65ºC or 75ºC and the T_{UTP} -10ºC or -20ºC. The OTP / UTP delay time can be chosen from 0~7.68s (512ms step).

TS3/PDSG can be selected through register configuration. In Voltage parameter set, set bit [59] to 1 to enable TS3 temperature sensing. The default power up of the IC is PDSG.

Charge Over Current Protection

If the battery current is over Charge Current Threshold (V_{COI}) and remains for a delay time, JW3371 shuts down the CHG and DSG.

Discharge Over Current Protection

If the battery current is over Discharge Current Threshold (V_{DOI}) and remains for a delay time, JW3371 shuts down the DSG.

Load Short Protection

If the voltage of external sense resistor (R_{sense}) is over Short Threshold (V_{OS}) and remains for a delay time, JW3371 shuts down the DSG.

The V_{OS} and the delay time can be setup by host processor. The delay time can be chosen from 0~2.048ms (64µs step).

Cell Open Wire Detection

When a cell voltage sensing wire is open, the measurement results of the two cells close to the open cell are affected.

JW3371 provides two pull-down current sources for the open wire detection of B2 to B10 and two pull-up current sources for the open wire detection of B0 and B1. If a cell input pin is floating due to an open wire condition, this current discharges the capacitance, causing the voltage at the pin to slowly drop. This drop in voltage eventually triggers a protection fault on that particular cell and the cell above it.

Take B9 open connection for example, after several cycles of measuring battery cell9 and cell10, the current source is engaged, the potential at B9 is pulled down. The ADC reading for cell9 could approach zero and reading cell10 approach full scale. The measurement result of cell9 and cell10 different from the previous cycle measurement result over 200mV, the JW3371 will send open wire signal to host processor. MCU is needed in the open wire detection of B0 and B10 by monitoring the voltage of cell 1 and cell 10. The under voltage protection of cell 1 or cell 10 triggered after open wire detection equals to the open wire of B0 or B10.

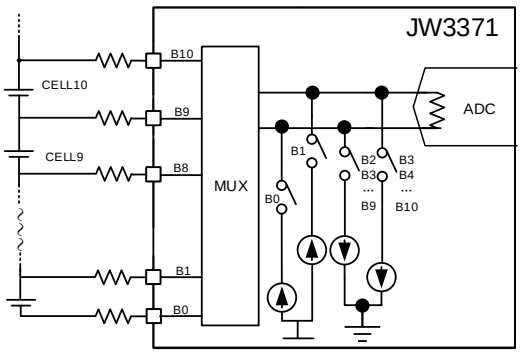


Figure 6. Open Connection

The Cell Open Wire Detection is executed when the MCU command is enable. Periodic open wire detection is recommended.

Notice：

1. When the single cell voltage lower than 1.5V, the open-wire fault statue maybe submitted.

2. The B0 and B10 open-wire detection should be handled by MCU.

3. When open-wire fault happened will trigger over-voltage or under-voltage protection and turn off CHG or DSG MOSFET.

Control Subsystem

Charge/Discharge Switch MOSFET

JW3371 can drive two external N-MOSFETs to control the charge / discharge loop. When Charge Switch MOSFET (CHG) is shut down, the charge current of battery stack is cut off; and when Discharge Switch MOSFET (DSG) is shut down, the discharge current is cut off.

Figure 7 shows the CHG and DSG FET circuit. The highest driving voltage of CHG and DSG is 12V and the falling time of DSG is about 100ns with 95mA sinking current and 1nF load capacitor.

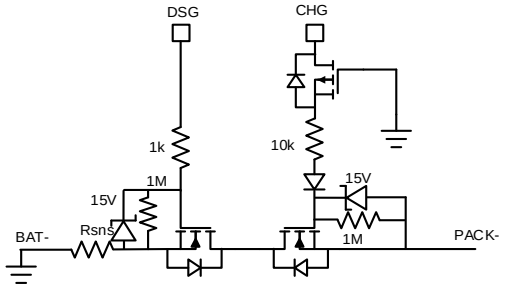


Figure 7. CHG and DSG FET Circuit

ALARM

The ALARMB pin serves as an active high digital interrupt signal that can be connected to a GPIO port of the host microcontroller. This signal is an OR of all bits in the system state register. Most of the states are fault events. The faults and the FET state is shown in the table below.

System States	Interrupt Inform	ALARM	Control CHG or DSG	
			CHG	DSG
Charge mode: over voltage, over/under Temp	Yes	Yes	OFF	ON
Discharge mode: under voltage, over/under Temp, over current, short current	Yes	Yes	ON	OFF
Charge over current, ALARM pin open wire	Yes	Yes	OFF	OFF
Cell Open Wire	No	No	No	
Balance ON/OFF	Yes	No	No	
Load Present	Yes	No	No	
TB OTP	Yes	Yes	No	
LDO OTP	Yes	Yes	No	
Low current wakeup	Yes	Yes	No	
charger wakeup	Yes	Yes	No	

In order to clear the ALARMB signal, the source bit in the system state register must first be cleared by “clear interrupt flag” instruction.

Some fault event triggers automatic disabling of both CHG and DSG FET drivers. And recovery from a fault event must be handled by the host microcontroller.

In cascaded mode application, when there is no fault, the ALARB of non 0000 address chip sends out pulse signal with high level time of 4ms and cycle of 8s as the detection and judgment of alarm open wire enable. When a non 0000 address enter failure mode, its ALARMB sends out a pulse signal. There are three types of pulse signals correspond to three types of faults.

1. Pulse signal with high level time of 5-14ms and cycle of 100ms, turn off CHG FET.

2. Pulse signal with high level time of 15-25ms and cycle of 100ms, turn off DSG FET.

3. Pulse signal with high level time of 30-50ms and cycle of 100ms, turn off CHG FET and DSG FET.

The ALARMB State is shown in the Figure 8.

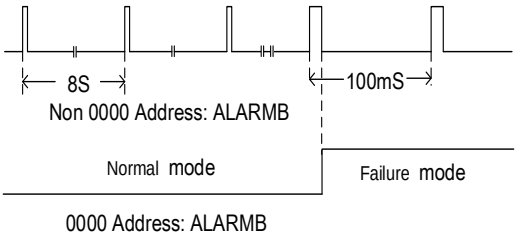


Figure 8. ALARMB State

Pre-Charge and Pre-Discharge Function

JW3371 integrated pre-charge and pre-discharge drivers for the deep discharge battery or some big capacitor load startup.

The pre-discharge function needs configuration by CPU which is not compatible with thermal sense function.

Passive Balance

JW3371 allows host processor choosing the battery cells to be discharged. When a cell is selected, an internal discharging MOSFET is turned on, which also turns on an external balancing Bipolar to largely increase the discharging current. An external resistor of 47Ω recommended to limit the power dissipated by the external Bipolar.

The balancing operation is turned off when any condition below is happening:

1.Communication with the host processor is interrupt for watchdog timer (t_{WD});

2.Battery under voltage protection;

3.The temperature of JW3371 is beyond T_{BALAN}.

The balancing circuitry will not release after under voltage protection clear away. However, it's released if both of the following conditions are satisfied:

1.Resume communication with the host processor;

2. The temperature of JW3371 returns to T_{BALAN_HYST} or even lower.

The detailed circuit is shown in the Figure 9.

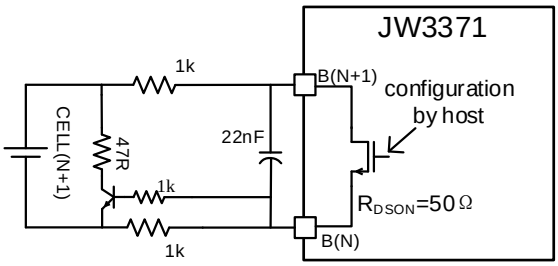


Figure 9. External Discharge Circuit Connection

(One cell)

The following equation shows how to calculate the balance current.

$$I_{BAL}(A) = MIN(\frac{V_{CELL}(V)}{R_{BAL}(\Omega)}, \beta I_b) + \frac{V_{CELL}(V)}{R_{DSON}(\Omega) + 1k\Omega + 1k\Omega}$$

JW3371 allows at most 3 consecutive cells being discharged simultaneously. If host processor chooses 4 or more consecutive cells, the discharging switches of the lowest cell of each 4 cells will be prohibited turning on.

Considering the accuracy of ADC measurement, while a cell is being measured, the discharge switches for this cell and the cell above and below are all disabled. The harshest conditions are listed below when all cells discharge simultaneously.

Mode	1	2	3	4	5	6	7	8	9	10
1	S	F	F	F	F	F	D	D	D	F
2	F	S	F	D	D	D	F	D	D	D

3	D	F	S	F	D	D	D	F	D	D
4	D	D	F	S	F	D	D	D	F	D
5	D	D	D	F	S	F	D	D	D	F
6	F	D	D	D	F	S	F	D	D	D
7	D	F	F	F	F	F	S	F	D	D
8	D	D	D	D	D	D	F	S	F	D
9	D	D	D	D	D	D	D	F	S	F
10	F	D	D	D	D	D	D	D	F	S

S-Sample: the cell is being measured

D-Discharge: internal discharging MOSFET is turned on

F-OFF: internal discharging MOSFET is turned off

Load State Detection

The VM pin is for load state detection. The comparison result of VM voltage and V_{VM} is used as a condition of interrupt releasing. In the normal status, the internal resistance (R_{VMS}) between the VM pin and GND pin are not connected. When the over-discharge or discharge over current status occurs, CPU sends commend to enable load detection circuit. R_{VMS} are connected until the status is released.

LDO

JW3371 provides 3.3V LDO for external application. The current limitation of LDO output is 100mA.

JW3371 provides two-step over-temperature protection for LDO. When the temperature detected reaches 125ºC, JW3371 could warn host processor. If the temperature exceeds 150ºC, LDO could be shut down.

Power

LDO/driver module power supply is VCC. PCHG/PDCHG/CHSE pull-up, power supply is VCC, others power supply is VIN.

SPI Communication

JW3371 provides two groups of SPI data interface. MISOB is used for sending data to lower unit or host processor; MOSIB, /CSB and CLKB are used for receiving data from lower unit or host processor; MISOA is used for receiving data from upper unit; MOSIA, /CSA and CLKA are used for sending data to upper unit. A 1k resistor must be connected in series between communication pins of the cascade units. Also, external pull-up for MOSIB, /CSB, CLKB through a 10k resistor and a 5V zener is connected in parallel. It is used for updating address while the cascade unit communication loss occurred. When this happens, the baud rate needs to be reduced to 1 / 10 of the original.

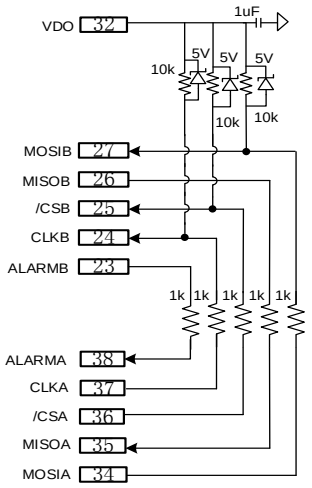


Figure 10. SPI Communication in Cascade Application

Host processor writes values to configuration registers inside JW3371 to setup the protection thresholds, delay time and control switches, which facilitates users to make settings and choose operating mode freely. The watchdog timer on the JW3371 will turn off the balancing circuitry if communication with the host processor is interrupt for watchdog timer (t_{WD}, 0~2min, 512ms step). The balancing circuitry will release when any command setup is successful.

Clock Phase and Polarity: JW3371 SPI compatible interface is configured to operate in a system using CPHA=1 and CPOL=1. Consequently, data on MOSIB must be stable during the rising edge of CLKB and while stop communication, MCU needs to pull high the input pins MOSIB, CLKB and /CSB.

Data Transfers: Every byte consists of 8 bits. On a write, the data value on MOSIB is latched into the device on the rising edge of CLKB (Figure11). Similarly, on a read, the data value output on MISOB is valid during the rising edge of CLKB. /CSB must remain low for the entire duration of a command sequence, including between a command byte and subsequent data.

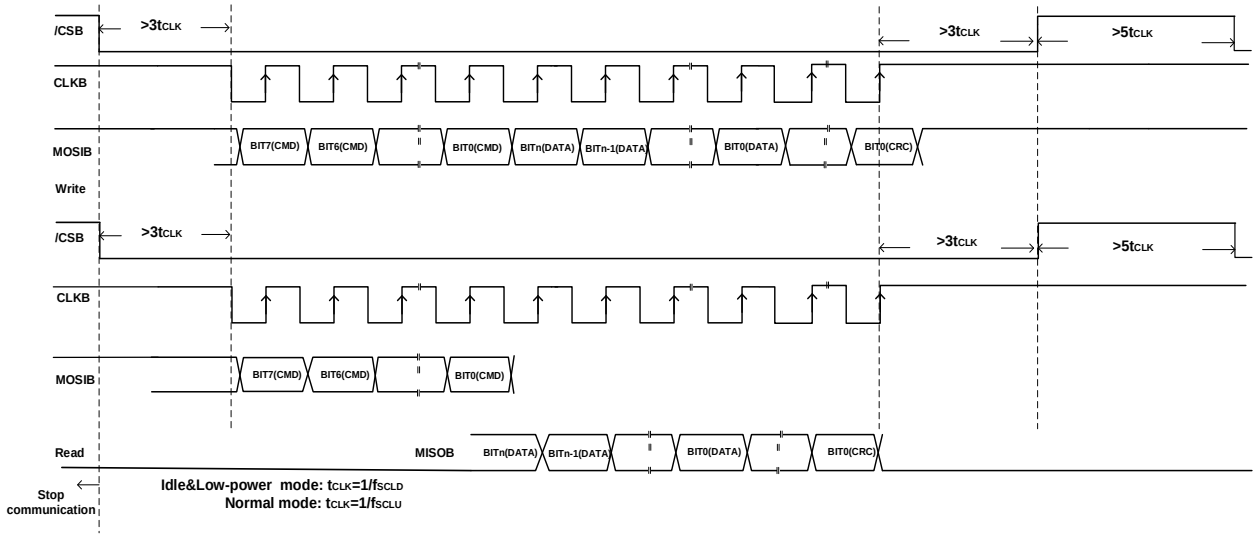


Figure11. Transmission Format

Random Cell Connection Support

The JW3371 device supports a random connection sequence of cells to the device during pack manufacturing unless the battery negative terminal connected to Power GND of the JW3371 device first.

For example, cell-8 in a 10-cell stack might be first connected at the input terminals leading to pins B8 and B7, then cell-4 may next be connected at the input terminals leading to pins B4 and B3, and so on. It is not necessary to connect the negative terminal of cell-1 first at B0. As another example, consider a battery stack that is already assembled and cells already interconnected to each other, then the stack is connected to the PCB through a connector, which is plugged or soldered to the PCB. In this case, the sequence order in which the connections are made to the PCB can be random in time, they do not need to be controlled in a certain sequence.

Cascade Configuration

JW3371 supports cascade application. Several devices can be daisy chained in series.

Configure device address by the logic levels on the SRN/[A3], ISN/[A2], ISP/[A1], SRP/[A0] pins, as shown in below table.

SRN /[A3]	ISN /[A2]	ISP /[A1]	SRP /[A0]	Device Address
0	0	0	0	1
0	0	0	1	2
0	0	1	0	3
0	0	1	1	4
0	1	0	0	5
0	1	0	1	6
0	1	1	0	7
0	1	1	1	8

1	0	0	0	9
1	0	0	1	10
1	0	1	0	11
1	0	1	1	12
1	1	0	0	13
1	1	0	1	14
1	1	1	0	15
1	1	1	1	Broadcast

Note:

6) SRP/[A0] is pull up to the 5V by default. The updating address instruction must be written while SRP/[A0] is pull up to the 5V. So update the address first after power on, voltage measured of all cascade units is greater than 0 indicates the address is correct, then remove the internal pull up by set control parameter register bit [55] to 1. This bit set to 1 will remove the function of updating address, and enable ADC, small current wake up and ship mode entry.

SPI Power Consumption in Cascade Application

The power consumption of SPI communication occurs when /CSB, MOSIB and CLKB pins are pulled down and MISOB pin is pulled up. The maximum power consumption can be estimated as the sum of sampling power consumption of voltage and current.

$$I_u = I_{SINKA} * 28 * 8 * \frac{\left(1 + 0.5 + \frac{I_{SOURCEB}}{I_{SINKA}} * 0.5\right)}{f_{clku} * T_{sample-v}}$$

$$I_i = I_{SINKA} * 5 * 8 * \frac{\left(1 + 0.5 + \frac{I_{SOURCEB}}{I_{SINKA}} * 0.5\right)}{f_{clku} * T_{sample-i}}$$

The recommended sampling period: $T_{sample-v}$=500ms.

The recommended sampling period: $T_{sample-i}$=200ms.

PCB Layout Precaution

The PCB layout of JW3371 must be carefully designed.

1. The TB and VDO pins should be bypassed with a 0.1μF and 1μF capacitor respectively.
2. Care should be taken when placing the ADC input filter capacitors to minimize PCB trace impedances.
3. The quality of the Kelvin connections at the sense resistor is critical. The sense resistor must have a temperature coefficient no greater than 50 ppm in order to minimize current measurement drift with temperature. Choose the value of the sense resistor to correspond to the available overcurrent and short circuit ranges of the JW3371 device. Parallel resistors can be used as long as good Kelvin sensing is ensured.
4. The JW3371 device uses an integrating delta-sigma ADC for current measurements. For best performance, 100Ω resistors should be included from the sense resistor terminals to the SRP and SRN inputs of the device, with a 10nF filter capacitor placed across the SRP and SRN pins. All filter components should be placed as close as possible to the device, rather than close to the sense resistor, and the traces from the sense resistor routed in parallel to the filter circuit. A ground plane can also be included around the filter network to add additional noise immunity.

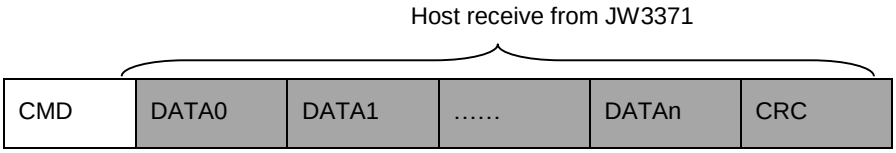
THE DETAILS FOR HOST PROCESSOR COMMAND REGISTERS

Instruction Structure

Write:

CMD	DATA0	DATA1	……	DATAn	CRC

Read:



Note:

1. The command is effective, when “DATA0+DATA1+…+DATAn+CRC=0xff” is setup.

CMD Structure

A3	A2	A1	A0	C2	C1	C0	ODD

Note:

1. A[3:0]: Configure the address to determine the useful IC except “A[3:0]≠1111”. If “A[3:0]=1111” is set, the command is effective to all the stacked devices (Broadcast State).
2. C[2:0]: Commands set. Reference table 1 for the detail.
3. ODD: Odd check bit, ^{A[3:0], C[2:0], ODD}=1.

Table 1. CMD Instructions

C[2:0]	B/S	Function	R/W	Data description
000	B	Power down	W	All chips into sleep mode
	S	Clear interrupt flag	W	Clear the interrupt fault flag bit set to 1 due to various faults
001	B	Power wake up	W	All chips into normal mode
	S	Balance set	W	Set battery balancing related registers
		Alarm set	W	Set alarm related registers
010	B	Set state to charge	W	Effective to all stacked units except the bottom one
	S	Voltage ADC read	R	Read 14 bit data of 10 battery voltages and 3 battery temperatures
011	B	Set state to discharge	W	Effective to all stacked units except the bottom one
	S	Current ADC read	R	Read 16bit data of current
100	B	Update device address	W	Through {SRN,SRP,ISN,ISP} configure device address *The device address updates when the IC is power-on or the command is active

	S	Current parameter set	R	Set charge discharge over-current threshold ,short-circuit protection threshold , delay time and small current detection threshold
101	B	Alarm & Cell open-wire info get	R	Read the alarm and battery status of all cascaded chips
	S	Detail alarm info get	R	Read the detailed fault interrupt flag bit of a chip
110	B/S	Control parameter set	W	Set control related registers
111	B/S	Voltage parameter set	R	Set the over / under voltage (temperature) threshold and delay time

Note:

B: Broadcast command: A broadcast command is one to which all devices on the bus will respond, regardless of device address.

S: Sing command: effective to specified device.

R: read.

W: write.

Table 2. Single Byte Instructions

Item	Content	Description
Power Down	0xf1	
Power Wakeup	0xf2	
Set state to charge	0xf4	
Set state to discharge	0xf7	
Update device address	0xf8	the command is effective when bit [55] of “**System control parameter set”** is set to “0”
Clear interrupt flag	xxxx_000x	0x01, 10, 20, 31, 40, 50, 51, 0x01: unit1; 0x20: unit2 of the cascade; 0x31: unit3 of the cascade; ...

Table 3. Alarm & Open-wire Info Get

Item	Content	Description
CMD(1B)		0xfb
DATA(4B)	[31:16]	Read ALARM interrupt flag of 16 stacked devices
	[15:0]	Read cell open wire flag of 16 stacked devices

Table 4. Detail Alarm Info. Get

Item	Content	Description
CMD(1B)		0x0b, 0x1a, 0x2a, 0x3b… 0x0b: unit1; 0x1a: unit2 of the cascade; 0x3b: unit3 of the cascade;

		…
DATA(9B)	[71:62]	Read over voltage interrupt flag of 10 cells, bit [71] corresponds to the 10th battery
	[61:58]	Reserved
	[57:48]	Read under voltage interrupt flag of 10 cells, bit [57] corresponds to the 10th battery
	[47:44]	Reserved
	[43:41]	Read over temperature interrupt flag of 3 channels bit [41]: TS1 over temperature bit [42]: TS2 over temperature bit [43]: TS3 over temperature
	[40]	Reserved
	[39:37]	Read under temperature interrupt flag of 3 channels bit [37]: TS1 over temperature bit [38]: TS2 over temperature bit [39]: TS3 over temperature
	[36]	Reserved
	[35]	Read over current interrupt flag in charge state
	[34]	Turn off DCHG FET for upper chip instruction
	[33]	Turn off CHG FET for upper chip instruction
	[32:31]	Read over current interrupt flag in discharge state, bit [32] correspond to two grades protection
	[30]	Reserved
	[29]	Reserved
	[28]	Read short circuit interrupt flag in discharge state
	[27:18]	Read open wire interrupt flag, which corresponds to 10 cells，bit[27] corresponds to the 10th battery.
	[17]	Open wire detection completion flag indicates the bit, which can be cleared only when the open wire detection enable is turned off
	[16]	Wake up event flag bit except wake up sleep state with command
	[15]	DCHG FET mode
	[14]	CHG FET mode
	[13]	Read over temperature interrupt flag of 3.3V TB subsystem
	[12]	Read over temperature interrupt flag of 3.3V LDO subsystem
	[11]	Read over temperature interrupt flag of balance subsystem
	[10]	Read the status of VM pin. 0: Load connected 1: Load removed
	[9]	Read stacked devices open wire interrupt
	[8]	Reserved
	[7]	Reserved

	[6]	Read the status of balance on-off. If the balance is disabled, the bit [6] is “1”, else, the bit [6] is “0”.
	[5]	Battery charge and discharge state, if bit [5] is 1, it is charged
	[4]	When the chip sleep status indicator bit [4] is 1, the chip is in sleep state
	[3]	Reserved
	[2]	The chip detects the result indicator bit of charger comparator If the charger is removed, bit [2] is 1
	[1:0]	Reserved
CRC(1B)		∑(DATA,CRC) = 0xff

Table 5. Voltage ADC Read

Item	Content	Description
CMD(1B)		0x04, 0x15, 0x25, 0x34…
DATA(26B)	B25B24	The ADC measurement results of cells 1 {B25[5:0],B24[7:0]}→cell1
	B23B22B21B20	The ADC measurement results of cells 2 and 3 {B23[5:0],B22[7:0]}→cell2 {B21[5:0],B20[7:0]}→cell3
	B19B18B17B16	The ADC measurement results of cells 4 and 5
	B15 B14B13B12	The ADC measurement results of cells 6 and 7
	B11B10B9B8	The ADC measurement results of cells 8 and 9
	B7B6B5B4	The ADC measurement results of cells 10 and battery temperature channel 1
	B3B2B1B0	The ADC measurement results of battery temperature channel 2 and 3
CRC(1B)		∑(DATA,CRC) = 0xff

Table 6. Current ADC Read

Item	Content	Description
CMD(1B)		0x07, 0x16, 0x26, 0x37…
DATA(3B)	[23]	Current parameter set OK flag
	[22]	Voltage parameter set OK flag
	[21]	Control parameter set OK flag
	[20]	Balance/Test/Alarm/Trim set OK flag
	[19:16]	Reserved
	[15:0]	The ADC measurement result of charge/discharge current
CRC(1B)		∑(DATA,CRC) = 0xff

Table 7. Balance/ Alarm/ System Control Set

Item	Content	Default	Recommended	Description

CMD(1B)	xxxx_001x					0x02, 0x13, 0x23, 0x32…
DATA(3B)	[23:21]	000 Balance set	[20:10]	0x0	0x0	Reserved
			[9:0]	0x0	0x0	Selection of cell for balancing bit[0]→cell 1,bit[9]→cell 10 1: cell balance selected 0: cell balance not selected At most three consecutive batteries are allowed to discharge simultaneously. When ADC samples a certain battery voltage, the battery voltage and its upper and lower batteries do not discharge
		010 Alarm set	[20:13]	0x0	0x0	Reserved
			[12]	0x0	0x0	Force to 0
			[11]	0x1	0x1	Alarm open wire detection: 1: alarm open wire detection is invalid 0: under normal state, the cycle of Alarmb is 8s, and the pulse width of high level is 4ms. If the low level of Alarma lasting more than 16s(MAX) is detected, the line is open
			[10:0]	0x0	0x0	Reserved
		100 System control	[20:16]	0x0	0x0	Reserved
			[15]	0x0	0x0	Analog module charger detection 0：enable 1：disable
			[14]	0x0	0x0	Analog module short circuit comparator 0：enable 1：disable
			[13]	0x0	0x0	Small current detection 0：enable 1：disable
			[12]	0x0	0x0	Analog module chip address control 0：enable 1：disable
			[11:10]	0x0	0x0	Reserved
			[9]	0x0	0x0	PDSG output control (works when Ts3 temperature protection is disabled) 0：output 0V 1：output 5V
			[8]	0x0	0x0	PCHG output control 0：output 0V 1：output 5V

			[7]	0x0	0x0	Reserved
			[6]	0x0	0x0	Setting of pull-up current during charger detection 0: 1μA 1: 0.5μA
			[5]	0x0	0x0	VM load detection module enable control 0：disable 1：enable
			[4]	0x0	0x0	Reserved
			[3]	0x0	0x0	Enable CHG 0:disable 1:enable
			[2]	0x0	0x0	CHG status 0:low,0V 1:high,12V * the command is effective when bit [3] is set to “1”
			[1]	0x0	0x0	Enable DISCHG 0:disable 1:enable
			[0]	0x0	0x0	DISCHG status 0:low,0V 1:high,12V * the command is effective when bit [1] is set to “1”
CRC(1B)						∑(DATA,CRC) = 0xff

Table 8. Control Parameter Set

Item	Content	Default	Recommended	Description
CMD(1B)				Broadcast: 0xfd; Single: 0x0d, 0x1c, 0x2c, 0x3d…
DATA(8B)	[63]	0x0	0x0	Forced to 0
	[62:58]	0x0	0x0	Reserved
	[57]	0x0	0x0	Send control bit of alarm pin to close the CO / DO tube function 0: allow alarm pin to turn off the sending of CO / DO. 1: Disable alarm pin from sending CO / DO.
	[56]	0x0	0x0	Detect the control bit of alarm pin closing CO / DO tube function 0: allow alarm pin to turn off CO / DO detection. 1: Disable alarm pin to turn off CO / DO detection, and clear the corresponding status detection bit.
	[55]	0x0	0x1	0: Update address, update the address first after power on, voltage measured of all cascade units is greater than 0 indicates the address is correct. 1: Forced to 1 after updating address successful, because only when this bit is 1, the voltage ADC measurement can work normally
	[54:52]	0x2	0x2	Forced to 2
	[51:49]	0x2	0x2	Forced to 2

	[48:46]	0x0	0x0	Forced to 0
	[45:44]	0x2	0x2	Forced to 2
	[43]	0x0	0x0	SPI /CSB wake up ship state 0: /CSB is low and cannot wake up; 1: /CSB is low and can wake up, enter sleep state;
	[42:40]	0x0	0x0	Forced to 0
	[39:36]	0x0	User-defined	Chip cascade number: [39:36]+1 The default value is 0, single chip works
	[35]	0x0	0x0	Enable 3.3V TB operation 0: enable(Recommended) 1: disable
	[34]	0x0	0x0	Enable 3.3V LDO operation 0: enable (Recommended) 1: disable
	[33]	0x0	0x0	0: It is forbidden to enter ship mode in sleep mode 1: ship mode is allowed in sleep mode
	[32]	0x0	0x0	Forced to 0
	[31:24]	0x78	0x78	Set the watchdog time(t_{WD}) of SPI communication; when no SPI communication state lasts for [31:24] * 512ms, if the balancing is on, the balancing will be turned off; if any SPI instruction is sent, it will recover
	[23:22]	0x0	0x0	Forced to 0
	[21]	0x0	0x0	Poll Voltage ADC converter control 0: poll status 1: appointed ADC only
	[20:16]	0x0	0x0	Select respective cell measurement (from cell1 to cell10, TP1 to TP3) 0x00→cell1, 0x01→cell2, …, 0x09→cell10 0x0E→TP1, 0x0F→TP2, 0x11→TP3 * respective cell voltage ADC measured data with bit [21] set to 1
	[15:12]	0x1	0x1	Forced to 1
	[11]	0x0	0x0	In sleep mode and the digital system clock is turn off, whether to turn on SPI communication timeout detection 0: disable SPI communication timeout detection, but the communication flag will not be cleared 1: Allow SPI communication timeout detection
	[10:7]	0x0	0x3	Forced to 3
	[6:4]	0x7	0x7	Forced to 7
	[3:0]	0x9	User-defined	Set the number of batteries =[3:0]+1
CRC(1B)				∑(DATA,CRC) = 0xff

Table 9. Voltage Parameter Set

<table>
<tr><th>Item</th><th>Content</th><th>Default</th><th>Recommended</th><th>Description</th></tr>
<tr><td>CMD(1B)</td><td></td><td></td><td></td><td>Broadcast: 0xfe; Single: 0x0e, 0x1f, 0x2f, 0x3e…</td></tr>
<tr><td rowspan="16">DATA(10B)</td><td>[79:72]</td><td>0xff</td><td>User-defined</td><td>Setting discharge under temperature protection threshold：
([79:72]+1)*64*5/16384</td></tr>
<tr><td>[71:64]</td><td>0x0</td><td>User-defined</td><td>Setting discharge over temperature protection threshold：
([79:72]+1)*64*5/16384</td></tr>
<tr><td>[63]</td><td>0x0</td><td>0x0</td><td>Reserved</td></tr>
<tr><td>[62]</td><td>0x0</td><td>0x0</td><td>Time step of overvoltage protection：
0 : 128ms 1 : 512ms</td></tr>
<tr><td>[61]</td><td>0x0</td><td>0x0</td><td>Reserved</td></tr>
<tr><td>[60]</td><td>0x0</td><td>0x0</td><td>Time step of under voltage protection：
0 : 512ms 1 : 1024ms</td></tr>
<tr><td>[59]</td><td>0x0</td><td>0x0</td><td>0: TS3 is forbidden to detect over and under temperature.
1: TS3 is allowed to detect over and under temperature.</td></tr>
<tr><td>[58]</td><td>0x0</td><td>0x1</td><td>Forced to 1</td></tr>
<tr><td>[57]</td><td>0x0</td><td>0x0</td><td>Forced to 0</td></tr>
<tr><td>[56]</td><td>0x0</td><td>0x0</td><td>Open wire detection enable of voltage ADC sampling line
0: the open wire detection function is disabled;
1: the open wire detection function is enabled
The next open wire detection must disable before enable.</td></tr>
<tr><td>[55:54]</td><td>0x0</td><td>0x0</td><td>Forced to 0</td></tr>
<tr><td>[53:52]</td><td>0x1</td><td>0x1</td><td>Forced to 1</td></tr>
<tr><td>[51]</td><td>0x0</td><td>0x0</td><td>Voltage ADC measurement mode
0: fast mode (Recommended)
1: filtering mode
* The processing time of fast mode is determined by bit[50:48] setting
The processing time of filtering mode is 65ms</td></tr>
<tr><td>[50]</td><td>0x1</td><td>0x1</td><td>Voltage ADC measurement handing
1: The processing time is determined by bit[49:48] setting
0: The processing time of “simple count” is 16.8ms</td></tr>
<tr><td>[49:48]</td><td>0x0</td><td>User-defined</td><td>Setting waiting and sampling time
<table>
<tr><th>[49:48]</th><th>waiting time</th><th>sampling time</th></tr>
<tr><td>00</td><td>128μS</td><td>512μS</td></tr>
<tr><td>01</td><td>256μS</td><td>512μS</td></tr>
<tr><td>10</td><td>256μS</td><td>1024μS</td></tr>
<tr><td>11</td><td>1024μS</td><td>1024μS</td></tr>
</table></td></tr>
<tr><td>[47:44]</td><td>0xf</td><td>User-defined</td><td>Over voltage protection delay time:
Bit[62] =0，[47:44]*128ms；
Bit[62] =1, [47:44]*512ms</td></tr>
<tr><td>[43:40]</td><td>0xf</td><td>User-defined</td><td>Under voltage protection delay time：
Bit[60] =0，[43:40]*512ms；</td></tr>
</table>

				Bit[60] =1，[43:40]*1024ms
	[39:36]	0xf	User-defined	Under temperature protection delay time: [39:36]*512ms
	[35:32]	0xf	User-defined	Over temperature protection delay time: [35:32]*512ms
	[31:24]	0xff	User-defined	Over voltage threshold: ([31:24]+1)*64*5/16384V
	[23:16]	0x0	User-defined	Under voltage threshold: ([23:16]+1)*64*5/16384V
	[15:8]	0xff	User-defined	Setting charge under temperature protection threshold: ([15:8]+1)*64*5/16384V
	[7:0]	0x0	User-defined	Setting charge over temperature protection threshold: ([7:0]+1)*64*5/16384V
CRC(1B)				∑(DATA,CRC) = 0xff

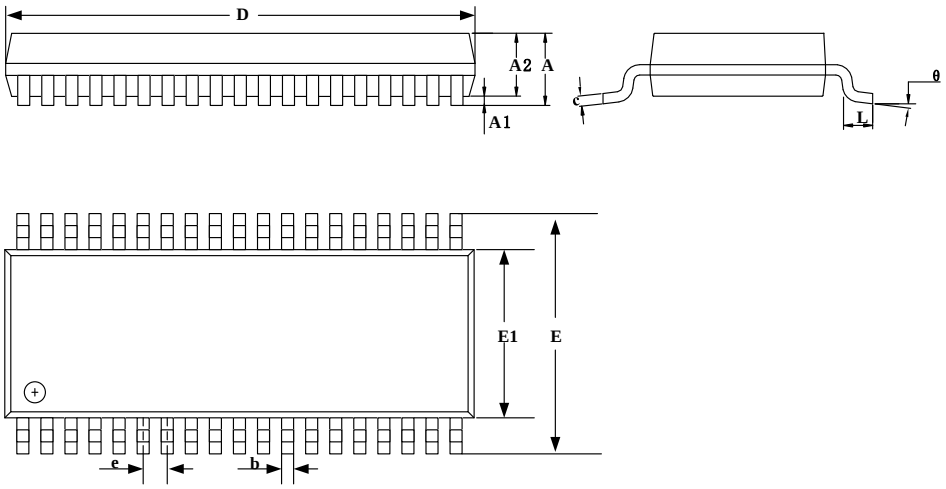
Table 10. Current Parameter Set

Item	Content	Default	Recommend	Description
CMD(1B)				0x08
DATA(10B)	[79:76]	0x7	0x7	Charge/Discharge status detection threshold: ±[79:76]*32*0.2/65536 Default: 0.6836mV Charge status: $V_{ISP-ISN}$< - [79:76]*32*0.2/65536 Discharge status: $V_{ISP-ISN}$>[79:76]*32*0.2/65536
	[75:70]	0x5	User-defined	Short circuit threshold in discharge: {[75] *240mV+(~[74]) *120mV+(~[73]) *60mV+ (~[72]) *30mV+(~[71]) *15mV+(~[70]) *7.5mV+42.5mV} Default: 237.5mV Hysteresis: 5mV **Notice**: "~" is negation symbol, bit [74:70] need negation operation, for example, bit [75:70] set as 000101, the short circuit threshold is: 0*240mV+1*120mV+1*60mV+0*30mV+1*15mV+ 0*7.5mV+42.5mV=237.5mVl
	[69]	0x0	0x1	Forced to 1
	[68:64]	0x1f	0x1f	Short circuit delay time in discharge: ([68:64]+1)*64μs
	[63:62]	0x2	0x2	Low current wakeup threshold (V_{LC}): 0x2:350uV 0x3:400uV $V_{SRP-SRN}$ within that range: the Sleep entry is permitted. $V_{SRP-SRN}$ beyond that range: the Sleep entry is prohibited. Note: Only low current wakeup function is enabled
	[61:60]	0x0	0x0	Forced to 0
	[59:56]	0xf	User-defined	charge over current protection delay time；[59:56]*64ms

	[55:51]	0x1f	User-defined	The second grade over current protection delay time: [55:51]*step, Step is controlled by [45].
	[50:46]	0x1f	User-defined	The first grade over current protection delay time: [50:46]*256ms+128ms
	[45]	0x0	0x1	time step for secondary discharge over current protection 0 : 4ms 1 : 32ms
	[44:40]	0x0	0xff	Reserved
	[39:32]	0xff	User-defined	The second grade over current protection threshold voltage in discharge:[39:32]*0.4/512
	[31:24]	0xff	User-defined	The first grade over current protection threshold voltage in discharge:[31:24]*0.4/512
	[23:16]	0x0	0xff	Reserved
	[15:8]	0xff	User-defined	The over current protection threshold voltage in charge: -[15:8]*0.4/512
	[8:0]	0x0	0xff	Reserved
CRC(1B)				∑(DATA,CRC) = 0xff

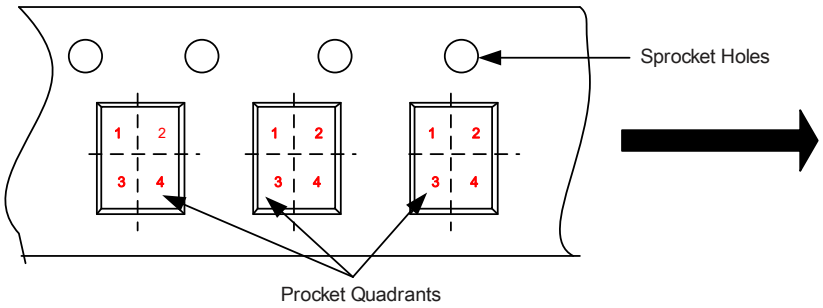
PACKAGE OUTLINE

TSSOP38 UNIT: mm



Symbol	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.20
A1	0.05	—	0.15
A2	0.60	—	1.00
b	0.15	—	0.31
c	0.07	—	0.25
D	9.20	9.70	10.20
E	5.85	6.40	6.85
E1	4.00	4.40	4.80
e	0.50BSC		
L	0.45	—	0.75
θ	0°	—	8°

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPAE



Package Type	Pin1 Quadrant
TSSOP38	1

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