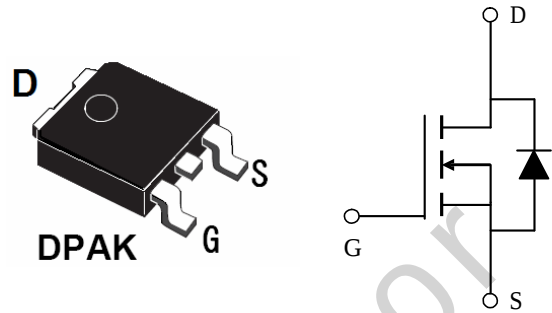


DESCRIPTION

The IRLR8726TRPBF is N channel enhancement mode power effect transistor which is produced using high cell density advanced trench technology.

The high density process is especially able to minize on-state resistance. These devices are. especially suited for low voltage application power management DC-DC converters.

PIN CONFIGURATION



FEATURE

- ◆ 30V/85A, $R_{DS(ON)}=4.0m\Omega(yp.)@V_{GS}=10V$
- ◆ 30V/65A, $R_{DS(ON)}=6.0m\Omega(yp.)@V_{GS}=4.5V$
- ◆ Super high design for extremely low $R_{DS(ON)}$
- ◆ Exceptional on-resistance and Maximum DC current capability
- ◆ Full RoHS compliance
- ◆ TO-252 package design
- ◆ 100% UIS Tested
- ◆ 100% Rg tested

APPLICATIONS

- ◆ Power Management
- ◆ DC/DC Converter
- ◆ Load Switch

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^{\circ}C$ Unless otherwise noted)

Symbol	Parameter	Max.	Units
V_{DS}	Drain-to-Source Voltage	30	V
V_{GS}	Gate-to-Source Voltage	± 20	
$I_D @ T_A = 25^{\circ}C$	Continuous Drain Current, $V_{GS} @ 10V$	18	A
$I_D @ T_A = 70^{\circ}C$	Continuous Drain Current, $V_{GS} @ 10V$	14	
$I_D @ T_C(Bottom) = 25^{\circ}C$	Continuous Drain Current, $V_{GS} @ 10V$	85	
$I_D @ T_C(Bottom) = 100^{\circ}C$	Continuous Drain Current, $V_{GS} @ 10V$	39	
$I_D @ T_C = 25^{\circ}C$	Continuous Drain Current, $V_{GS} @ 10V$ (Package Limited)	42	
I_{DM}	Pulsed Drain Current	160	
$P_D @ T_A = 25^{\circ}C$	Power Dissipation	3.6	W
$P_D @ T_C(Bottom) = 25^{\circ}C$	Power Dissipation	52	
	Linear Derating Factor	0.03	W/ $^{\circ}C$
T_J	Operating Junction and	-55 to + 150	$^{\circ}C$
T_{STG}	Storage Temperature Range		

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress rating only and functional device operation is not implied

■ **ELECTRICAL CHARACTERISTICS** ($T_A=25^{\circ}\text{C}$ Unless otherwise noted)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Static Parameters						
V _{(BR)DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D = 250uA	30			V
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D = 250uA	1.0		2.5	V
I _{GSS}	Gate Leakage Current	V _{DS} =0V, V _{GS} =±25V			±100	nA
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =-24V, V _{GS} =0			1	uA
		V _{DS} =-24V, V _{GS} =0 T _J =85°C			30	
R _{DS(ON)}	Drain-Source On-Resistance	V _{GS} = 10V, I _D = 20 A		4.0	5.5	mΩ
		V _{GS} = 4.5V, I _D = 15 A		6.0	6.8	
Source-Drain Diode						
V _{SD}	Diode Forward Voltage	I _S = 40 A, V _{GS} =0V		0.7	1.3	V
Dynamic Parameters						
Q _g	Total Gate Charge	V _{DS} = 15V V _{GS} = 10V I _D = 49 A		23		nC
Q _{gs}	Gate-Source Charge			5		
Q _{gd}	Gate-Drain Charge			3		
C _{iss}	Input Capacitance	V _{DS} = 10V V _{GS} =0V f=1MHz		1356		pF
C _{oss}	Output Capacitance			55		
C _{rss}	Reverse Transfer Capacitance			45		
T _{d(on)}	Turn-On Time	V _{DS} = 15V I _D = 40A V _{GEN} = 4.5V R _G =1.8Ω		8		nS
T _r				9		
T _{d(off)}	Turn-Off Time			32		
T _f				6		

Note: 1. Pulse test: pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$

2. Static parameters are based on package level with recommended wire bonding

■ **TYPICAL CHARACTERISTICS** (25°C Unless Note)

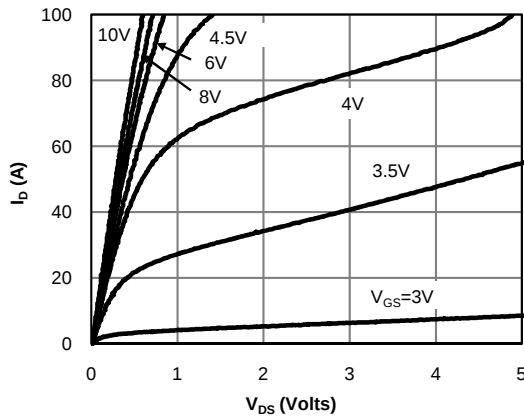


Fig 1: On-Region Characteristics (Note E)

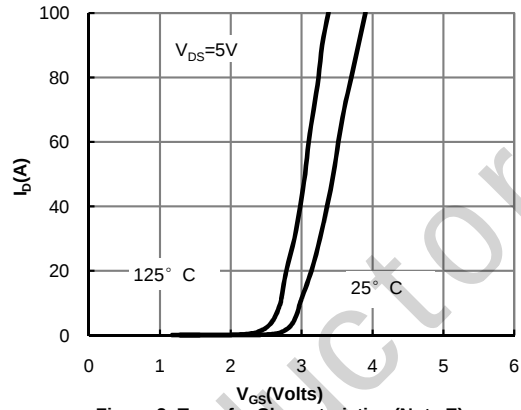


Figure 2: Transfer Characteristics (Note E)

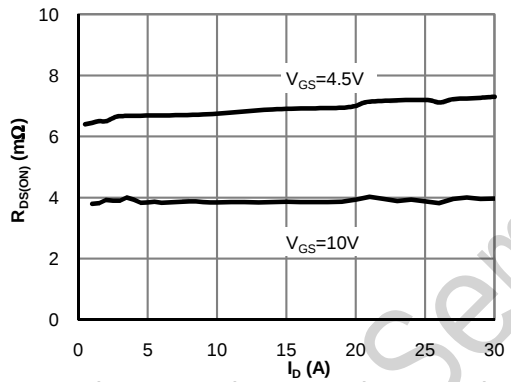


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

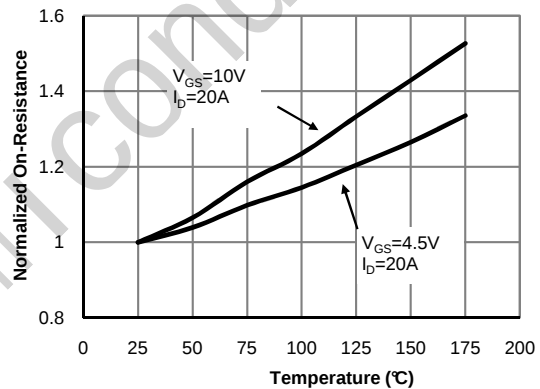


Figure 4: On-Resistance vs. Junction Temperature (Note E)

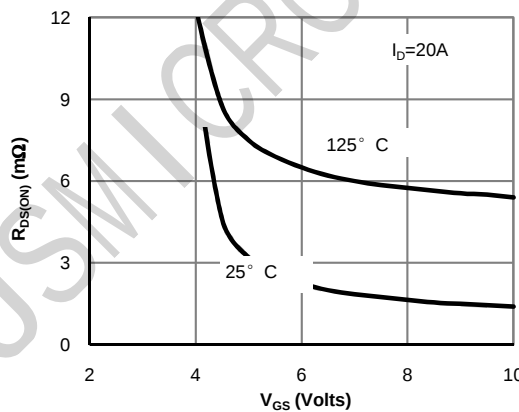


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

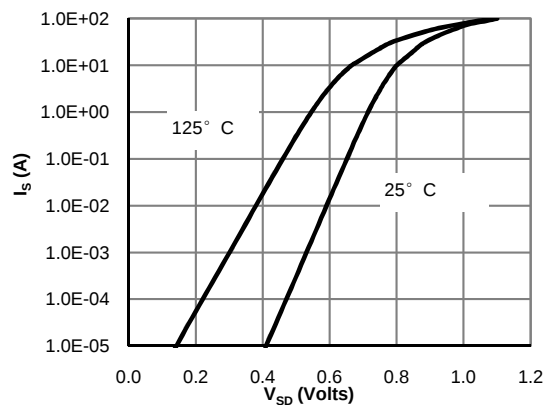
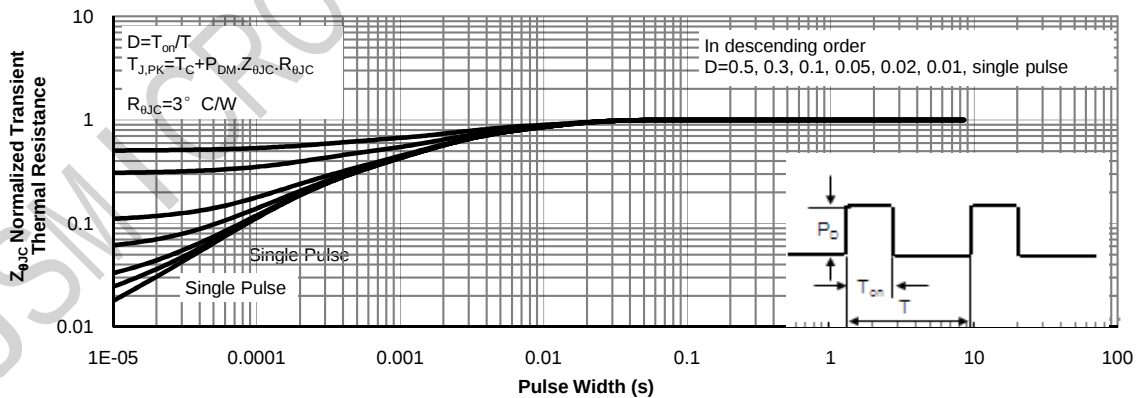
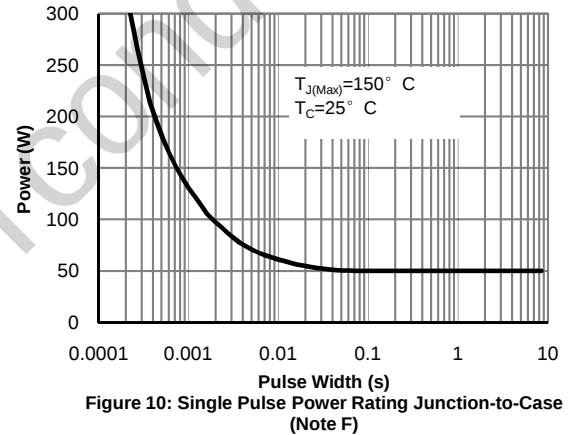
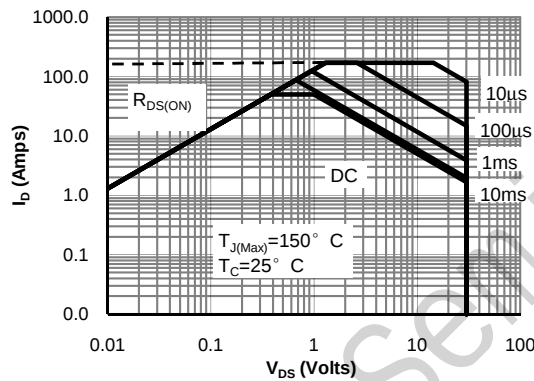
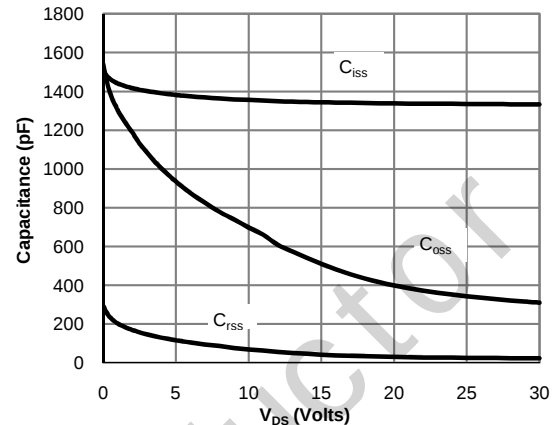
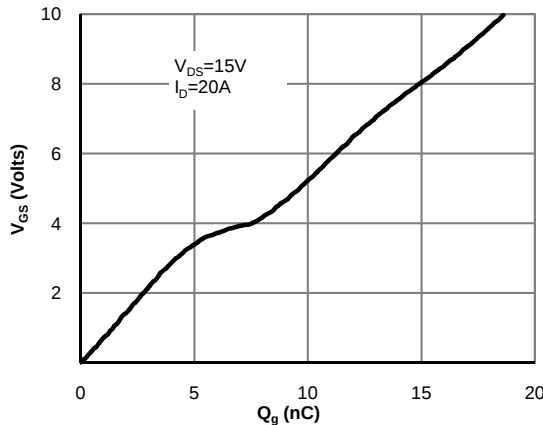


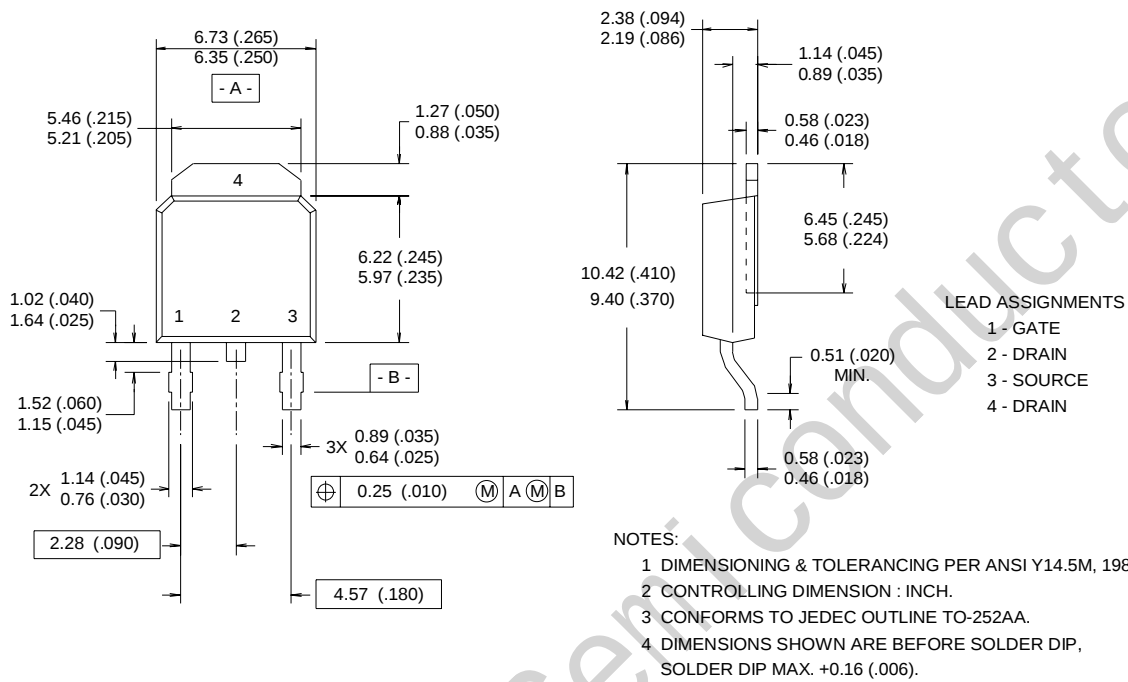
Figure 6: Body-Diode Characteristics (Note E)

■ TYPICAL CHARACTERISTICS (continuous)



■ TO-252 Outline Package Dimension

Dimensions are shown in millimeters (inches)



单击下面可查看定价，库存，交付和生命周期等信息

[>>JSMSEMI\(杰盛微\)](#)