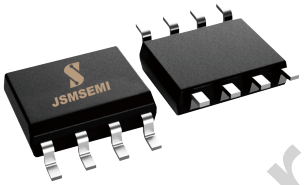
■ DESCRIPTION

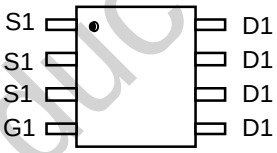
The AO4468 is the N-Channel logic enhancement mode power field effect transistor is produced using high cell density advanced trench technology..

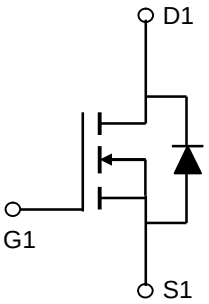
This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application, notebook computer power management and other battery powered circuits where high-side switching

■ PIN CONFIGURATION



Top View





■ FEATURE

- ***30V/10 A, $R_{DS(ON)}$=16mΩ (typ.)@VGS=10V***
- ***30V/10A, $R_{DS(ON)}$=20mΩ (typ.)@VGS= 4.5V***
- Super high design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and Maximum DC current capability
- Full RoHS compliance
- SOP8 package design
- 100% UIS Tested
- 100% Rg tested

■ APPLICATIONS

- Power Management
- Portable Equipment
- DC/DC Converter
- Load Switch
- DSC
- LCD Display inverter

■ ABSOLUTE MAXIMUM RATINGS (T_A = 25℃ Unless otherwise noted)

Symbol	Parameter		Typical	Unit
V_{DSS}	Drain-Source Voltage		30	V
V_{GSS}	Gate-Source Voltage		±20	V
I_D	Continuous Drain Current (TJ=150℃)	V_{GS}-10V	10	A
I_{DM}	Pulsed Drain Current		40	A
I_S	Continuous Source Current (Diode Conduction)		4.0	A
P_D	Power Dissipation	T_A=25℃	2.8	W
		T_A=70℃	1.8	
T_J	Operation Junction Temperature		150	℃
T_{STG}	Storage Temperature Range		-55~+150	℃
$R_{\theta JA}$	Thermal Resistance Junction to Ambient		62.5	℃/W

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress rating only and functional device operation is not implied

■ *ELECTRICAL CHARACTERISTICS(T_A=25℃ Unless otherwise noted)*

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Static Parameters						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D= 250uA	30			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D= 250uA	1.0		2.0	V
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±20V			±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}= 24V, V_{GS}=0			1	uA
		V_{DS}= 24V, V_{GS}=0 T_J=85℃			30	
$R_{DS(ON)}$	Drain-Source On-Resistance	V_{GS}= 10V, I_D= 10 A		16	25	mΩ
		V_{GS}= 4.5V, I_D= 8 A		20	30	
Source-Drain Diode						
V_{SD}	Diode Forward Voltage	I_S= 2.0A, V_{GS}=0V		0.7	1.3	V
Dynamic Parameters						
Q_g	Total Gate Charge	V_{DS}= 15V		11.6		nC
Q_{gs}	Gate-Source Charge	V_{GS}= 10V		2.5		
Q_{gd}	Gate-Drain Charge	I_D= 9.0A		3.9		
C_{iss}	Input Capacitance	V_{DS}= 25V		770		pF
C_{oss}	Output Capacitance	V_{GS}=0V		110		
C_{rss}	Reverse Transfer Capacitance	f=1MHz		90		
$T_{d(on)}$	Turn-On Time	V_{DS}= 15V		5		nS
T_r		R_L=15Ω		3.5		
$T_{d(off)}$	Turn-Off Time	I_D= 1A		19		
T_f		V_{GEN}= 10V R_G=6Ω		3.5		

Note: 1. Pulse test: pulse width<=300uS, duty cycle<=2%

2.Static parameters are based on package level with recommended wire bonding

■ *TYPICAL CHARACTERISTICS (25℃ Unless Note)*

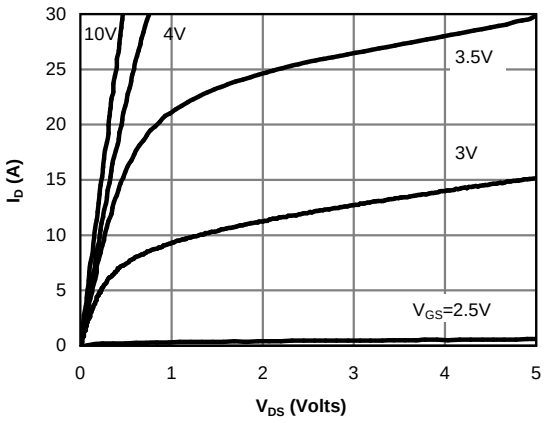


Fig 1: On-Region Characteristics (Note E)

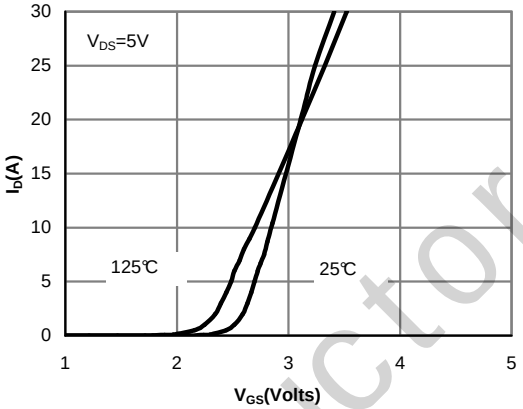


Figure 2: Transfer Characteristics (Note E)

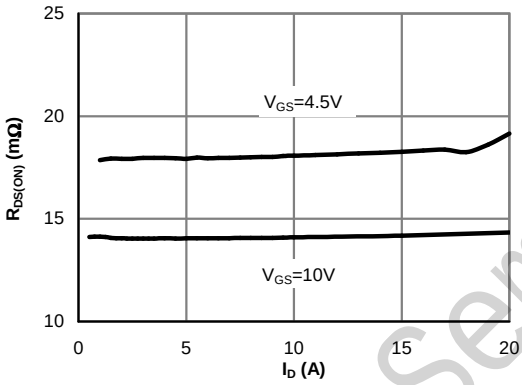


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

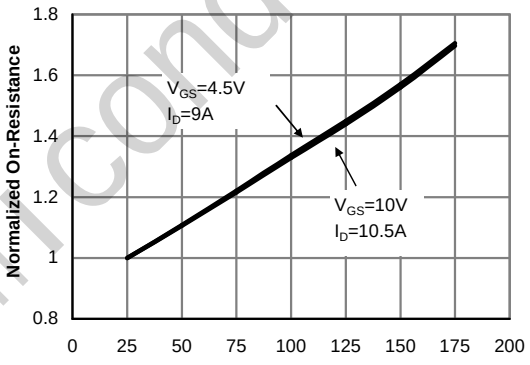


Figure 4: On-Resistance vs. Junction Temperature (Note E)

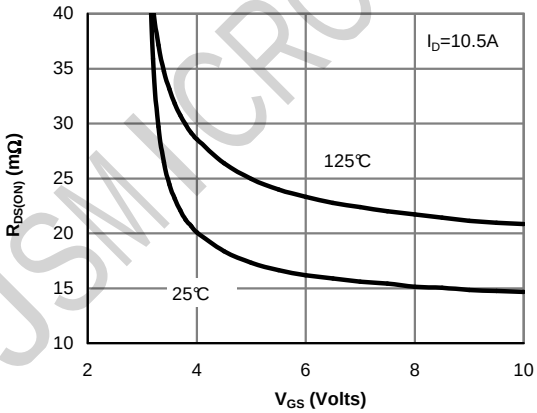


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

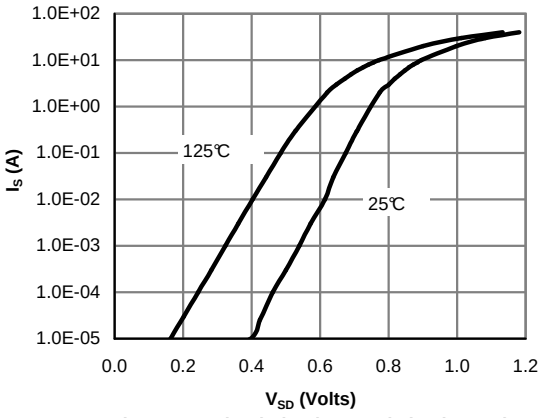


Figure 6: Body-Diode Characteristics (Note E)

■ *TYPICAL CHARACTERISTICS (continuous)*

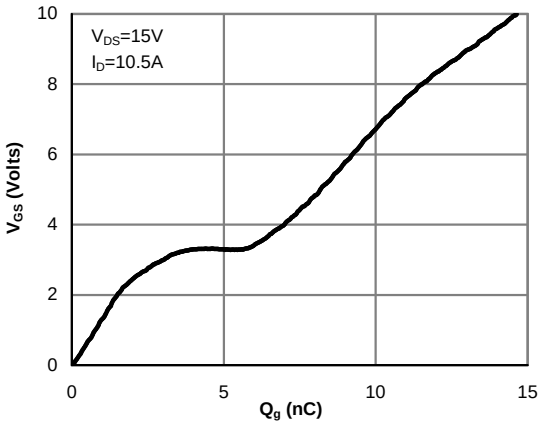


Figure 7: Gate-Charge Characteristics

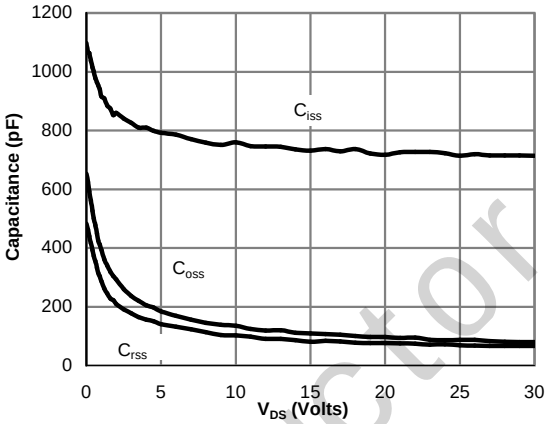


Figure 8: Capacitance Characteristics

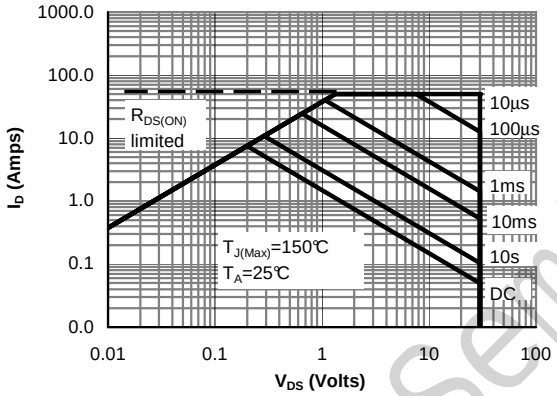


Figure 10: Maximum Forward Biased Safe Operating Area (Note F)

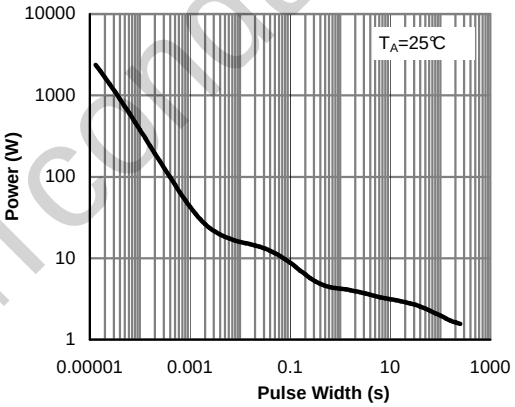


Figure 11: Single Pulse Power Rating Junction-to-Ambient (Note F)

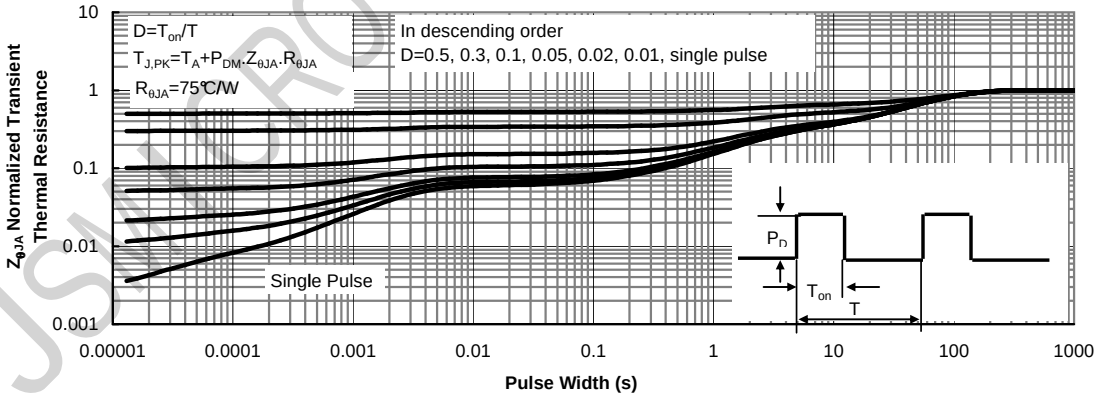
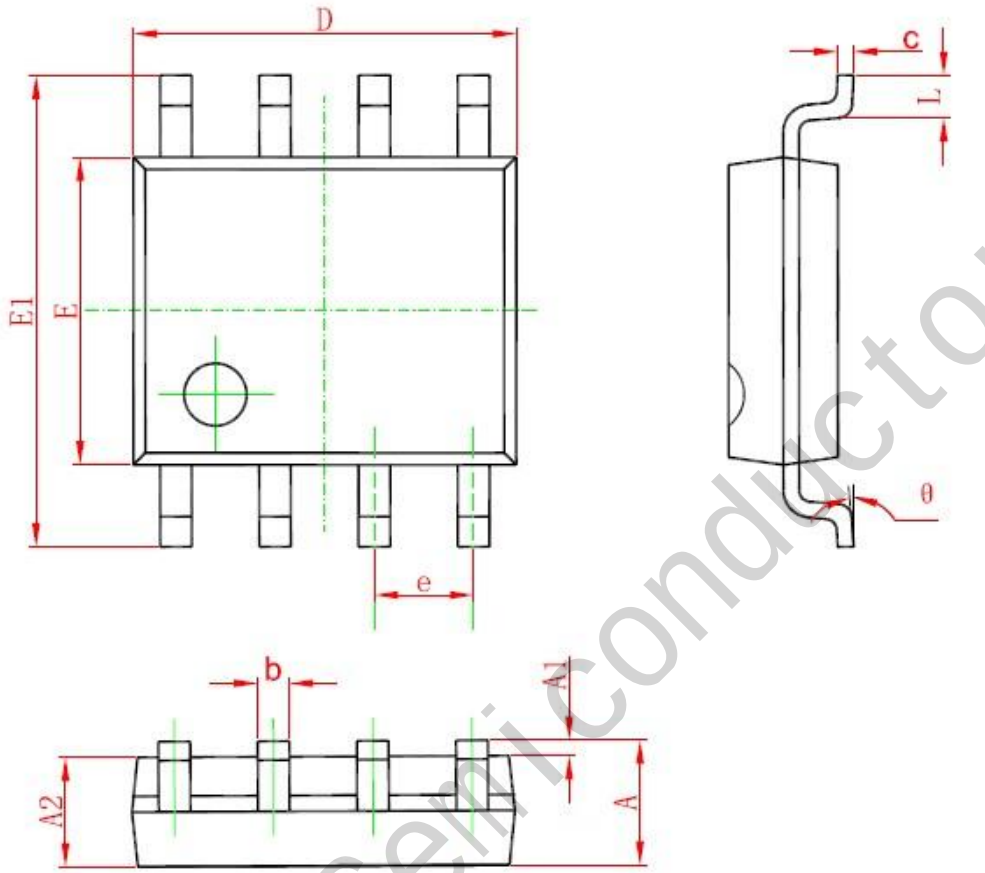


Figure 12: Normalized Maximum Transient Thermal Impedance (Note F)

■ *SOP8 PACKAGE OUTLINE DIMENSIONS*



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

单击下面可查看定价，库存，交付和生命周期等信息

>>JSMSEMI(杰盛微)