

DESCRIPTION

The P3203CMG is the N-Channel logic enhancement mode power field effect transistor is produced using high cell density advanced trench technology.

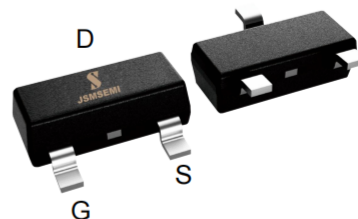
This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application, and low in-line power loss are needed in a very small outline surface mount package.

FEATURE

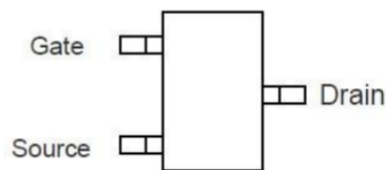
- ◆ 30V/6.0A, $R_{DS(ON)}=18m\Omega(\text{typ.})@V_{GS}=10V$
- ◆ 30V/4.8A, $R_{DS(ON)}=25m\Omega(\text{typ.})@V_{GS}=4.5V$
- ◆ Super high design for extremely low $R_{DS(ON)}$
- ◆ Exceptional on-resistance and Maximum DC current capability
- ◆ Full RoHS compliance
- ◆ SOT23 package design

APPLICATIONS

- ◆ Power Management
- ◆ Portable Equipment
- ◆ DC/DC Converter
- ◆ Load Switch
- ◆ DSC



N-Channel MOSFET



TOP VIEW
SOT-23

ABSOLUTE MAXIMUM RATINGS ($T_A=25^\circ\text{C}$ Unless otherwise noted)

Symbol	Parameter		Typical	Unit
V_{DSS}	Drain-Source Voltage		30	V
V_{GSS}	Gate-Source Voltage		± 20	V
I_D	Continuous Drain Current ($T_C=25^\circ\text{C}$)	$V_{GS}=10V$	6.0	A
	Continuous Drain Current ($T_C=70^\circ\text{C}$)		5.0	
I_{DM}	Pulsed Drain Current		20	A
I_S	Continuous Source Current (Diode Conduction)		1.5	A
P_D	Power Dissipation	$T_A=25^\circ\text{C}$	1.5	W
		$T_A=70^\circ\text{C}$	0.9	
T_J	Operation Junction Temperature		150	$^\circ\text{C}$
T_{STG}	Storage Temperature Range		-55~+150	$^\circ\text{C}$
$R_{\theta JA}$	Thermal Resistance Junction to Ambient		90	$^\circ\text{C/W}$

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress rating only and functional device operation is not implied

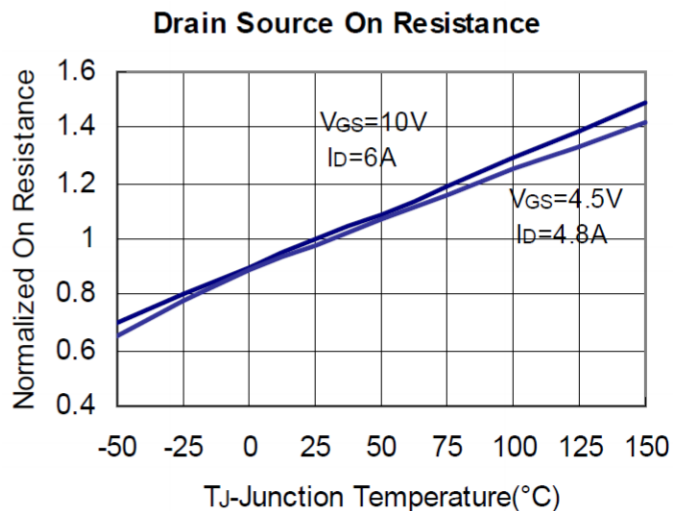
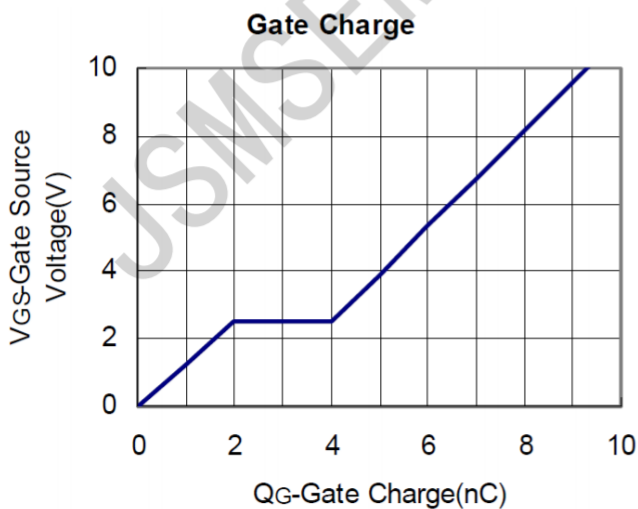
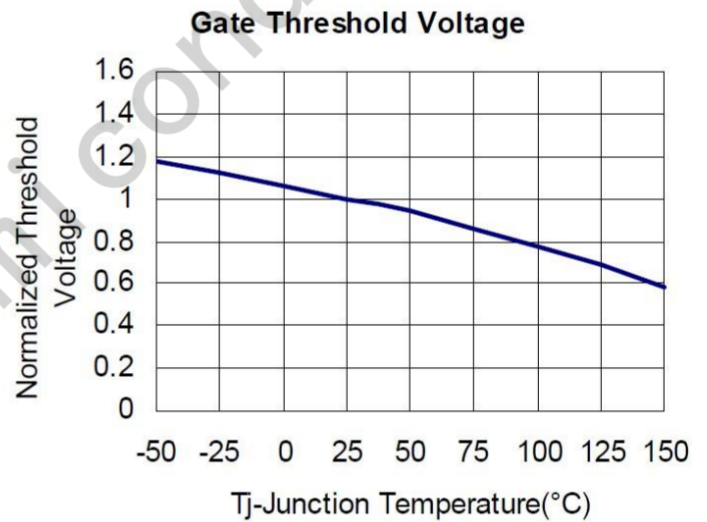
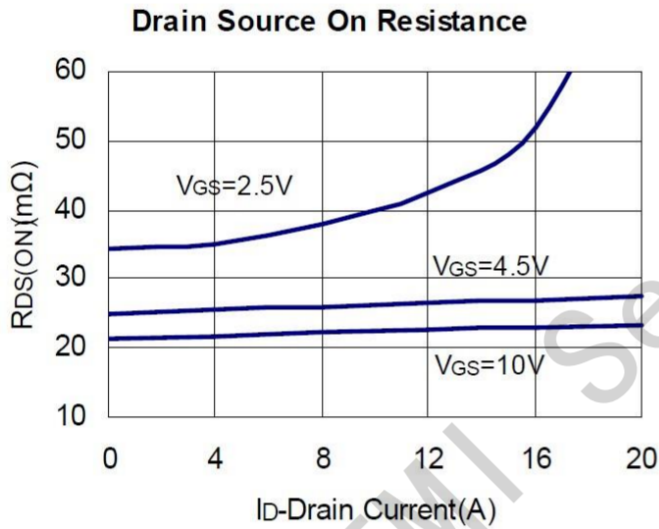
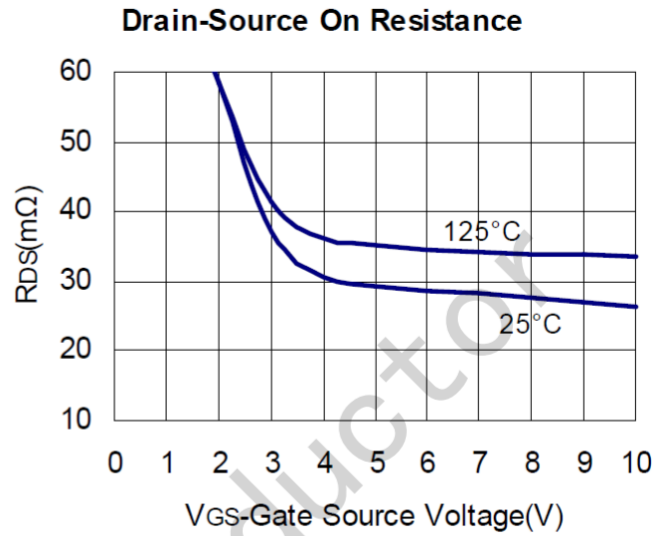
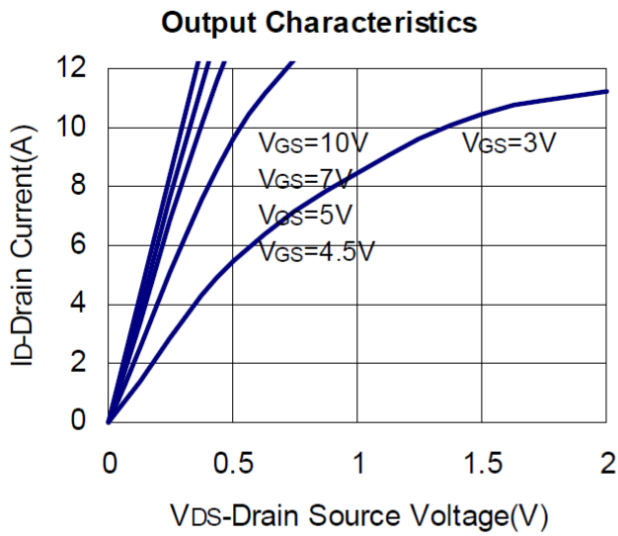
ELECTRICAL CHARACTERISTICS ($T_A=25^\circ\text{C}$ Unless otherwise noted)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Static Parameters						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	30			V
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	1		2	V
I_{GSS}	Gate Leakage Current	$V_{DS}=0V, V_{GS}=\pm 20V$			± 100	nA
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=24V, V_{GS}=0$			1	uA
		$V_{DS}=24V, V_{GS}=0$ $T_J=55^\circ\text{C}$			5	
$R_{DS(ON)}$	Drain-Source On-Resistance	$V_{GS}=10V, I_D=6.0A$		18	30	m Ω
		$V_{GS}=4.5V, I_D=4.8A$		25	40	
Source-Drain Diode						
V_{SD}	Diode Forward Voltage	$I_S=1.0A, V_{GS}=0V$		0.7	1.0	V
Dynamic Parameters						
Q_g	Total Gate Charge	$V_{DS}=20V$		6		nC
Q_{gs}	Gate-Source Charge	$V_{GS}=4.5V$		1.1		
Q_{gd}	Gate-Drain Charge	$I_D=6.0A$		2.5		
C_{iss}	Input Capacitance	$V_{DS}=15V$		414		pF
C_{oss}	Output Capacitance	$V_{GS}=0V$		60		
C_{rss}	Reverse Transfer Capacitance	$f=1\text{MHz}$		49		
$T_{d(on)}$	Turn-On Time	$V_{DS}=15V$		7.5		nS
T_r		$I_D=5A$		45		
$T_{d(off)}$	Turn-Off Time	$V_{GEN}=10V$		10		
T_f		$R_G=3.3\Omega$		4		

Note: 1. Pulse test: pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$

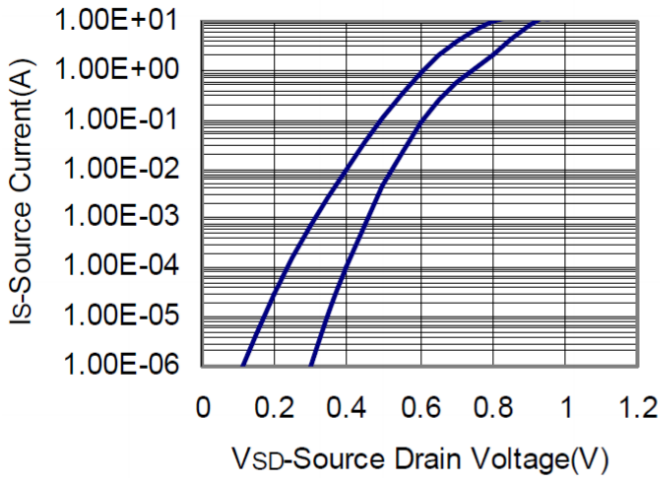
2. Static parameters are based on package level with recommended wire bonding

■ TYPICAL CHARACTERISTICS (25°C Unless Note)

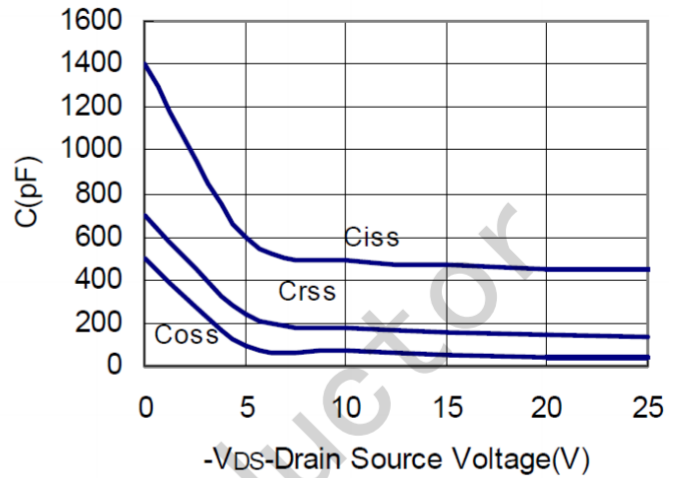


■ TYPICAL CHARACTERISTICS (continuous)

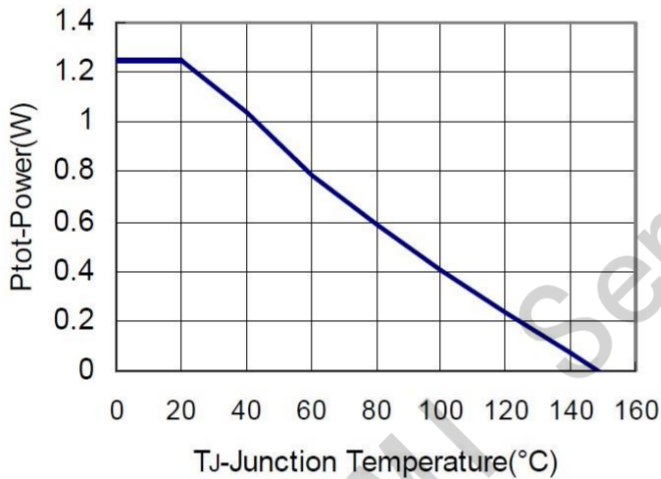
Source Drain Diode Forward



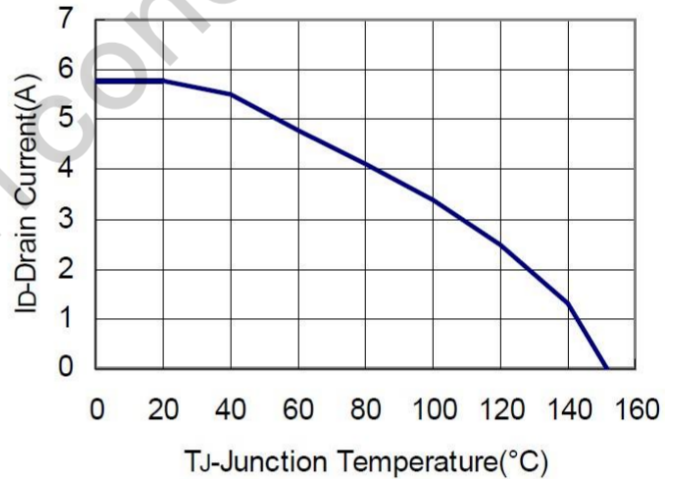
Capacitance



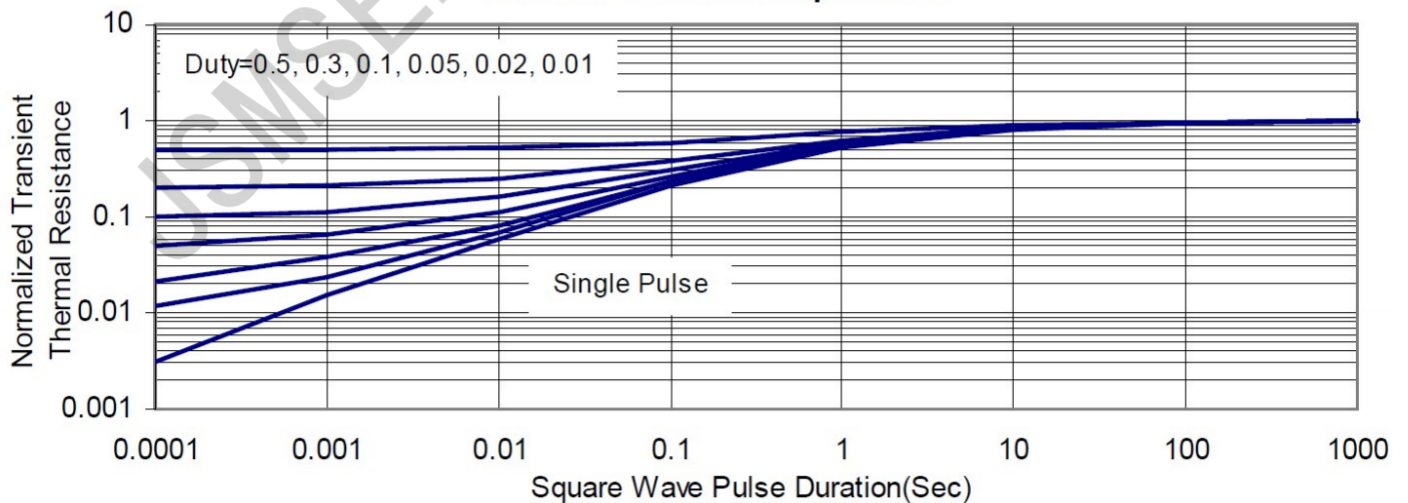
Power Dissipation



Drain Current

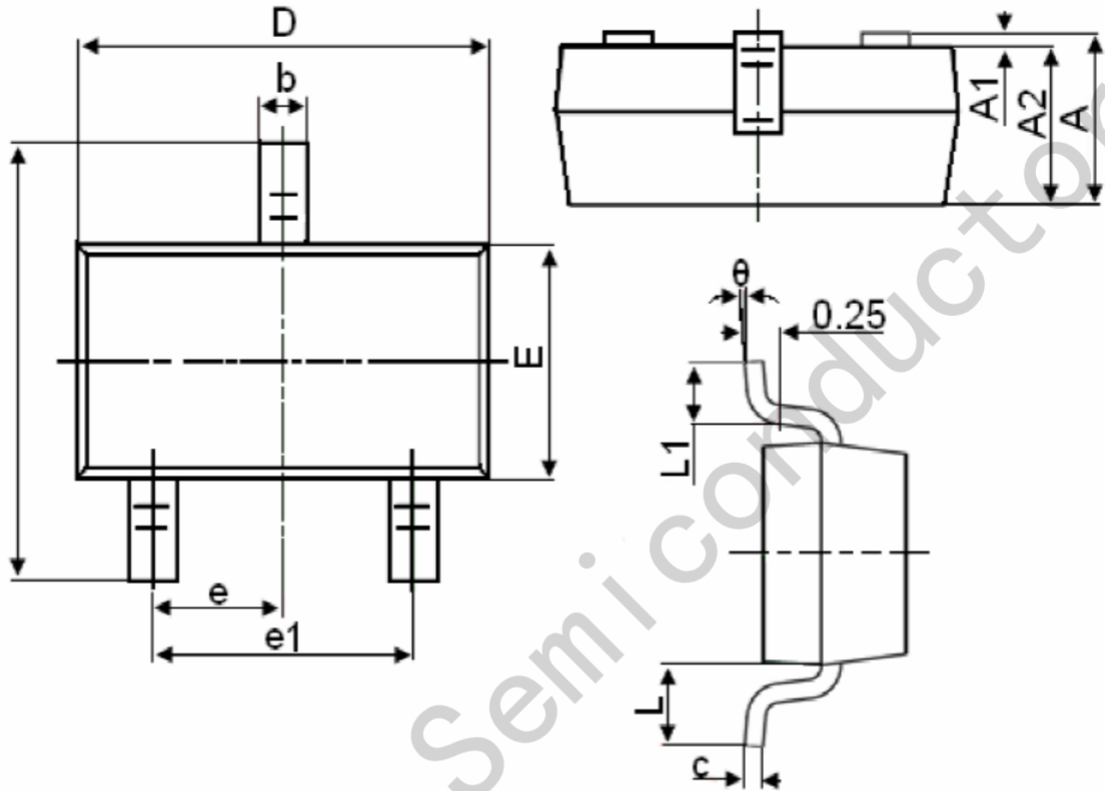


Thermal Transient Impedance



Package Information

SOT-23



Symbol	Dimensions in Millimeters(mm)		Dimensions In Inches	
	Min	Max	Min	Max
A	0.900	1.150	0.035	0.045
A1	0.000	0.100	0.000	0.004
A2	0.900	1.050	0.035	0.041
b	0.300	0.500	0.012	0.020
c	0.080	0.150	0.003	0.006
D	2.800	3.000	0.110	0.118
E	1.200	1.400	0.047	0.055
E1	2.250	2.550	0.089	0.100
e	0.950TYP		0.037TYP	
e1	1.800	2.000	0.071	0.079
L	0.550REF		0.022REF	
L1	0.300	0.500	0.012	0.020
θ	0°	8°	0°	8°

单击下面可查看定价，库存，交付和生命周期等信息

[>>JSMSEMI\(杰盛微\)](#)