



Click [here](#) for the 3D model.

### Dimensions

Chip Size	0805
L	2.032mm +/-0.381mm (0.08 in +/-0.015 in)
W	1.27mm +/-0.381mm (0.05 in +/-0.015 in)
T	1.397mm MAX (0.055 in MAX)

### Packaging Specifications

Packaging	Waffle
Packaging Quantity	25000

### General Information

Series	SMD Mil PRF123
Style	SMD Chip
Description	SMD Chip, Ultra Stable
RoHS	No
Prop 65	<b>⚠ WARNING:</b> Cancer and reproductive harm - <a href="http://www.p65warnings.ca.gov">http://www.p65warnings.ca.gov</a>
Termination	Tin
Failure Rate	N/A
AEC-Q200	No
Shelf Life	78 Weeks
MSL	1

### Specifications

Capacitance	27 pF
Capacitance Tolerance	10%
Voltage DC	100 VDC
Dielectric Withstanding Voltage	250 VDC
Temperature Range	-55/+125°C
Temperature Coefficient	BP
Capacitance Change with Reference to +25°C and 0 VDC Applied (TCC)	15%, 1MHz 1.0Vms
Dissipation Factor	2.5%
Insulation Resistance	100 GOhms

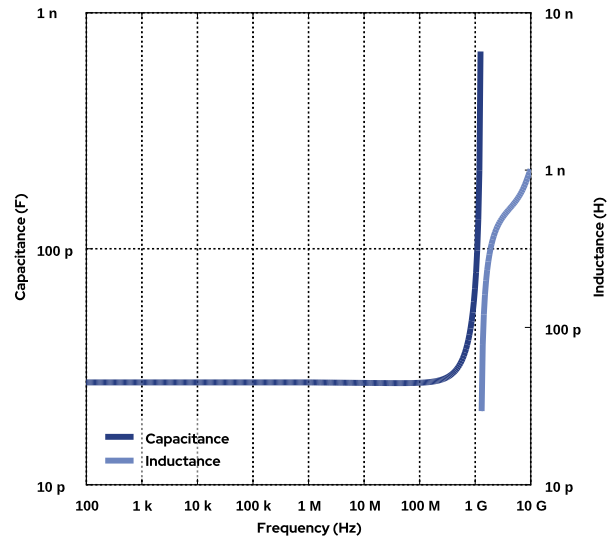
## Simulations

For the complete simulation environment please visit [K-SIM](#).

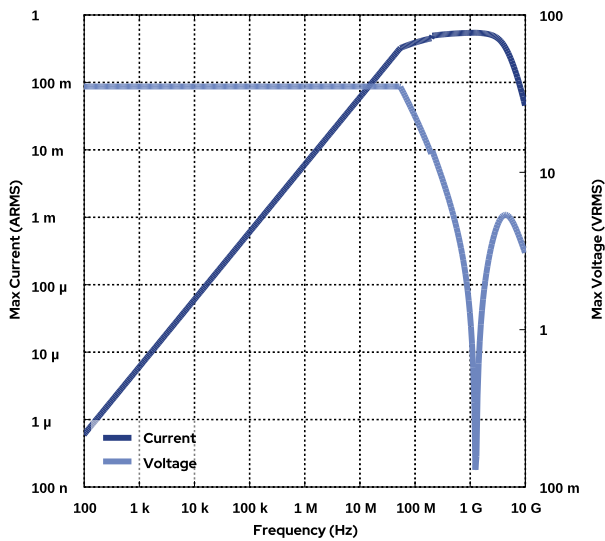
**Impedance and ESR**



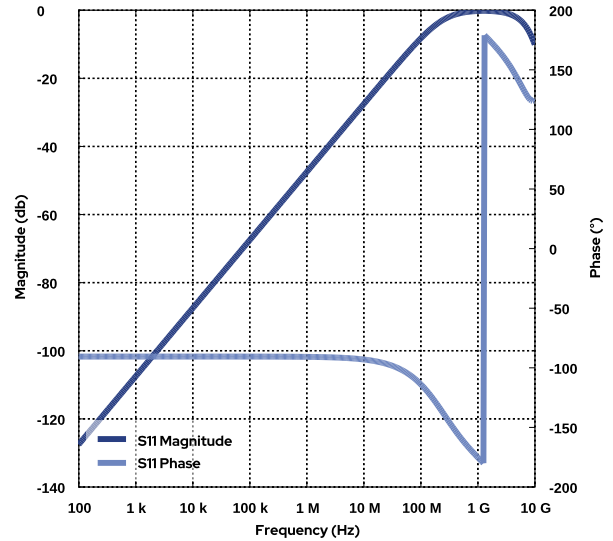
**Capacitance and Inductance**

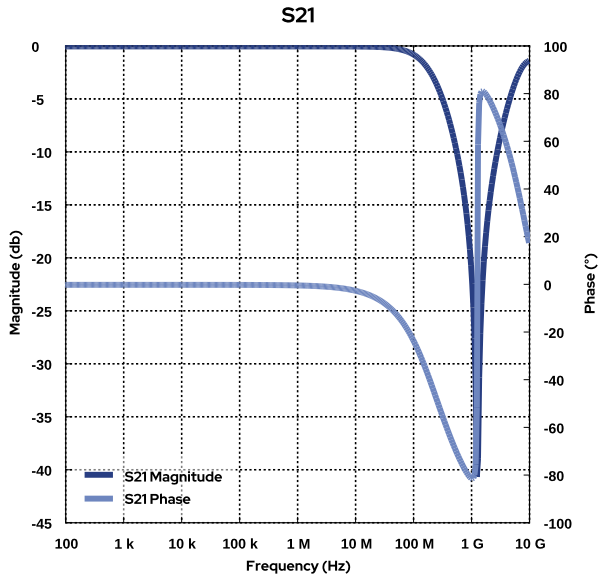


**Current and Voltage**



**S11**





**These are simulations.**

This is not a specification!

The responses shown represent the typical response for each part type. Specific responses may vary, depending on manufacturing variation affects of all parameters involved, including the specified tolerances applied to capacitance and unspecified variations of ESR, ESL, and leakage resistance.

The responses shown do not represent a specified or implied maximum capability of the device for all applications.

- The ESR used for ripple "Ripple Current/Voltage vs. Frequency" plots is the ESR at ambient temperature.
- The ESR in the "Temperature Rise vs. Ripple Current" plots is adjusted to each incremental temperature rise before the power and ripple current is calculated.
- The effects shown herein are based on measured data from a multiple part sample of the parts in question.
- Ripple capability of this device will be factored by thermal resistance (Rth) created by circuit traces (addi affects of all parameters involved, including the specified tolerances applied to capacitance and unspecified variations of ESR, ESL, and leakage resistance.
- The peak voltages generated in the "Temperature Rise vs. Combined Ripple Currents" plot are calculated for each frequency and are not combined with voltages generated at any other harmonics.
- Please consult with the catalog or field applications engineer for maximum capability of the device in specific applications.

All product information and data (collectively, the "Information") are subject to change without notice.

KEMET K-SIM is designed to simulate behavior of components with respect to frequency, ambient temperature, and DC bias levels. The responses shown represent the typical response for each part type. Specific responses may vary, depending on manufacturing variation effects of all parameters involved, including the specified tolerances applied to capacitance and unspecified variations of ESR, ESL, and leakage resistance.

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If you have any questions please contact K-SIM.

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