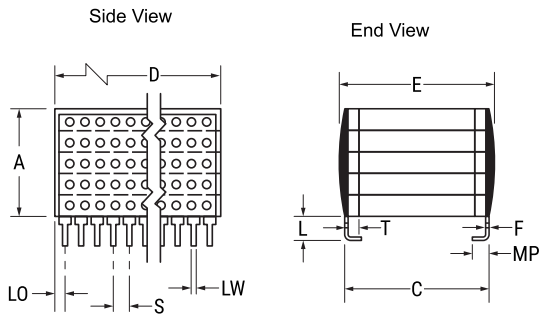


KPS LDD Comm SMPS, Ceramic, 50 uF, 10%, 100 VDC, BR, N/A



Dimensions	
D	25.715mm +/-1.585mm
L	1.78mm +/-0.25mm
T	1.397mm MAX
S	2.54mm TYP
F	0.254mm +/-0.051mm
A	16.51mm MAX
C	11.43mm +/-0.635mm
E	12.7mm MAX
LO	1.586mm MAX
LW	0.508mm +/-0.051mm
MP	1.27mm MIN

Packaging Specifications	
Packaging:	Waffle, Box
Packaging Quantity:	28

General Information	
Series:	KPS LDD Comm SMPS
Style:	Leaded Stacked Chip
Description:	Low ESR, High Current Stacked Ceramic Chips
Features:	Low ESR, High Current, High Performance
RoHS:	No
Prop 65:	WARNING: Cancer and reproductive harm - www.p65warnings.ca.gov .
SCIP Number:	4221181d-d71c-4d0a-af45-5eab760732b2
Termination:	60/40 Solder Coated
Lead:	J Leads
Failure Rate:	N/A
Testing and Reliability:	Commercial
AEC-Q200:	No
Notes:	Note: Number of chips in stack depends on design. Number of Chips in this stack = 5. Note: Turn Radius For Lead Extension Is 0.1 Radians (Typical). Note: Lead alignment within pin rows shall be within ±0.13 mm.

Specifications	
Capacitance:	50 uF
Capacitance Tolerance:	10%
Voltage DC:	100 VDC
Dielectric Withstanding Voltage:	250 VDC
Temperature Range:	-55/+125°C
Temperature Coefficient:	BR
Dissipation Factor:	2.5% 1 kHz 25C
Aging Rate:	1% Loss/Decade Hour
Insulation Resistance:	2 GOhms

Statements of suitability for certain applications are based on our knowledge of typical operating conditions for such applications, but are not intended to constitute - and we specifically disclaim - any warranty concerning suitability for a specific customer application or use. This Information is intended for use only by customers who have the requisite experience and capability to determine the correct products for their application. Any technical advice inferred from this Information or otherwise provided by us with reference to the use of our products is given gratis, and we assume no obligation or liability for the advice given or results obtained.

单击下面可查看定价，库存，交付和生命周期等信息

[>>KEMET\(基美\)](#)