



Click [here](#) for the 3D model.

Dimensions

| | |
|---|--------------------|
| D | 25.64mm +/-0.635mm |
| L | 6.35mm MIN |
| H | 2.54mm NOM |
| F | 1.397mm +/-0.25mm |
| A | 8.13mm MAX |
| B | 9.908mm MAX |
| C | 11.43mm +/-0.635mm |
| E | 12.7mm MAX |
| K | 0.5mm NOM |

Packaging Specifications

| | |
|--------------------|-------------|
| Packaging | Waffle, Box |
| Packaging Quantity | 16 |

General Information

| | |
|-------------|--|
| Series | KPS-MCC Indust COG HT200C |
| Style | Leaded Stacked Chip |
| Description | Low ESR, Stacked Ceramic Chips |
| Features | 200C, Low ESR, High Thermal Stability, Bulk Capacitance |
| RoHS | No |
| Prop 65 | ⚠ WARNING: Cancer and reproductive harm - http://www.p65warnings.ca.gov |
| Termination | 60/40 Solder Coated |
| Lead | Straight Leads |
| AEC-Q200 | No |
| Notes | Number of chips in this stack: 6. |

Specifications

| | |
|---------------------------------|---------------------|
| Capacitance | 1.2 uF |
| Capacitance Tolerance | 10% |
| Voltage DC | 500 VDC |
| Dielectric Withstanding Voltage | 650 VDC |
| Temperature Range | -55/+200°C |
| Temperature Coefficient | COG |
| Dissipation Factor | 0.1% 1kHz 25C |
| Aging Rate | 0% Loss/Decade Hour |
| Insulation Resistance | 830 MOhms |

Statements of suitability for certain applications are based on our knowledge of typical operating conditions for such applications, but are not intended to constitute - and we specifically disclaim - any warranty concerning suitability for a specific customer application or use. This information is intended for use only by customers who have the requisite experience and capability to determine the correct products for their application. Any technical advice inferred from this information or otherwise provided by us with reference to the use of our products is given gratis, and we assume no obligation or liability for the advice given or results obtained.

单击下面可查看定价，库存，交付和生命周期等信息

[>>KEMET\(基美\)](#)