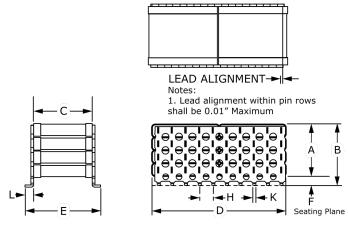


General Information



Series	KPS-MCC Indust COG HT200C	
Style	Leaded Stacked Chip	
Description	Low ESR, Stacked Ceramic Chips	
Features	200C, Low ESR, High Thermal Stability, Bulk Capacitance	
RoHS	With Exemptions	
REACH	SVHC (Pb – CAS 7439-92-1)	
SCIP Number	297427bb-2a48-4853-b594-641304a2cc24	
Termination	Silver	
Lead	L Leads	
AEC-Q200	No	
Notes	Number of chips in this stack: 8.	

Click here for the 3D model.

Dimensions	
D	25.64mm +/-0.635mm
L	1.4mm +/-0.127mm
Н	2.54mm NOM
F	1.778mm +/-0.25mm
А	10.67mm MAX
В	12.702mm MAX
С	11.43mm +/-0.635mm
E	13.7mm +/-0.89mm
К	0.5mm NOM

Packaging Specifications

Packaging	Waffle, Box
Packaging Quantity	16

Specifications				
Capacitance	1uF			
Capacitance Tolerance	10%			
Voltage DC	630 VDC			
Dielectric Withstanding Voltage	819 VDC			
Temperature Range	-55/+200°C			
Temperature Coefficient	COG			
Dissipation Factor	0.1% 1 kHz 25C			
Aging Rate	0% Loss/Decade Hour			
Insulation Resistance	1GOhms			

Statements of suitability for certain applications are based on our knowledge of typical operating conditions for such applications, but are not intended to constitute - and we specifically disclaim - any warranty concerning suitability for a specific customer application or use. This Information is intended for use only by customers who have the requisite experience and capability to determine the correct products for their application. Any technical advice inferred from this Information or otherwise provided by us with reference to the use of our products is given gratis, and we assume no obligation or liability for the advice given or results obtained.

单击下面可查看定价,库存,交付和生命周期等信息

>>KEMET(基美)