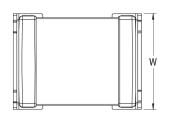
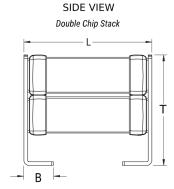


TOP VIEW Single or Double Chip Stack





General Information	
Series	KPS SMD Comm X7R HV
Style	Stacked Chip
Description	SMD, MLCC, Stacked, Double Chip, High Voltage, Temperature Stable
Features	Temperature Stable
RoHS	Yes
Termination	Tin
AEC-Q200	No
Component Weight	800 mg
Miscellaneous	X7R dielectric is not recommended for AC line filtering or pulse applications.
Chip Size	2220-2
Shelf Life	78 Weeks
MSL	1

Click here for the 3D model.

Dimensions	
L	6mm +/-0.5mm
W	5mm +/-0.5mm
т	5mm +/-0.50mm
В	1.6mm +/-0.3mm

Packaging Specifications	
Packaging	T&R, 180mm, Plastic Tape
Packaging Quantity	200

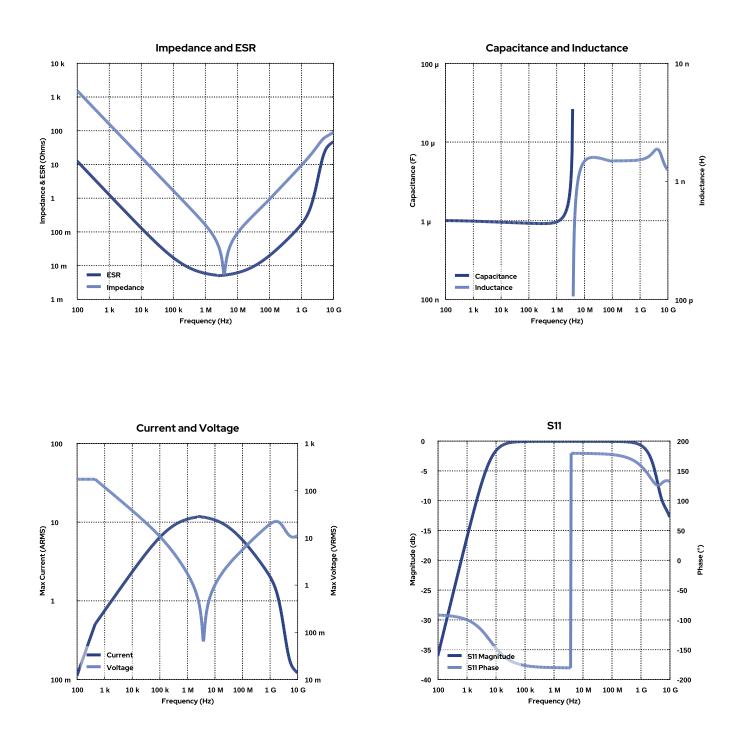
Specifications			
Specifications			
Capacitance	1uF		
Measurement Condition	1 kHz 1.0Vrms		
Capacitance Tolerance	20%		
Voltage DC	500 VDC		
Dielectric Withstanding Voltage	750 VDC		
Temperature Range	-55/+125°C		
Temperature Coefficient	X7R		
Capacitance Change with Reference to +25°C and 0 VDC Applied (TCC)	15%, 1kHz 1.0Vrms		
Dissipation Factor	2.5% 1 kHz 1.0Vrms		
Aging Rate	3% Loss/Decade Hour: Referee Time is 1000 Hours		
Insulation Resistance	100 MOhms		

Statements of suitability for certain applications are based on our knowledge of typical operating conditions for such applications, but are not intended to constitute - and we specifically disclaim - any warranty concerning suitability for a specific customer application or use. This Information is intended for use only by customers who have the requisite experience and capability to determine the correct products for their application. Any technical advice inferred from this Information or otherwise provided by us with reference to the use of our products is given gratis, and we assume no obligation or liability for the advice given or results obtained.

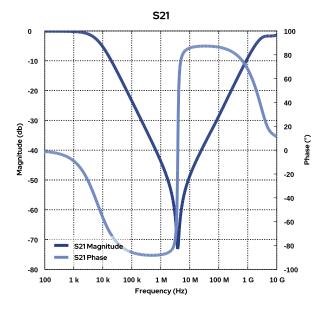


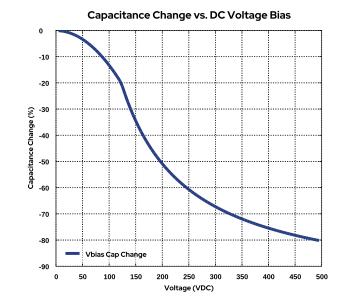
## Simulations

For the complete simulation environment please visit K-SIM.











## These are simulations.

This is not a specification!

The responses shown represent the typical response for each part type. Specific responses may vary, depending on manufacturing variation affects of all parameters involved, including the specified tolerances applied to capacitance and unspecified variations of ESR, ESL, and leakage resistance.

The responses shown do not represent a specified or implied maximum capability of the device for all applications.

- The ESR used for ripple "Ripple Current/Voltage vs. Frequency" plots is the ESR at ambient temperature.
- The ESR in the "Temperature Rise vs. Ripple Current" plots is adjusted to each incremental temperature rise before the power and ripple current is calculated.
- The effects shown herein are based on measured data from a multiple part sample of the parts in question.
- Ripple capability of this device will be factored by thermal resistance (Rth) created by circuit traces (addi affects of all parameters involved, including the specified tolerances applied to capacitance and unspecified variations of ESR, ESL, and leakage resistance. The peak voltages generated in the "Temperature Rise vs. Combined Ripple Currents" plot are calculated for each frequency and are not combined with voltages generated at any other
- harmonics.
- Please consult with the catalog or field applications engineer for maximum capability of the device in specific applications.

All product information and data (collectively, the "Information") are subject to change without notice.

KEMET K-SIM is designed to simulate behavior of components with respect to frequency, ambient temperature, and DC bias levels. The responses shown represent the typical response for each part type. Specific responses may vary, depending on manufacturing variation effects of all parameters involved, including the specified tolerances applied to capacitance and unspecified variations of ESR, ESL, and leakage resistance.

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If you have any questions please contact K-SIM.

单击下面可查看定价,库存,交付和生命周期等信息

>>KEMET(基美)

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