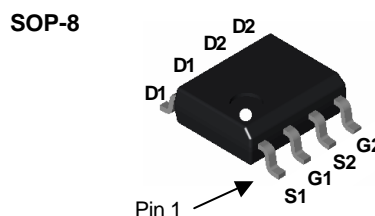
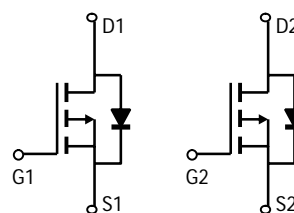


**4953** Dual P-Channel -30V(D-S) MOSFET

$V_{(BR)DSS}$	$R_{DS(on)MAX}$	$I_D$
-30V	0.059Ω@-10V	-5.3A
	0.089Ω@-4.5V	



**Equivalent Circuit**



**MARKING**



**General FEATURE**

- TrenchFET Power MOSFET
- Lead free product is acquired
- Surface mount package

**APPLICATION**

- Load Switch for Portable Devices
- DC/DC Converter

**Maximum ratings ( $T_a=25^{\circ}C$  unless otherwise noted)**

Parameter	Symbol	Value	Unit
Drain-Source Voltage	$V_{DS}$	-30	V
Gate-Source Voltage	$V_{GS}$	±20	
Continuous Drain Current	$I_D$	-5.3	A
Pulsed Drain Current	$I_{DM}$	-20	
Maximum Power Dissipation	$P_D$	2.0	W
Thermal Resistance from Junction to Ambient( $t \leq 5s$ )	$R_{\theta JA}$	125	$^{\circ}C/W$
Junction Temperature	$T_J$	150	$^{\circ}C$
Storage Temperature	$T_{stg}$	-55 ~+150	

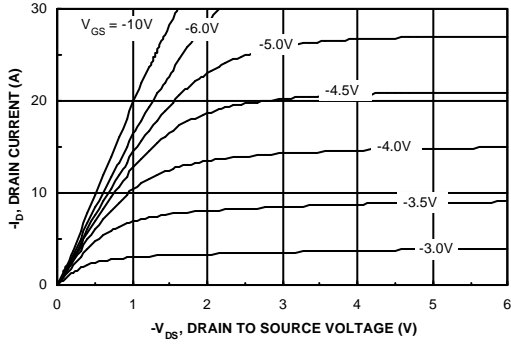
**Electrical Characteristics**  $T_A = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
<b>Off Characteristics</b>						
$BV_{DSS}$	Drain–Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = -250\ \mu\text{A}$	-30			V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = -24\text{ V}, V_{GS} = 0\text{ V}$			-1	$\mu\text{A}$
$I_{GSSF}$	Gate–Body Leakage, Forward	$V_{GS} = -20\text{ V}, V_{DS} = 0\text{ V}$			-100	nA
$I_{GSSR}$	Gate–Body Leakage, Reverse	$V_{GS} = 20\text{ V}, V_{DS} = 0\text{ V}$			100	nA
<b>On Characteristics</b>						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = -250\ \mu\text{A}$	-1	-1.5	-3	V
$R_{DS(on)}$	Static Drain–Source On–Resistance	$V_{GS} = -10\text{ V}, I_D = -5.3\text{ A}$		54	59	m $\Omega$
		$V_{GS} = -4.5\text{ V}, I_D = -4.2\text{ A}$		84	89	
$I_{D(on)}$	On–State Drain Current	$V_{GS} = -10\text{ V}, V_{DS} = -5.0\text{ V}$	-20			A
$g_{FS}$	Forward Transconductance	$V_{DS} = -5\text{ V}, I_D = -5\text{ A}$		10		S
<b>Dynamic Characteristics</b>						
$C_{iss}$	Input Capacitance	$V_{DS} = -15\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$		528		pF
$C_{oss}$	Output Capacitance			132		pF
$C_{rss}$	Reverse Transfer Capacitance			70		pF
<b>Switching Characteristics</b>						
$t_{d(on)}$	Turn–On Delay Time	$V_{DD} = -15\text{ V}, I_D = -1\text{ A},$ $V_{GS} = -10\text{ V}, R_{GEN} = 6\ \Omega$		7		ns
$t_r$	Turn–On Rise Time			13		ns
$t_{d(off)}$	Turn–Off Delay Time			14		ns
$t_f$	Turn–Off Fall Time			9		ns
$Q_g$	Total Gate Charge	$V_{DS} = -15\text{ V}, I_D = -5\text{ A},$ $V_{GS} = -5\text{ V}$		6.0	9	nC
$Q_{gs}$	Gate–Source Charge			2.2		nC
$Q_{gd}$	Gate–Drain Charge			2.0		nC
<b>Drain–Source Diode Characteristics and Maximum Ratings</b>						
$I_S$	Maximum Continuous Drain–Source Diode Forward Current				-1.3	A
$V_{SD}$	Drain–Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = -2.6\text{ A}$		-0.8	-1.2	V

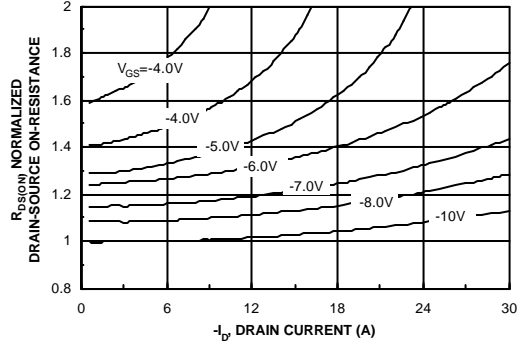
**Notes:**

1.  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.

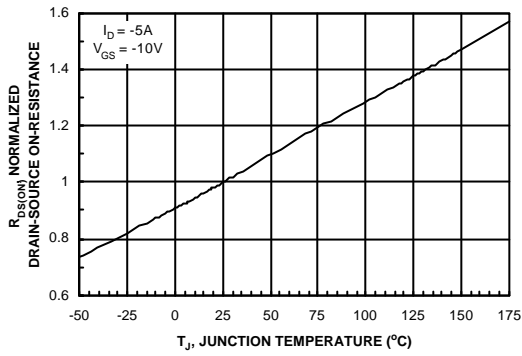
**Typical Characteristics**



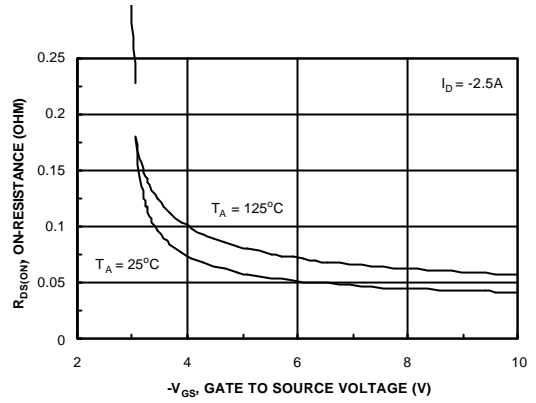
**Figure 1. On-Region Characteristics.**



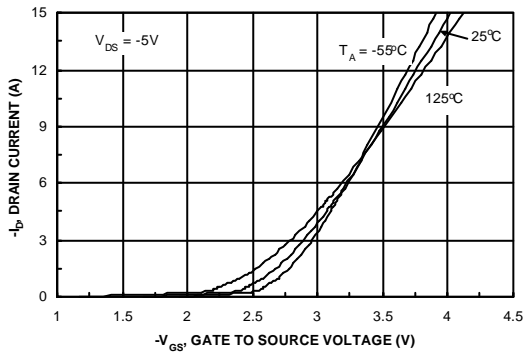
**Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.**



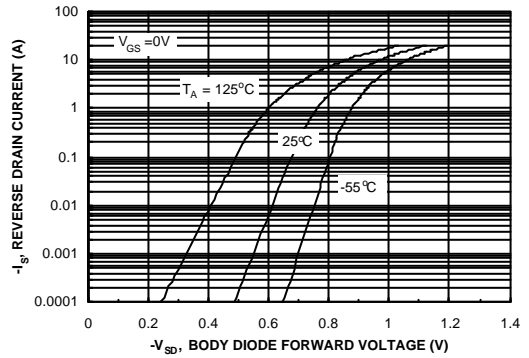
**Figure 3. On-Resistance Variation with Temperature.**



**Figure 4. On-Resistance Variation with Gate-to-Source Voltage.**

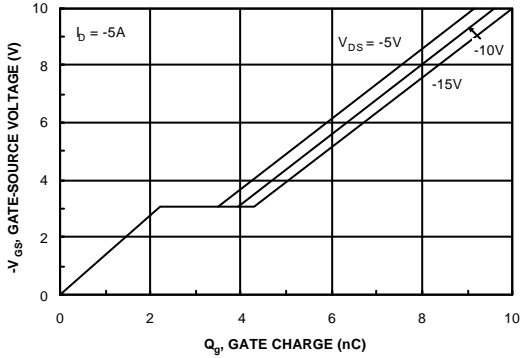


**Figure 5. Transfer Characteristics.**

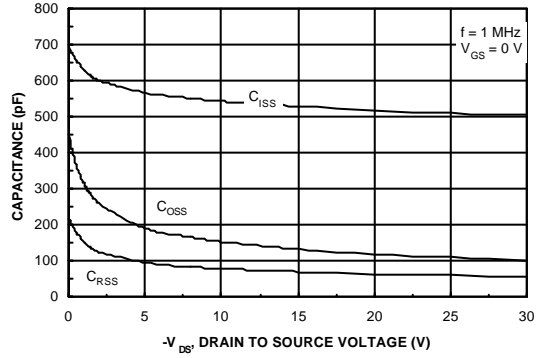


**Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.**

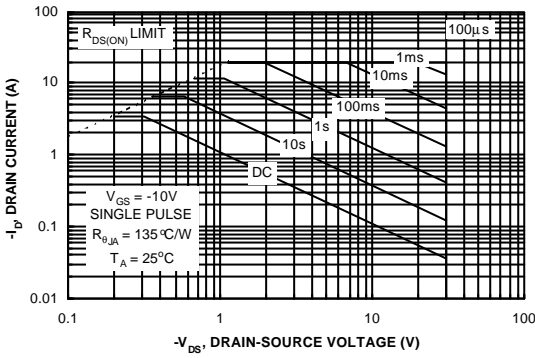
**Typical Characteristics**



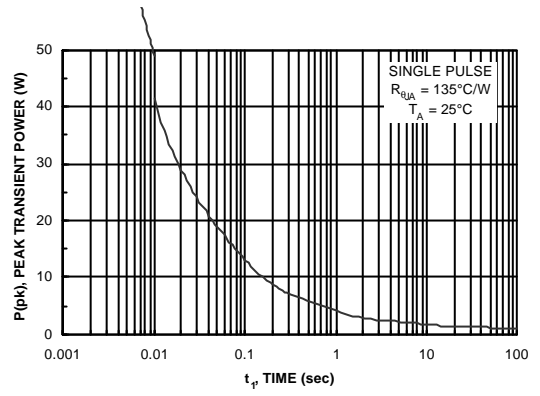
**Figure 7. Gate Charge Characteristics.**



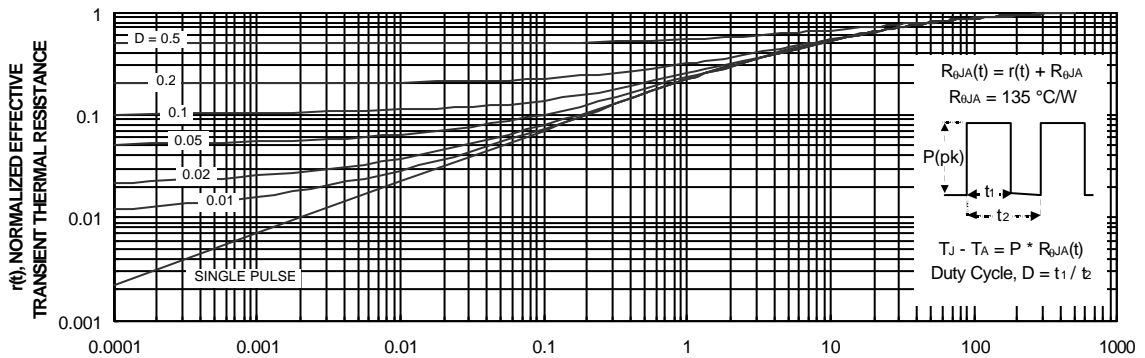
**Figure 8. Capacitance Characteristics.**



**Figure 9. Maximum Safe Operating Area.**



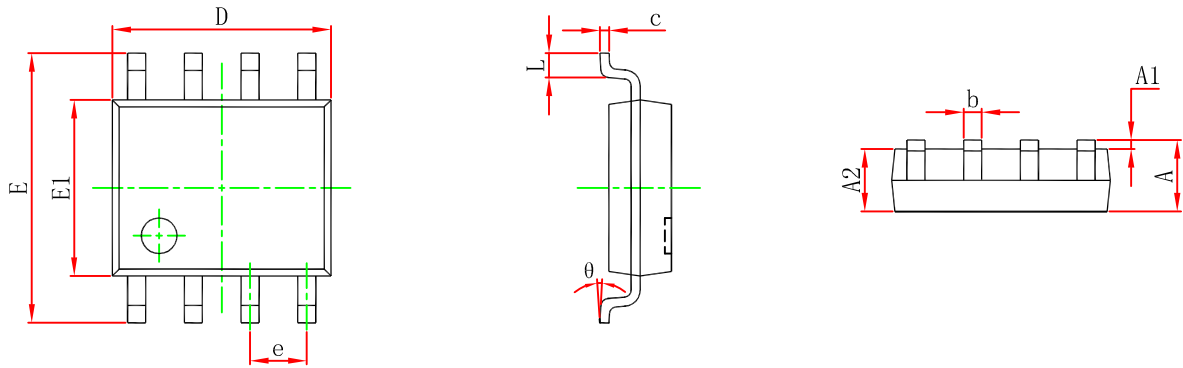
**Figure 10. Single Pulse Maximum Power Dissipation.**



**Figure 11. Transient Thermal Response Curve.**

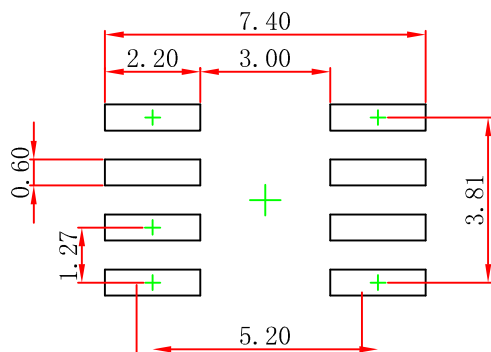
Thermal characterization performed using the conditions described in Note 1c. Transient thermal response will change depending on the circuit board design.

**SOP8 Package Outline Dimensions**



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.800	5.000	0.189	0.197
e	1.270 (BSC)		0.050 (BSC)	
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

**SOP8 Suggested Pad Layout**



- Note:
1. Controlling dimension: in millimeters.
  2. General tolerance:  $\pm 0.05\text{mm}$ .
  3. The pad layout is for reference purposes only.

单击下面可查看定价，库存，交付和生命周期等信息

[>>KUU\(永裕泰\)](#)