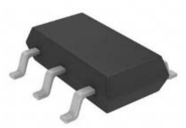
32V, 2A, 520KHz, Synchronous, Step-Down Converter

LA1312C

Overview

The LA1312C is an easy to use synchronous step-down Buck converter. Which integrated low on resistance high-side and low-side power MOSFETs . The LA1312C can deliver 2A output current efficiently with constant on time (COT) control for fast loop response.



SOT23-6L

The LA1312C achieves high power conversion efficiency over a wide load range.

The LA1312C has built-in protection features, such as cycle-by-cycle current limit, hiccup mode short-circuit protection, FB open short protection and thermal shutdown in case of excessive power dissipation. The LA1312C is available in a space-saving SOT23-6L package.

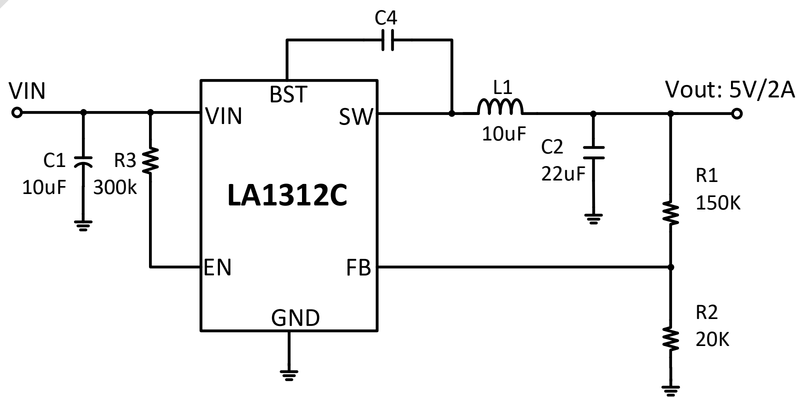
Features

- 4.5V to 32V Wide Input Range
- 2A Continuous Output Current
- 135mΩ/85mΩ Internal Power MOSFETs
- Constant On Time Control for Fast Loop Response
- 520KHz Switching Frequency
- Forced PWM Mode Operation
- Support Up to 98% Large Range Duty Cycle
- Internal Soft Start
- Output Voltage Adjustable from 0.6V
- Support Pre-Biased Output Startup
- Full Protection, Over Current Protection and Hiccup, Output Over Voltage Protection, FB Open Short Protection, Over Temperature Protection
- Available in a SOT23-6L Package

Applications

- Surveillance Camera
- Home Appliance and Whitegoods
- Multi-functional Printer
- Automotive
- Industrial Control

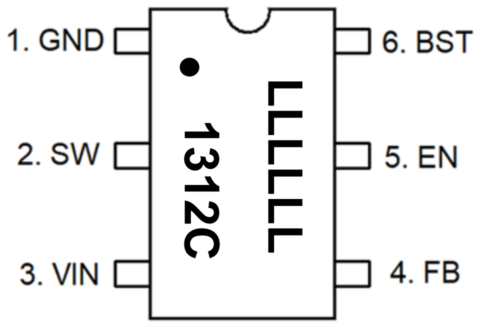
Typical Application



Package Mark and Order Information

Device	Package	Temperature range	Packaging Type	Purchase Contact
LA1312C	SOT23-6L	-40 to 150℃	T/R 3000pcs/roll	sales@latticeart.com

Pin Diagram

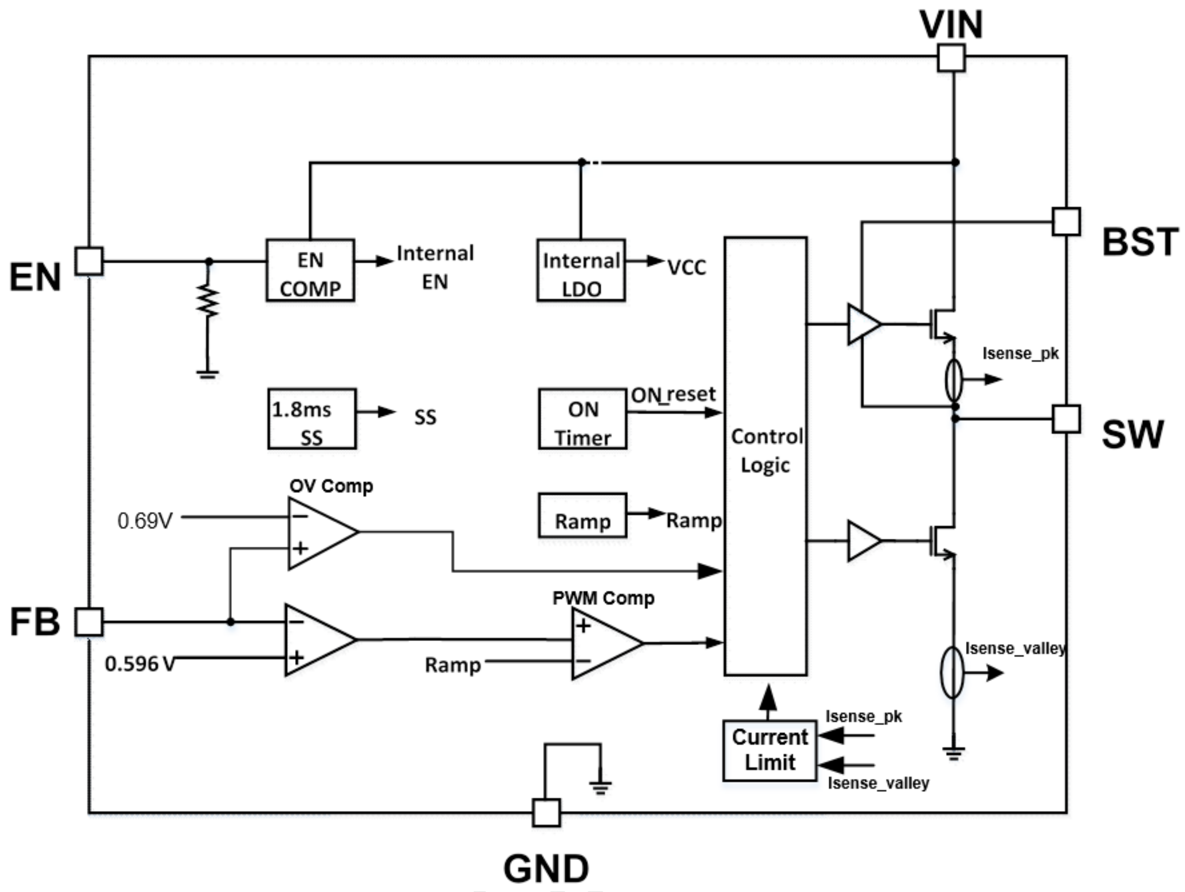


LLLLLL: Lot number
1312C: Product code

Pin Description

Pin No.	Symbol	Pin Description
1	GND	Power Ground terminal.
2	SW	Switching output of the convertor. Internally connected to source of the high-side FET and drain of the low-side FET. Connect to power inductor.
3	VIN	Supply input terminal to internal bias LDO and high-side FET. Connect to input supply and input bypass capacitors CIN. Input bypass capacitors must be directly connected to this pin and GND.
4	FB	Feedback input to the convertor. Connect a resistor divider to set the output voltage. Never short this terminal to ground during operation.
5	EN	Precision enable input to the convertor. Do not float. High = on, Low = off. Can be tied to VIN by a resistor. Precision enable input allows adjustable UVLO by external resistor divider.
6	BST	Bootstrap capacitor connection for high-side FET driver. Connect a high quality 100nF capacitor from this pin to the SW pin. For higher than 6V output application, recommend to put an 20Ω BST resistor.

Block Diagram



Absolute Maximum Ratings (Note 1)

T_A=25°C, unless otherwise specified.

Symbol	Definition	Ratings	Unit
V_{IN}	VIN to GND	-0.3~32	V
SW	SW to GND	-0.7 (-5V in 10ns)~VIN + 0.7	V
EN	Max Input current to EN pin	100(2)	uA
BST	BST to SW	-0.3~6	V
All Other Pins		-0.3~6	V
T_{STG}	Storage temperature	-55 to150	°C
T_j	Junction temperature	-40 to150	°C

Note 1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are not tested at manufacturing.

Note 2: For details on ENs ABS max rating, please refer to the Enable Control section.

Recommended Operating Conditions

Symbol	Definition	Ratings	Unit
BST	BST to SW	4~5	V
FB	FB to GND	0~1	V
EN	EN to GND	0~5	V
V_{IN}	VIN to GND	4.5~28	V
V_{OUT}	V_{OUT} to GND	0.6~VIN*D_{MAX}(3) or 13V	V
I_{OUT}	Max Continuous Output Current	0~2	A

Note 3: $D_{MAX} = T_{ON\_MAX}/(T_{ON\_MAX} + T_{OFF\_MIN})$. Typical value is 98%.

Thermal Resistance (Note 4)

Symbol	Definition	Ratings	Unit
$R_{\theta JC}$	Junction to case thermal resistance	21	°C/W
$R_{\theta JA}$	Junction to ambient thermal resistance	40	°C/W

Note 4: Measured on EV1312C-00B 2-Layer PCB.

ESD Rating

Symbol	Definition	Ratings	Unit
HBM	Human body model	± 2000	V
CDM	Changed device model	± 500	V

Electrical Characteristics

V_{IN}=12V, V_{EN}=2V, T_A=25°C, unless otherwise specified.

Symbol	Parameter	Condition	Min	Typ	Max	Units
VIN_{UVR}	VIN UVLO rising threshold		4.1	4.25	4.4	V
VIN_{UVF}	VIN UVLO falling threshold		3.85	4.0	4.15	V
VIN_{UV_hys}	VIN UVLO hysteresis			0.25		V
I_{QS}	Shutdown supply current	V_{EN} < 0.3V V_{IN}=12V		1	3	μA
I_Q	Quiescent supply current	No load, VFB = 1V, no switching		160		μA
LKG_{HS}	High-side leakage	V_{EN} = 0V, V_{SW} = 0V			1	μA
LKG_{LS}	Low-side leakage	V_{EN} = 0V, V_{SW} = 28V			1	μA
V_{FB}	Feedback voltage	T_A=25°C	584	596	608	mV
		T_J=-40°C ~ 125°C	581	596	611	mV
V_{FB_SHORT}	FB short threshold			280		mV
V_{FB_OV}	FB OV threshold			0.69	0.71	V
I_{LK_FB}	Feedback leakage	V_{EN} = 1V, V_{FB} = 2V			0.1	μA
R_{ON_HS}	High-side switch on resistance	V_{BST} - V_{SW} = 5V		135		mΩ
R_{ON_LS}	Low-side switch on resistance			85		mΩ
I_{LIM_LS}	Low-side Current limit	T_J=-40°C ~ 125°C	2.3	2.9	3.5	A
I_{LIM_HS}	High-side Current limit	T_J=-40°C ~ 125°C	3.6	4.8	5.8	A
I_{LIM_NOCP}	Negative Current limit	T_J=-40°C ~ 125°C	-2.4	-2	-1.6	A
T_{SS}	Soft-start time	V_{FB} from 0% to 100%		1.8		ms
F_{SW}	Oscillator frequency		440	520	600	KHz
T_{ON_MIN}	Minimum switch on time (5)			80		ns
T_{OFF_MIN}	Minimum switch off time (5)			120		ns
T_{ON_MAX}	Maximum switch on time		5.2	6.4		μs
V_{EN_R}	Enable rising threshold	Low to high	1.1	1.2	1.3	V
V_{EN_F}	Enable falling threshold	High to low	0.9	1	1.1	V
V_{EN_Hys}	Enable Threshold Hysteresis			0.2		V
R_{EN}	Enable input resistor			1500		kΩ

Electrical Characteristics

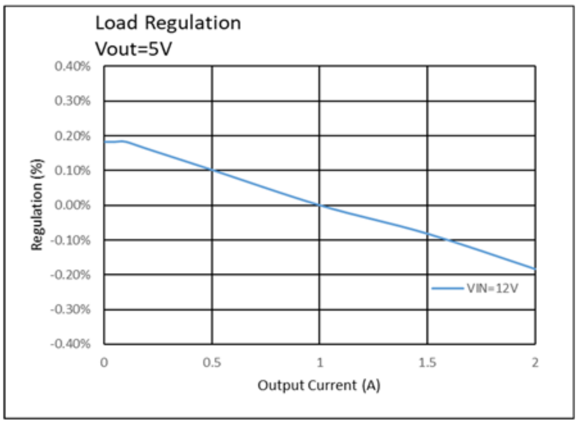
V_{IN}=12V, V_{EN}=2V, T_A=25°C, unless otherwise specified.

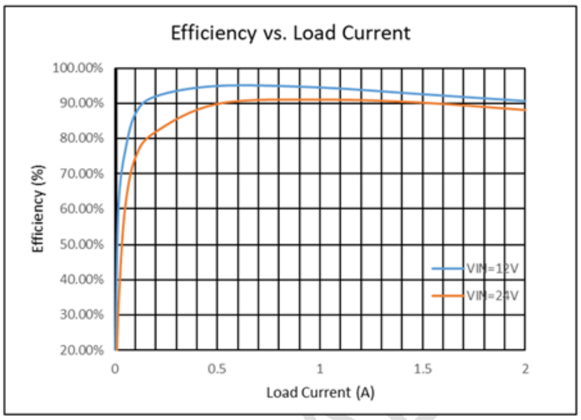
Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{OTP_R}	Thermal shutdown (5)			150		°C
T_{OTP_F}	Thermal shutdown hysteresis (5)			130		°C
T_{OTP_Hys}	OTP hysteresis			20		°C

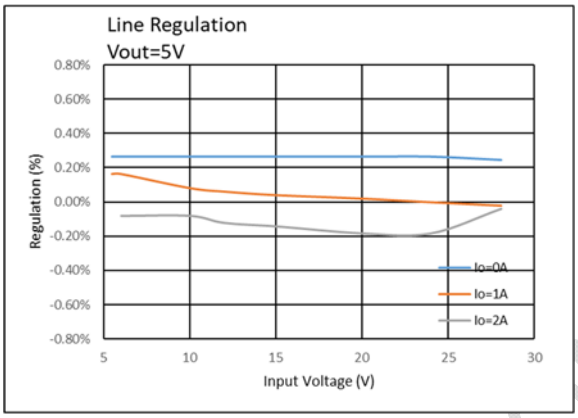
Note 5: Not tested in production and derived from bench characterization.

Typical Performance Characteristic

V_{OUT}=5V: V_{IN} = 12V, C1 = 10μF, C2 = 22μF, L1 = 10μH, and T_A = +25°C, unless otherwise noted.





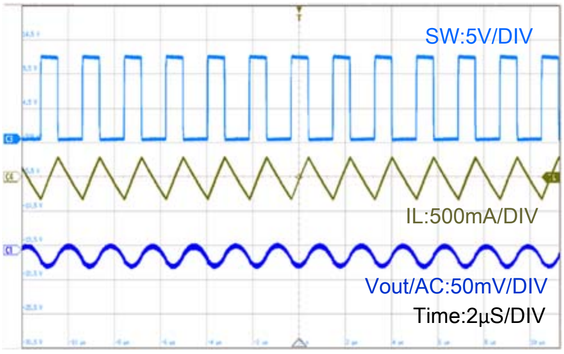


Typical Performance Characteristic *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, C1 = 10µF, C2 = 22µF, L1 = 10µH, and T_A = +25°C, unless otherwise noted.

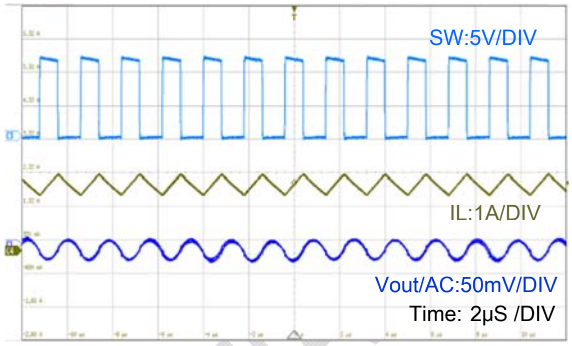
Output Voltage Ripple

IOUT = 0A



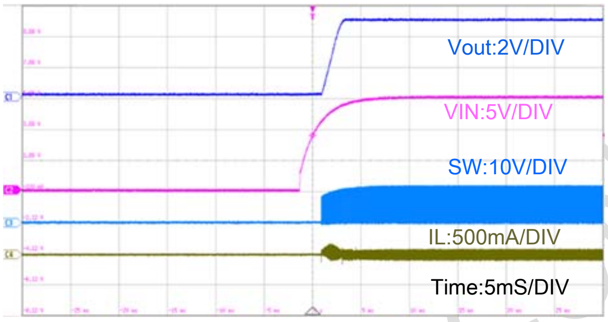
Output Voltage Ripple

IOUT = 2A



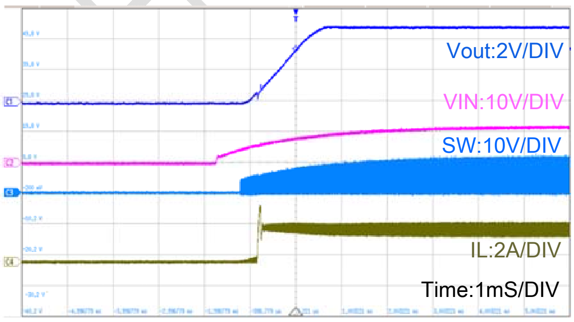
Start-Up through V_{IN}

IOUT = 0A



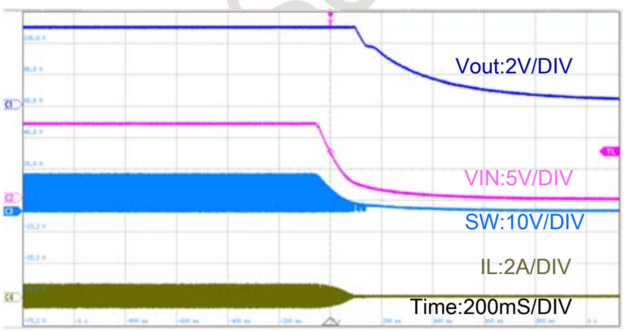
Start-Up through V_{IN}

IOUT = 2A



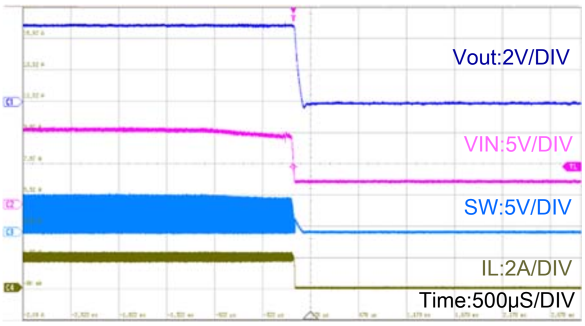
Shut-Down through V_{IN}

IOUT = 0A



Shut-Down through V_{IN}

IOUT = 2A

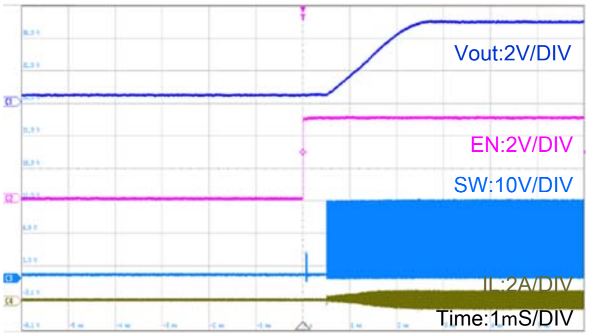


Typical Performance Characteristic *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, C1 = 10µF, C2 = 22µF, L1 = 10µH, and T_A = +25°C, unless otherwise noted.

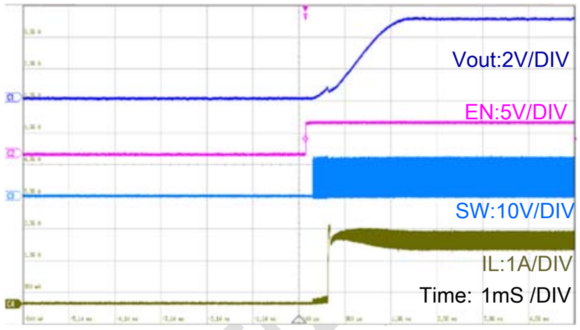
Start-Up through EN

IOUT = 0A



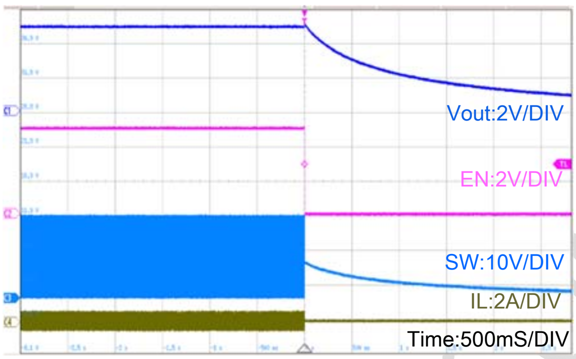
Start-Up through EN

IOUT = 2A



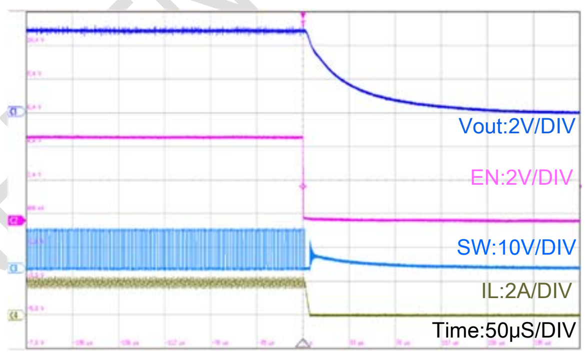
Shut-Down through EN

IOUT = 0A



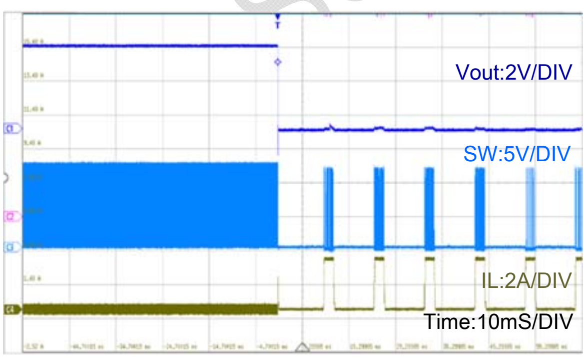
Shut-Down through EN

IOUT = 2A



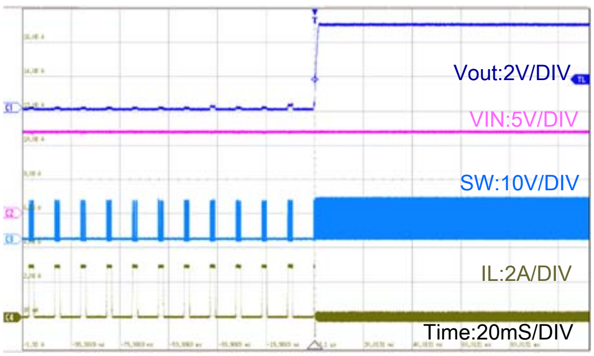
Short-Circuit Entry

IOUT = 0A



Short-Circuit Recovery

IOUT = 0A

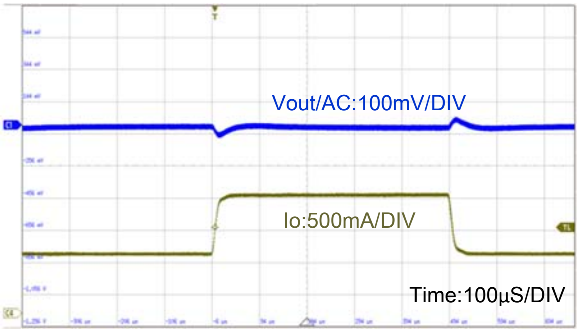


Typical Performance Characteristic *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, C1 = 10µF, C2 = 22µF, L1 = 10µH, and T_A = +25°C, unless otherwise noted.

Load Transient

IOUT = 1A to 2A, 2.5A/us slew rate



Function Descriptions

Pulse-Width Modulation (PWM) Control

The LA1312C is fully integrated synchronous rectified step-down switch mode converter. Constant-on-time (COT) control is employed to provide fast transient response and easy loop stabilization. At the beginning of each cycle, the high-side MOSFET (HS-FET) is turned ON when the feedback voltage (VFB) is below the reference voltage (VREF), which indicates insufficient output voltage. The ON period is determined by both the output voltage and input voltage to make the switching frequency fairy constant over input voltage range.

After the ON period elapses, the HS-FET is turned off, or becomes OFF state. It is turned ON again when VFB drops below VREF. By repeating operation this way, the converter regulates the output voltage. The integrated low- side MOSFET (LS-FET) is turned on when the HS-FET is in its OFF state to minimize the conduction loss. To avoid shoot-through, a dead-time (DT) is internally generated between HS-FET off and LS-FET on, or LS-FET off and HS-FET on.

An internal compensation is applied for COT control to make a more stable operation even when ceramic capacitors are used as output capacitors, this internal compensation will then improve the jitter performance without affect the line or load regulation.

Enable (EN) Control

Enable (EN) is a digital control pin that turns the regulator on and off. Drive EN high to turn on the regulator. Drive EN low to turn off the regulator. An internal 1.5MΩ resistor from EN to GND allows EN to be floated to shut down the chip. EN is clamped internally using a 6V Zener diode. EN can connected to VIN directly by a resistor.

The EN Pin can connect to VIN by a pull-up resistor, but EN input current need below 100uA. For example, if VIN=24V, the IZener=(24-6)/RPULL-UP<100uA, So, RPULL-UP>180KΩ.

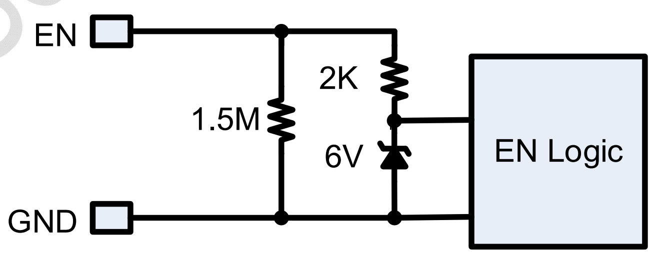


Figure 1: Zener Diode between EN and GND

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The LA1312C UVLO comparator monitors the input voltage. The UVLO rising threshold is 4.25V typical, while its falling threshold is 4.0 V typical.

Internal Soft Start (SS)

Soft start (SS) prevents the converter output voltage from overshooting during start-up. When the chip starts, the internal circuitry generates a soft-start voltage (VSS) that ramps up from 0V to 1V. When SS is below REF, SS overrides REF, so the error amplifier uses SS as the reference. When SS exceeds REF, the error amplifier uses REF as the reference. The SS time is set to 1.8ms internally.

Over-Current Protection (OCP) and Short Circuit Protection (SCP)

The LA1312C has a valley current-limit control. During LS-FET on, the inductor current is monitored. If the current is higher than valley current limit, the high side will not turn on again. The output voltage drops until VFB is below the under voltage (FB UV) threshold. Once UV is triggered, the LA1312C enters hiccup mode to restart the part periodically.

During OCP, the device attempts to recover from the over-current fault with hiccup mode. In hiccup mode, the chip disables the output power stage, discharges the soft start, and attempts to soft start again automatically. If the over-current condition still holds after the soft start ends, the device repeats this operation cycle until the over-current condition is removed and the output rises back to regulation levels. OCP is a non-latch protection.

Output Over-Voltage Protection (OVP)

The LA1312C has the output sinking mode to regulate the output voltage to the target value when VFB is higher than 100%*REF but below the over-voltage protection (OVP) threshold. During output sinking mode, the LS-FET remains on until the -2A negative current limit is triggered. After LS-FET is turned off the HS-FET will turn on and turn off again until the ON-timer elapses. The LA1312C repeat this operation until VFB drops back to 100%*REF. If VFB voltage rise above the OVP threshold, LA1312C will stops switching. If VFB falls below the OVP threshold, LA1312C will start switching again.

Pre-Bias Start-Up

The LA1312C is designed for monotonic start-up into pre-biased loads. If the output is pre-biased to a certain voltage during start-up, the BST voltage is refreshed and charged, and the voltage on the soft start is charged as well. If the BST voltage exceeds its rising threshold voltage and the soft-start voltage exceeds the sensed output voltage at FB, the part works normally.

Large Duty Cycle Operation

LA1312C will automatically extend the on time to support the application when VIN is close to VOUT. The on time extend circuit will be triggered when Toff min time is reached. The LA1312C can support up to 98% maximum duty cycle.

Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the silicon die temperature exceeds 150°C, the entire chip shuts down. When the temperature falls below its lower threshold (typically 130°C), the chip is enabled again.

Application Information

Setting the Output Voltage

The LA1312C output voltage can be set by the external resistor dividers. The reference voltage is fixed at 0.596V. The feedback network is shown below Figure.

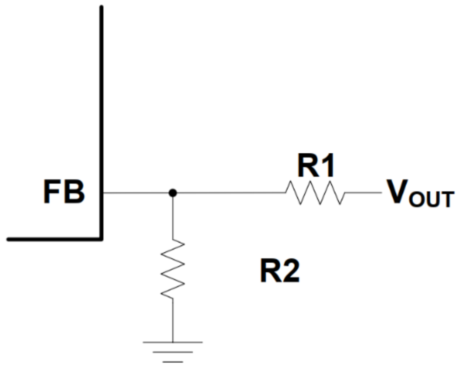


Figure 2 Feedback Network

Choose R_1 and R_2 using Equation:

$$V_{OUT} = V_{FB}(R_1 + R_2) / R_2$$

Selecting the Inductor

An inductor is necessary for supplying constant current to the output load while being driven by the switched input voltage. A larger-value inductor results in less ripple current and a lower output ripple voltage, but also has a larger physical footprint, higher series resistance, and lower saturation current.

For most designs, the inductance value can be derived from Equation:

$$L = \frac{V_{OUT} * (V_{IN} - V_{OUT})}{V_{IN} * \Delta I_L * F_{OSC}}$$

Where ΔIL is the inductor ripple current.

Choose the inductor ripple current to be approximately 30% of the maximum load current. The maximum inductor peak current can be calculated with Equation:

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2}$$

Table 1 lists the recommended feedback resistor values for common output voltages.

Table 1: Resistor Selection for Common Output Voltages[6]

VOUT (V)	R1 (kΩ)	R2 (kΩ)	L (μH)	C_{OUT}(uF)
5	110	15	10	22
3.3	68	15	10	22

Note 6: For a detailed design circuit, please refer to the Typical Application Circuits.

Selecting the Output Capacitor

The output capacitor (C2, C3) maintains the DC output voltage ripple. Use ceramic, tantalum, or low-ESR electrolytic capacitors. For best results, use low ESR capacitors to keep the output voltage ripple low. The output voltage ripple can be estimated with Equation:

$$\Delta V_{OUT}=\frac{V_{OUT}}{F_{OSC}*L}*(1-\frac{V_{OUT}}{V_{IN}})*(R_{ESR}+\frac{1}{8*F_{OSC}*C_{OUT}})$$

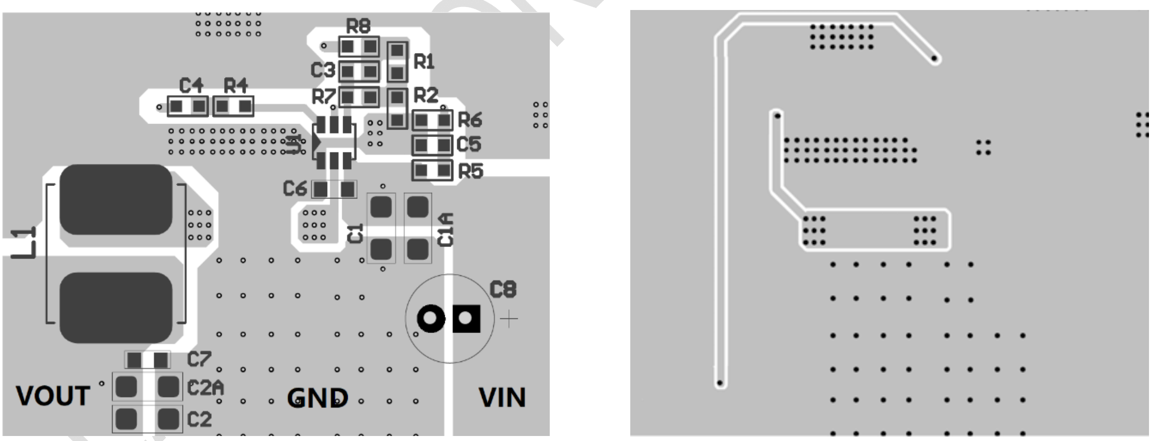
Where L is the inductor value, and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

The characteristics of the output capacitor also affect the stability of the regulation system. The LA1312C can be optimized for a wide range of capacitance and ESR values.

PCB Layout Guidelines

Efficient layout of the switching power supplies is critical for stable operation. For the high frequency switching converter, poor layout design may cause poor line or load regulation and stable issues. For best results, refer to below figure and follow the guidelines below.

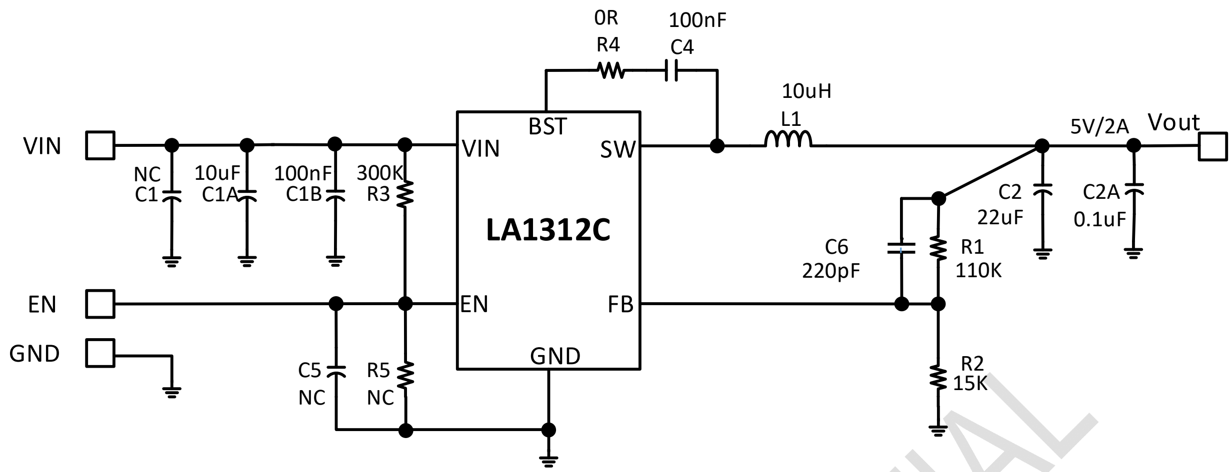
- Place the input capacitor as close to VIN and GND as possible.
- Place the external feedback resistors as close to FB as possible.
- Keep the switching node (such as SW, BST) far away from the feedback network.
- Add a grid of thermal vias under the exposed pad to improve thermal conductivity.



Top Layer **Bottom Layer**

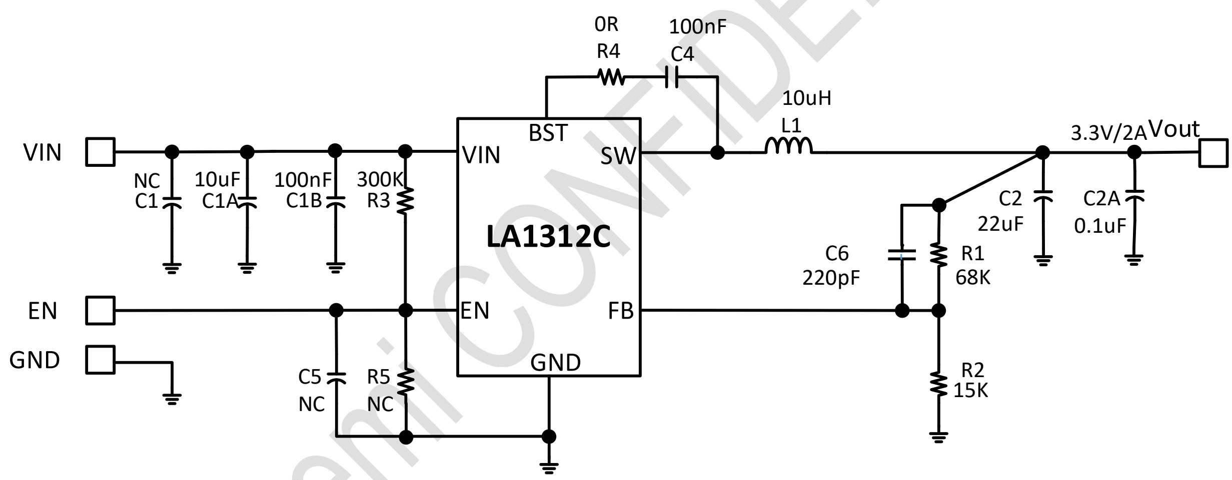
Figure 3 Recommend PCB Layout

Typical Application Circuits



Note: C6 is optional for better transient performance.

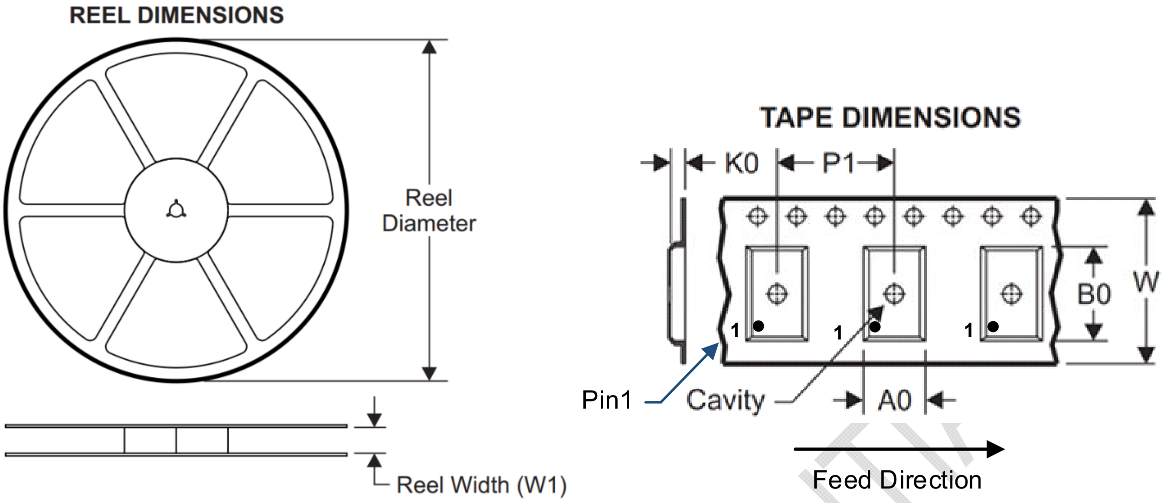
Figure 4 VIN=12V, VOUT=5V/2A



Note: C6 is optional for better transient performance.

Figure 5 VIN=12V, VOUT=3.3V/2A

Tape and Reel Information

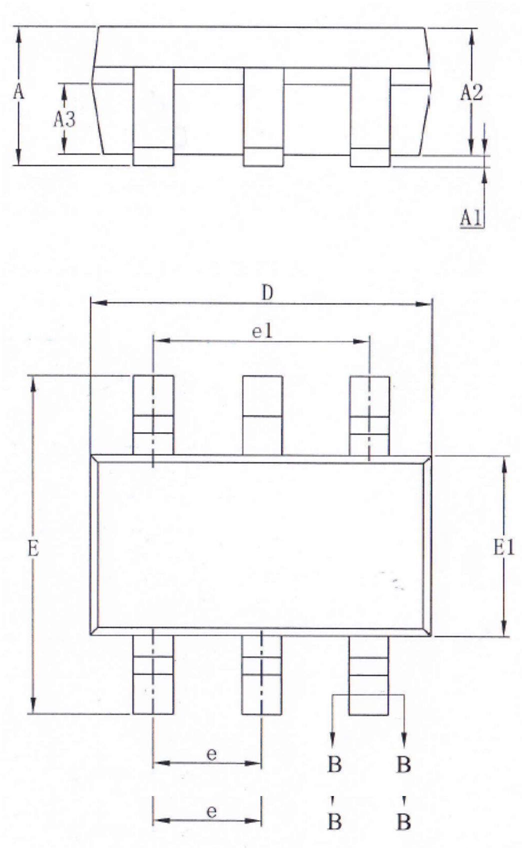


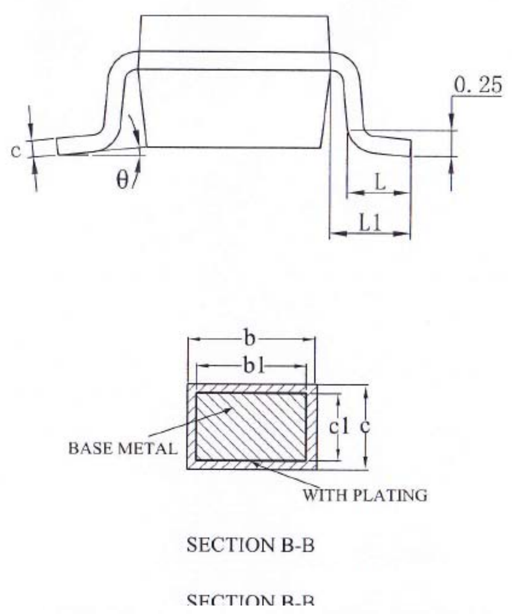
Information

Device	Package Type	Pins	SPQ	Real Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)
LA1312C	SOT23-6L	6	3000	178	9	3.25	3.3	1.38	4	8

Detail Package Outline Drawing

Package type: SOT23-6L





SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.25
A1	0.04	—	0.10
A2	1.00	1.10	1.20
A3	0.60	0.65	0.70
b	0.33	—	0.41
b1	0.32	0.35	0.38
c	0.15	—	0.19
c1	0.14	0.15	0.16
D	2.82	2.92	3.02
E	2.60	2.80	3.00
E1	1.50	1.60	1.70
e	0.95BSC		
e1	1.90BSC		
L	0.30	—	0.60
θ	0	—	8°