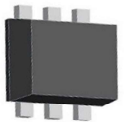
16V, 2A, 800KHz, Synchronous Step-Down Converter

LA1212S

Overview

The LA1212S is a high frequency (800KHz) step-down switching regulator with integrated internal power MOSFETs. It achieves 2A of continuous output current from a 4.5V to 16V input voltage range with excellent load and line regulation. The LA1212S uses synchronous-mode operation for higher efficiency over the output current-load range.



SOT563

The constant-on-time (COT) control operation provides very fast transient response, easy loop design, and very tight output regulation. Full protection features include short-circuit protection (SCP), over-current protection (OCP), under-voltage protection (UVP), and thermal shutdown. The LA1212S is available in an ultra-small SOT563 package and requires a minimal number of readily available, standard, external components.

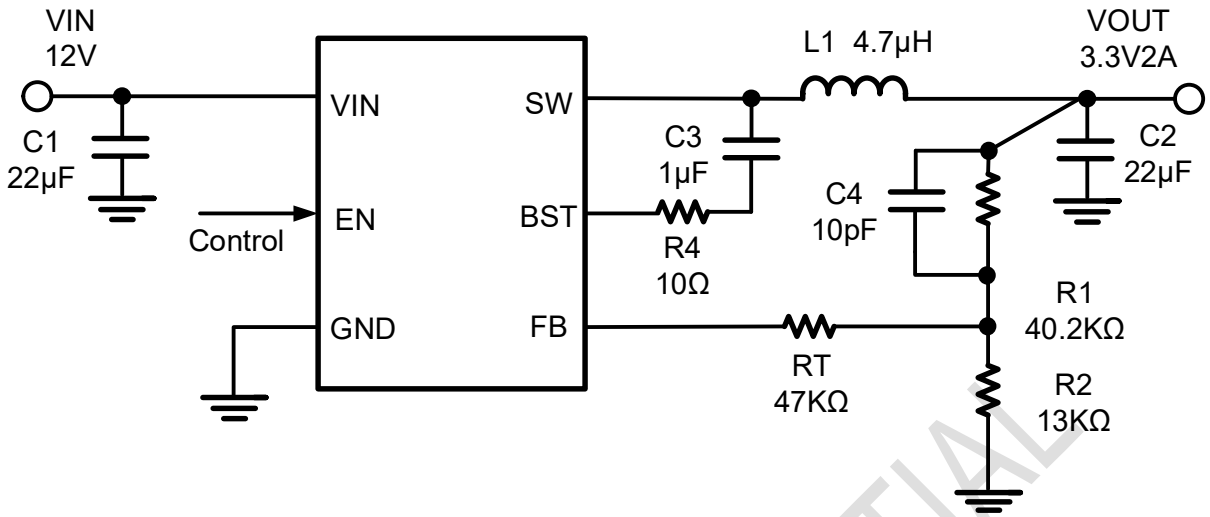
Features

- 4.5V to 16V Input Voltage Range Supporting
- 20V Absolute Maximum Rating
- 2A Continuous Output Current
- Output Adjustable from 0.8V
- 130mΩ and 75mΩ Internal Power MOSFETs
- 190μA Low I_Q
- 800KHz Switching Frequency
- High-Efficiency Synchronous Mode Operation
- Internal Soft Start (SS)
- Over-Current Protection (OCP) and Hiccup
- Power-Save Mode (PSM) at Light Load
- Thermal Shutdown
- Available in a SOT563 Package

Applications

- Surveillance Cameras
- Digital STB and OTT Box
- Broadband Products
- TV and Monitors
- General Purpose

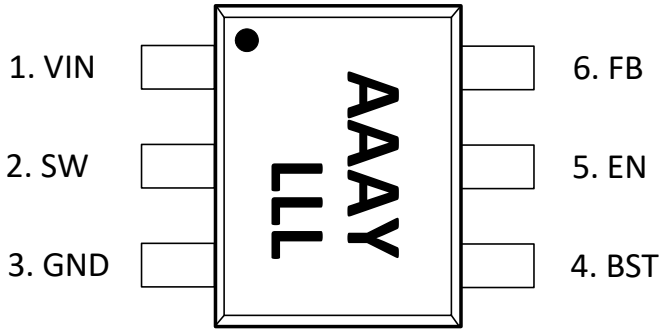
Typical Application



Package Mark and Order Information

Device	Package	Temperature range	Packaging Type	Purchase Contact
LA1212S	SOT563	-40 to 125 °C	T/R 5000pcs/roll	sales@latticeart.com

Pin Diagram

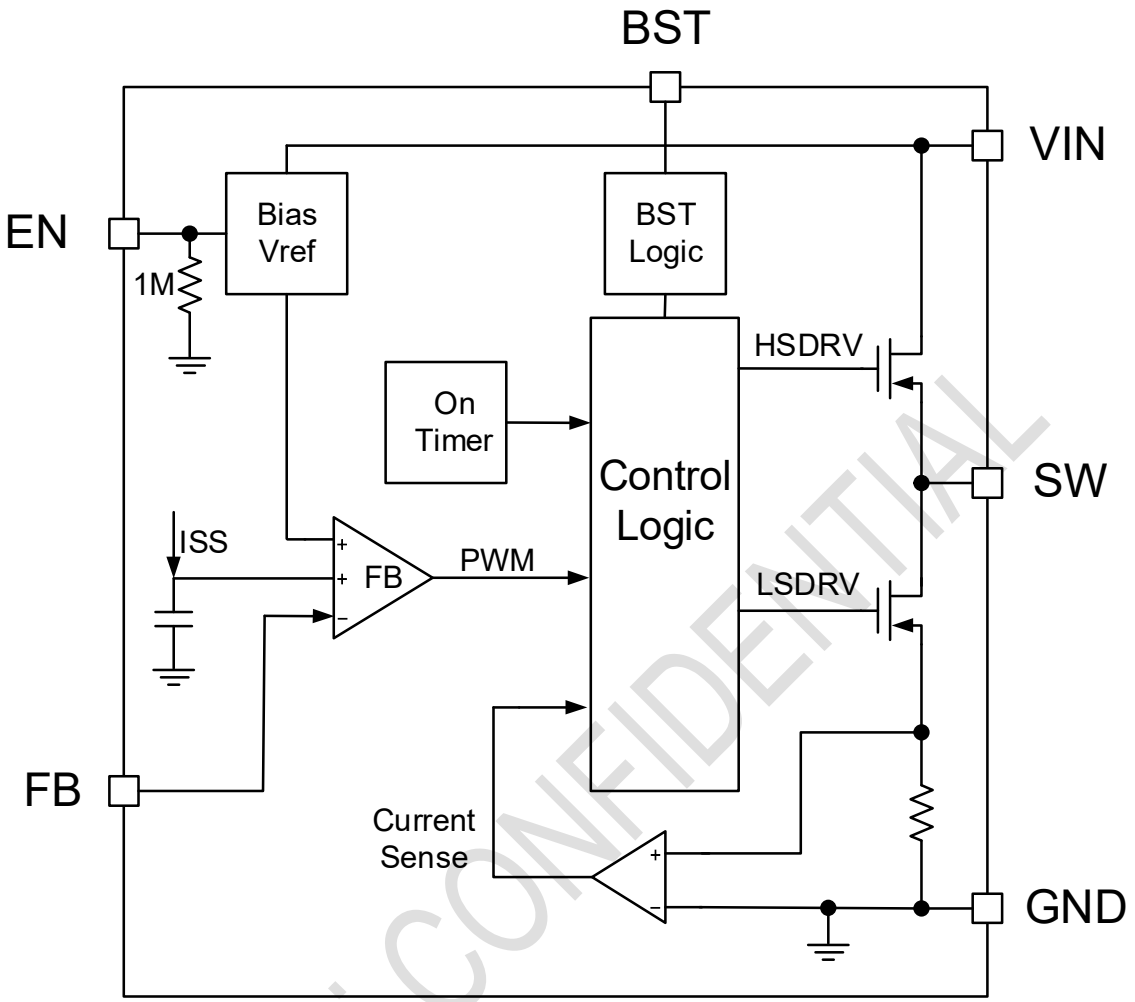


AAA: Product code of LA1212S
Y: Year code
LLL: Lot Number

Pin Description

Pin No.	Symbol	Pin Description
1	VIN	**Supply voltage.** The LA1212S operates from a 4.5V to 16V unregulated input. A decoupling capacitor is needed to prevent large voltage spikes from appearing at the input.
2	SW	**Output switching node.**
3	GND	**System ground.** GND is the reference ground of the regulated output voltage. GND requires extra care during the PCB layout. Connect GND with copper traces and vias .
4	BST	**Bootstrap.** Connect a 1μF BST capacitor and a resistor between SW and BST to form a floating supply across the high-side switch driver.
5	EN	**On/off control.**
6	FB	**Feedback.** Connect FB to the tap of an external resistor divider from the output to GND to set the output voltage. The frequency foldback comparator lowers the oscillator frequency when the FB voltage drops below 600mV to prevent current-limit runaway during a short circuit fault.

Block Diagram



Absolute Maximum Ratings (note 1)

T_A=25^{0}C, unless otherwise specified.

Symbol	Definition	Ratings	Unit
VIN	VIN to GND	-0.3~20	V
V_{SW}	SW to GND	-0.6 (-6.5 for <10ns) to VIN+0.3 (21 for <10ns)	V
V_{BST}	BST to SW	V_{SW} + 5	V
V_{EN}(2)	EN to GND	-0.3~5	V
All other pins		-0.3~5	V
I_{load}	Max output current	2	A
T_{STG}	Storage temperature	-65 to +150	°C

Note 1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are not tested at manufacturing.

Note 2: For details on ENs ABS max rating, please refer to the Enable Control section.

Recommended Operating Conditions

Symbol	Definition	Ratings	Unit
VIN	VIN to GND	4.5~16	V
SW	SW to GND	-0.6~16	V
GND	IC ground	0	V
BST	BST to SW	2.2~3.3	V
EN	EN to GND	0~5	V
FB	FB to GND	0~1	V
T_j	Junction temperature	-40 to +125	°C

Thermal Resistance

Symbol	Definition	Ratings	Unit
$R_{\theta JC}$	Junction to case thermal resistance	60	°C/W
$R_{\theta JA}$	Junction to ambient thermal resistance	130	°C/W

Electrical Characteristics

V_{IN}=12V, V_{EN}=2V, T_A=25°C, unless otherwise specified.

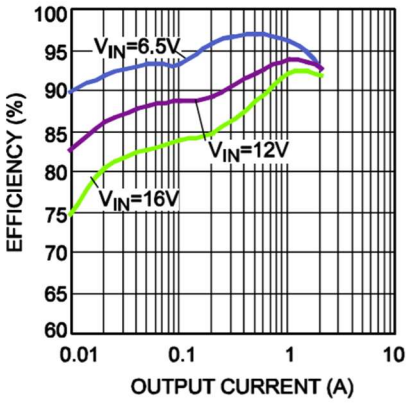
Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{FB}	Feedback voltage	T_J=25°C	0.795	0.807	0.819	V
		T_J= -40°C to +125°C	0.791	0.807	0.823	
I_{FB}	Feedback current			10	100	nA
V_{UV_TH}	FB UV threshold (H to L)	Hiccup entry		75%		V_{REF}
D_{Hiccup}(3)	Hiccup Duty Cycle			25%		
R_{ON_HSmos}	High-side switch on resistance	V_{BST-SW}=3.3V		130		mΩ
R_{ON_LSmos}	Low-side switch on resistance			75		mΩ
SW_{LKG}	Switch leakage current	V_{EN} = 0V, V_{SW}=12V			10	μA
VIN_{UVU}	VIN UVLO Up threshold		3.7	4.1	4.18	V
VIN_{UV_Hys}	VIN UVLO hysteresis			330		mV
I_{LIM}	Valley Current limit		1.8	2.4	3.8	A
I_{ZCD}	ZCD	V_{OUT}=3.3V, L=4.7μH,I_O=0A	-150	-20	150	mA
T_{ON_MIN}(3)	Minimum On time			45		ns
T_{OFF_MIN}(3)	Minimum Off time			180		ns
T_{SS}	Soft-start time	FB from 10% to 90%	1	1.4	2	ms
F_{SW}	Oscillator frequency	V_{FB}=0.75V	600	800	1000	KHz
I_Q	Quiescent supply current	V_{EN}=2V, V_{FB}=0.85V, VIN=12V	0.16	0.19	0.23	mA
I_{SD}	Shutdown current	V_{EN}=0V			10	μA
V_{EN_R}	Enable rising threshold	Low to high	1.14	1.2	1.26	V
V_{EN_Hys}	Enable Threshold hysteresis			0.1		V
I_{EN}	Enable input current	V_{EN} = 2V		2		μA
T_{OTP_R}(3)	Thermal shutdown			150		°C
T_{OTP_Hys}(3)	Thermal hysteresis			20		°C

NOTE 3: Guaranteed by design and engineering sample characterization.

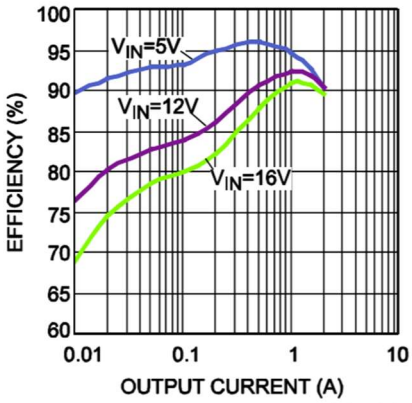
Typical Performance Characteristic

V_{OUT}=3.3V: V_{IN} = 12V, C_{OUT} = 22μF, L1 = 4.7μH, and T_A = +25°C, unless otherwise noted.

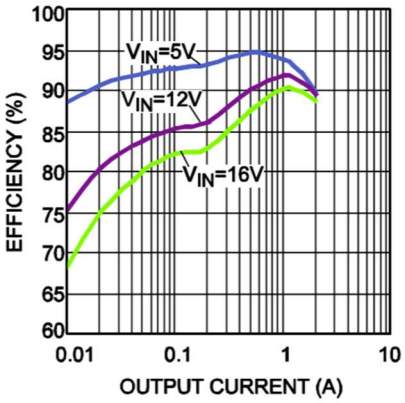
Efficiency
V_{OUT}=5V, L=4.7μH, DCR=24.5mΩ



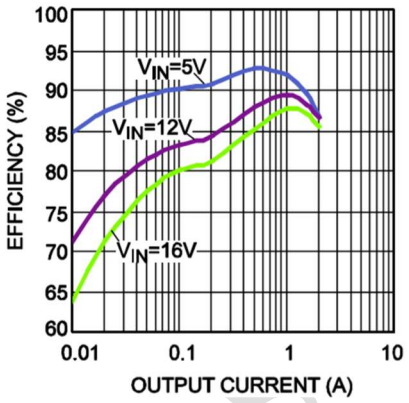
Efficiency
V_{OUT}=3.3V, L=4.7μH, DCR=24.5mΩ



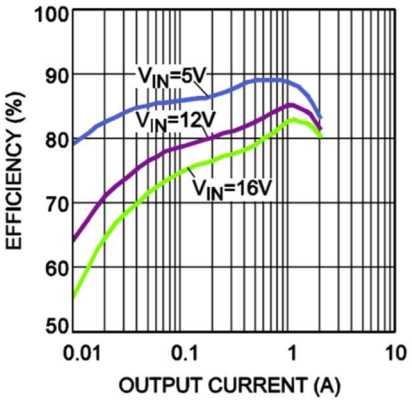
Efficiency
V_{OUT}=2.5V, L=3.3μH, DCR=9mΩ



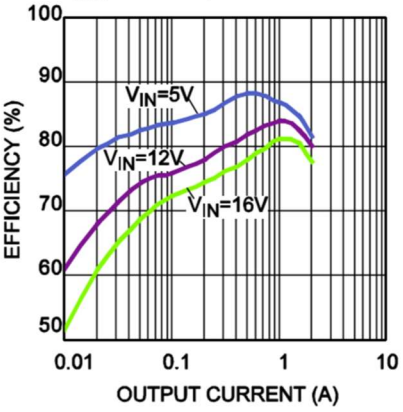
Efficiency
V_{OUT}=1.8V, L=2.2μH, DCR=11.4mΩ



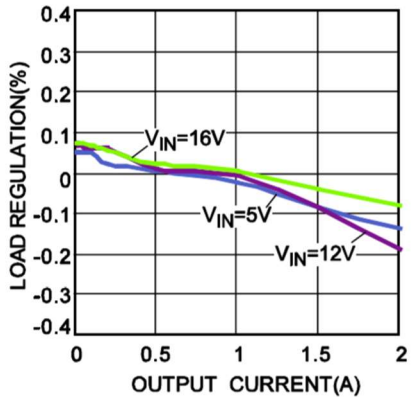
Efficiency
V_{OUT}=1.2V, L=1.5μH, DCR=4.3mΩ



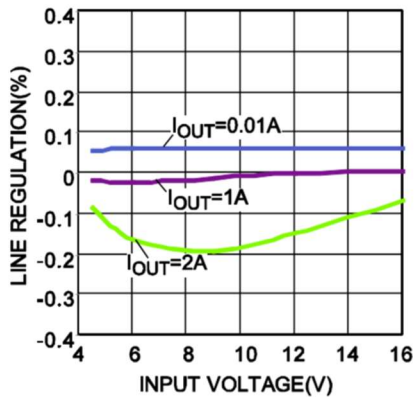
Efficiency
V_{OUT}=1V, L=1.5μH, DCR=4.3mΩ



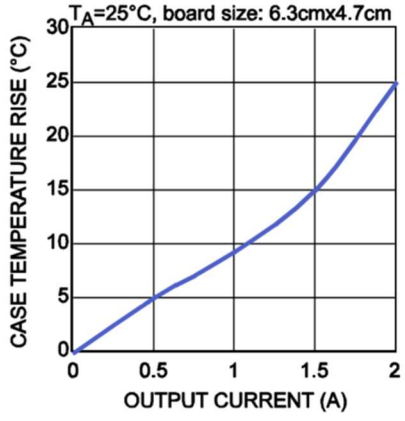
Load Regulation
I_{OUT}= 0.01A to 2A



Line Regulation
V_{IN}= 4.5V to 16V

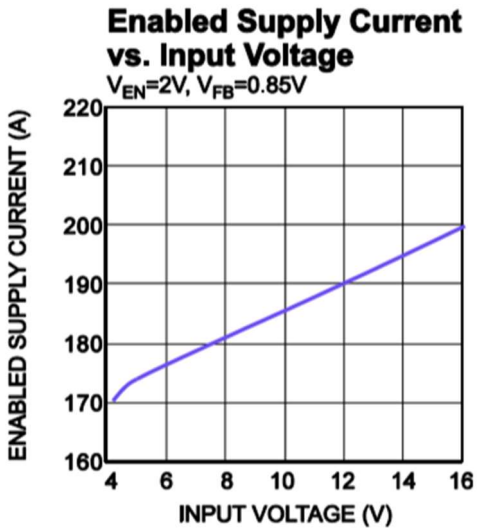


Case Temperature Rise vs. Output Current
T_A=25°C, board size: 6.3cmx4.7cm



Typical Performance Characteristic

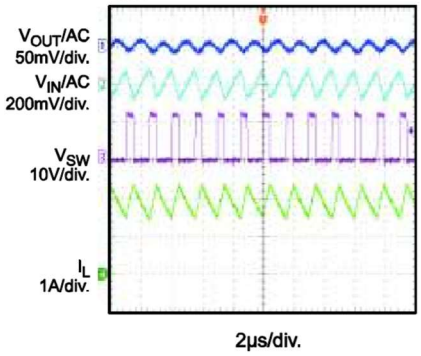
V_{OUT}=3.3V: V_{IN} = 12V, C_{OUT} = 22µF, L1 = 4.7µH, and T_A = +25°C, unless otherwise noted.



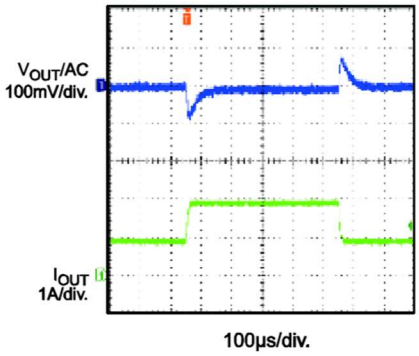
Typical Performance Characteristic

V_{OUT}=3.3V: V_{IN} = 12V, C_{OUT} = 22μF, L1 = 4.7μH, and T_A = +25°C, unless otherwise noted.

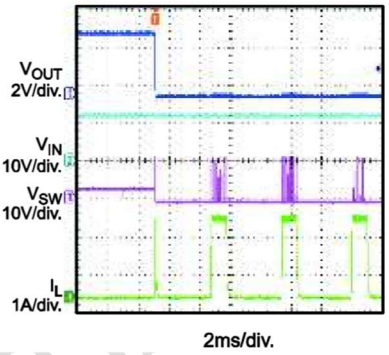
Input/Output Ripple
I_{OUT}=2A



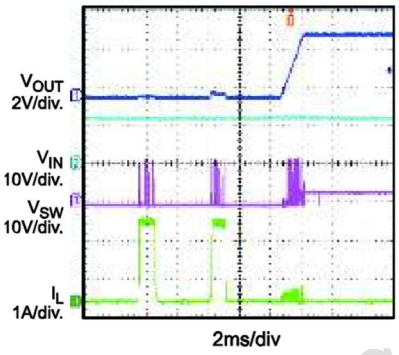
Transient Response
I_{OUT}=1A to 2A, 2.5A/μs



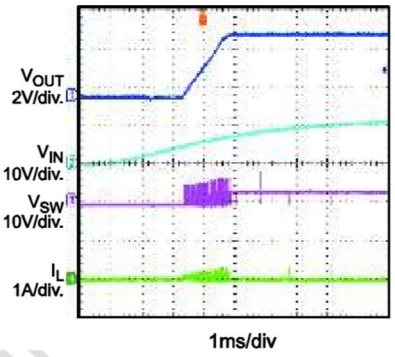
Short-Circuit Entry
I_{OUT}=0A



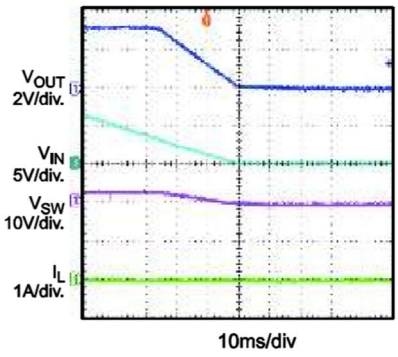
Short-Circuit Recovery
I_{OUT}=0A



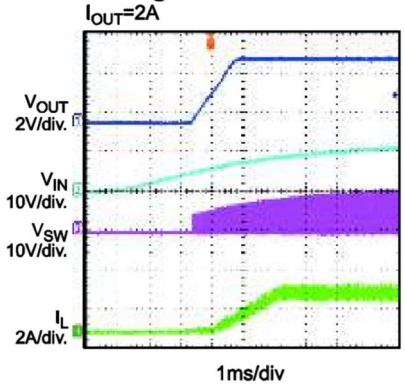
Start-Up through Input Voltage
I_{OUT}=0A



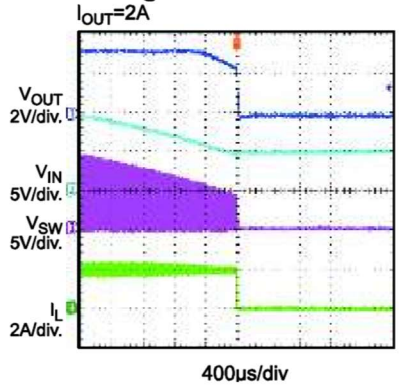
Shutdown through Input Voltage
I_{OUT}=0A



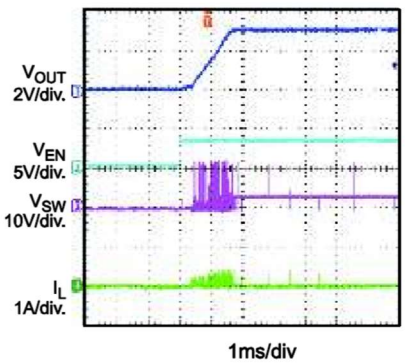
Start-Up through Input Voltage
I_{OUT}=2A



Shutdown through Input Voltage
I_{OUT}=2A



Start-Up through Enable
I_{OUT}=0A



Function Descriptions

1. Continuous conduction mode

Continuous conduction mode (CCM) is when the output current is high and the inductor current is always above zero amps. The low side MOSFET (LS-FET) is turned on when the HS-FET is in its off state to minimize conduction loss. There is a dead short between the input and GND if both the HS-FET and LS-FET are turned on at the same time. This is called a shoot-through. To avoid shoot-through, a deadtime is generated internally between the HSFET off and LS-FET on period or LS-FET off and HS-FET on period.

When the LA1212S works in pulse-frequency modulation (PFM) mode during light-load operation, the LA1212S reduces the switching frequency automatically to maintain high efficiency, and the inductor current drops almost to zero. When the inductor current reaches zero, the low-side driver goes into tristate (Hi-Z). The output capacitors discharge slowly to GND through R1 and R2. When VFB drops below V_{REF}, the HS-FET is turned on. This operation improves device efficiency greatly when the output current is low.

Light-load operation is also called skip mode because the HS-FET does not turn on as frequently as it does during heavy-load conditions. The frequency at which the HS-FET turns on is a function of the output current. As the output current increases, the current modulator regulation time period becomes shorter, the HS-FET turns on more frequently, and the switching frequency increases in turn. The output current reaches the critical level when the current modulator time is zero and can be determined with Equation (1):

$$I_{OUT} = \frac{(V_{IN}-V_{OUT})\times V_{OUT}}{2\times F_{OSC}\times L\times V_{IN}} \quad \cdots\cdots (1)$$

The device reverts to pulse-width modulation (PWM) mode once the output current exceeds the critical level. Afterward, the switching frequency remains fairly constant over the output current range.

2. Enable (EN) Control

EN is a digital control pin that turns the regulator on and off. Drive EN high to turn on the regulator. Drive EN low to turn off the regulator. An internal 1MΩ resistor from EN to GND allows EN to float to shut down the IC.

EN is clamped internally using a 2.8V series Zener diode. Connecting the EN input through a pull-up resistor to VIN limits the EN input current to less than 100μA to prevent damaging the Zener diode. For example, when connecting a 100kΩ pull-up resistor to 12V VIN, I_{Zener} = (12V - 2.8V) / (100kΩ + 35kΩ) = 68μA.

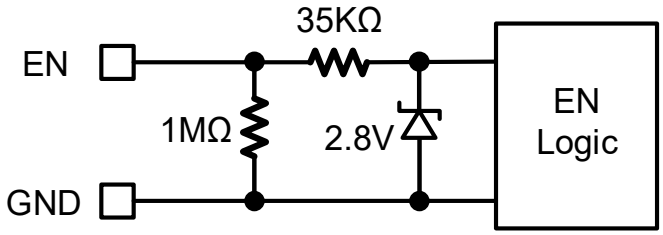


Figure 1: Zener Diode between EN and GND

3. Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The LA1212S UVLO comparator monitors the input voltage. The UVLO rising threshold is about 4.1V, while its falling threshold is consistently 3.77V.

4. Soft Start

Soft start prevents the converter output voltage from overshooting during start-up. When the chip starts up, the internal circuitry generates a soft-start voltage (SS) that ramps up from 0V to 1.2V. When SS is lower than REF, SS overrides REF so the error amplifier uses SS as the reference. When SS exceeds REF, the error amplifier uses REF as the reference. The SS time is set to 1.4ms internally.

5. Pre-Bias Start-Up

The LA1212S is designed for monotonic start-up into pre-biased loads. If the output is pre-biased to a certain voltage during start-up, the BST voltage is refreshed and charged, and the voltage on the soft start is not charged when BST voltage low. If the BST voltage exceeds its rising threshold voltage and the soft-start voltage exceeds the sensed output voltage at FB, the LA1212S starts working normally.

6. Short circuit protection (SCP) and Over current protection (OCP)

The LA1212S has a valley current-limit control. During the LS-FET on state, the inductor current is monitored. When the sensed inductor current reaches the valley current limit, the Low side limit comparator turns over. The device enters over-current protection (OCP) mode, and the HS-FET waits until the valley current limit disappears before turning on again. Meanwhile, the output voltage drops until VFB is below the under-voltage (UV) threshold (typically 75% below the reference). Once UV is triggered, the LA1212S enters hiccup mode to restart the part periodically.

During OCP, the device attempts to recover from over-current fault with hiccup mode. The chip disables the output power stage, discharges the soft start, and attempts to soft start again automatically. If the over-current condition still remains after the soft start ends, the device repeats this operation cycle until over-current condition is removed, and the output rises back to regulation level. OCP is a non-latch protection.

7. Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the silicon die temperature exceeds 150°C, the entire chip shuts down. When the temperature falls below its lower threshold (typically 130°C), the chip is enabled again.

8. Floating Driver and Bootstrap Charging

An external bootstrap capacitor powers the floating power MOSFET driver. This floating driver has its own UVLO protection with a rising threshold of 2.2V and a hysteresis of 150mV. VIN regulates the bootstrap capacitor voltage internally through D1, M1, C3, L1, and C2 (see Figure 2). If VIN - VSW exceeds 3.3V, U2 regulates M1 to maintain a 3.3V BST voltage across C3.

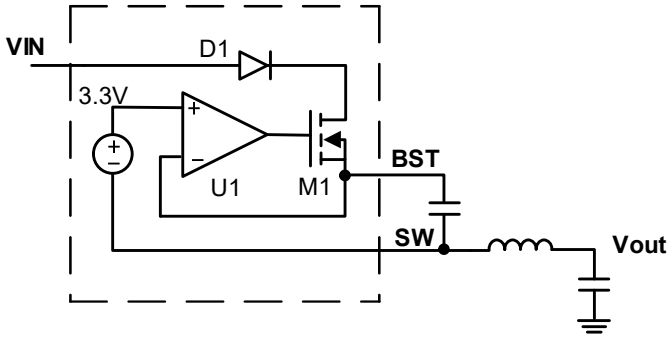


Figure 2: Internal Bootstrap Charger

Application Information

1. Setting the Output Voltage

An external resistor divider is used to set the output voltage. First, choose a value for R2. R2 should be chosen reasonably, since a small R2 leads to considerable quiescent current loss, while a large R2 makes FB noise-sensitive. R2 should be within 5 - 100kΩ. Typically, set the current through R2 to be between 5 - 30μA for a good balance between system stability and no-load loss. Then determine R1 with Equation (2):

$$R_1 = \frac{V_{OUT}-V_{REF}}{V_{REF}} \times R_2 \quad \cdots\cdots \quad (2)$$

The feedback circuit is shown in Figure 3.

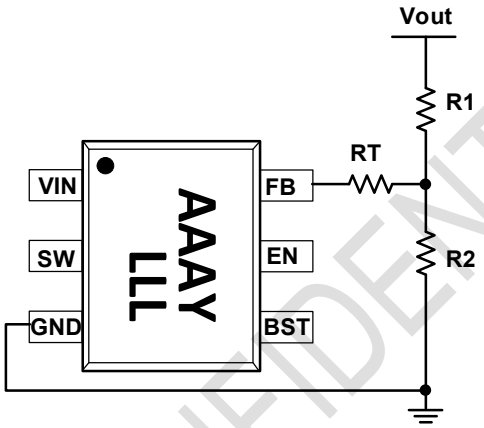


Figure 3: Feedback Network

Table 1 and Table 2 list the recommended parameters for common output voltages [3] .

V_{OUT}(V)	R1(KΩ)	R2(KΩ)	RT(KΩ)	L(μH)
5	40.2	7.68	47	4.7
3.3	40.2	13	47	4.7
2.5	40.2	19.1	62	3.3
1.8	40.2	32.4	75	2.2
1.5	40.2	45.3	86.6	2.2
1.2	40.2	82	105	1.5
1	20.5	84.5	160	1.5

Table 1: Parameters Selection for Common Output Voltages, C_{OUT} = 22μF

V_{OUT}(V)	R1(KΩ)	R2(KΩ)	RT(KΩ)	L(μH)
5	40.2	7.68	0	4.7
3.3	40.2	13	0	4.7
2.5	40.2	19.1	10	3.3
1.8	40.2	32.4	10	2.2
1.5	40.2	45.3	20	2.2
1.2	40.2	82	25	1.5
1	20.5	84.5	51	1.5

Table 2: Parameters Selection for Common Output Voltages, C_{OUT} = 22μF*2

NOTE 4: For a detailed design circuit, please refer to the Typical Application Circuits.

2. Selecting the Inductor

An inductor is necessary for supplying constant current to the output load while being driven by the switched input voltage. A larger-value inductor results in less ripple current and a lower output ripple voltage, but also has a larger physical footprint, higher series resistance, and lower saturation current. A good rule for determining the inductance value is to design the peak-to-peak ripple current in the inductor to be in the range of 30 - 40% of the maximum output current, and that the peak inductor current is below the maximum switch current limit. The inductance value can be calculated with Equation (3):

$$L = \frac{V_{OUT}}{F_{SW}\Delta I_L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad \cdots\cdots \quad (3)$$

Where ΔIL is the peak-to-peak inductor ripple current. The inductor should not saturate under the maximum inductor peak current. The peak inductor current can be calculated with Equation (4):

$$L_{LP} = I_{OUT} + \frac{V_{OUT}}{2F_{SW}L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad \cdots\cdots \quad (4)$$

3. Selecting the Input Capacitor

The input current to the step-down converter is discontinuous and therefore requires a capacitor to supply AC current to the step-down converter while maintaining the DC input voltage. Ceramic capacitors are recommended for the best performance and should be placed as close to VIN as possible. Capacitors with X5R and X7R ceramic dielectrics are recommended because they are fairly stable with temperature fluctuations. The capacitors must also have a ripple current rating greater than the maximum input ripple current of the converter. The input ripple current can be estimated with Equation (5):

$$I_{CIN} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad \cdots\cdots \quad (5)$$

The worst-case condition occurs at VIN = 2VOUT, shown in Equation (6):

$$I_{CIN} = \frac{I_{OUT}}{2} \quad \cdots\cdots \quad (6)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current. The input capacitance value determines the input voltage ripple of the converter. If there is an input voltage ripple requirement in the system, choose the input capacitor that meets the specification. The input voltage ripple can be estimated with Equation (7):

$$\Delta V_{IN} = \frac{I_{LOAD}}{F_{OSC}C_1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad \cdots\cdots \quad (7)$$

The worst-case condition occurs at VIN = 2VOUT, shown in Equation (8):

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{F_{SW}C_{IN}} \quad \cdots\cdots \quad (8)$$

4. Selecting the Output Capacitor

An output capacitor is required to maintain the DC output voltage. Ceramic or POSCAP capacitors are recommended. The output voltage ripple can be estimated with Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{OSC}L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(ESR + \frac{1}{8F_{OSC}C_{OUT}}\right) \quad \cdots\cdots \quad (9)$$

In the case of ceramic capacitors, the impedance at the switching frequency is

dominated by the capacitance. The output voltage ripple is caused mainly by the capacitance. For simplification, the output voltage ripple can be estimated with Equation (10):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8F_{OSC}^2 L_1 C_2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad \cdots\cdots \quad (10)$$

In the case of POSCAP capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated with Equation (11):

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{OSC} L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times ESR \quad \cdots\cdots \quad (11)$$

A larger output capacitor also can achieve a better load transient response, but be sure to consider the maximum output capacitor limitation in the design application. If the output capacitor value is too high, the output voltage cannot reach the design value during the softstart time and fails to regulate. The maximum output capacitor value (Co_max) can be limited approximately with Equation (12):

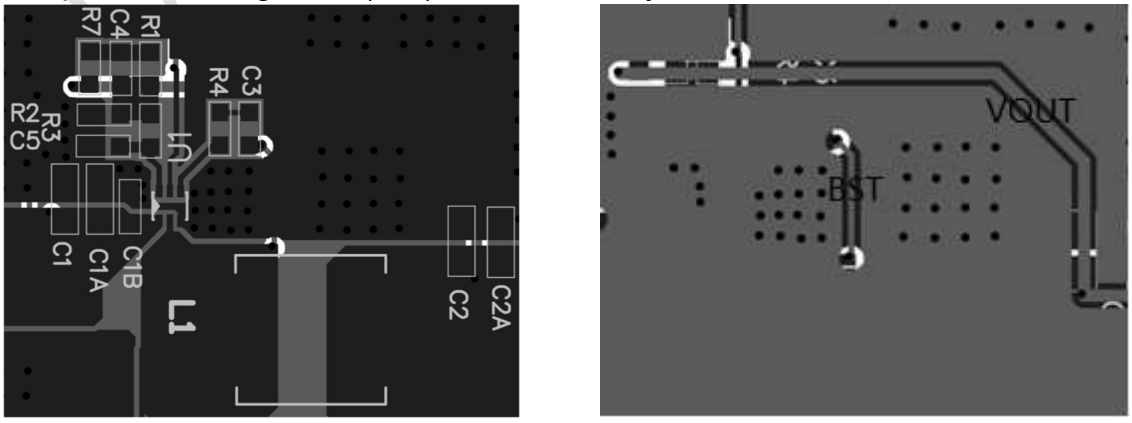
$$C_{O\_MAX} = \frac{(I_{LIM\_AVG} - I_{OUT})}{V_{OUT}} \times T_{SS} \quad \cdots\cdots \quad (12)$$

Where I_{LIM_AVG} is the average start-up current during the soft-start period, and Tss is the soft start time.

5. PCB Layout Guidelines

Efficient PCB layout of the switching power supplies is critical for stable operation. A poor layout design can result in poor line or load regulation and stability issues. For best results, refer to Figure 4 and follow the guidelines below.

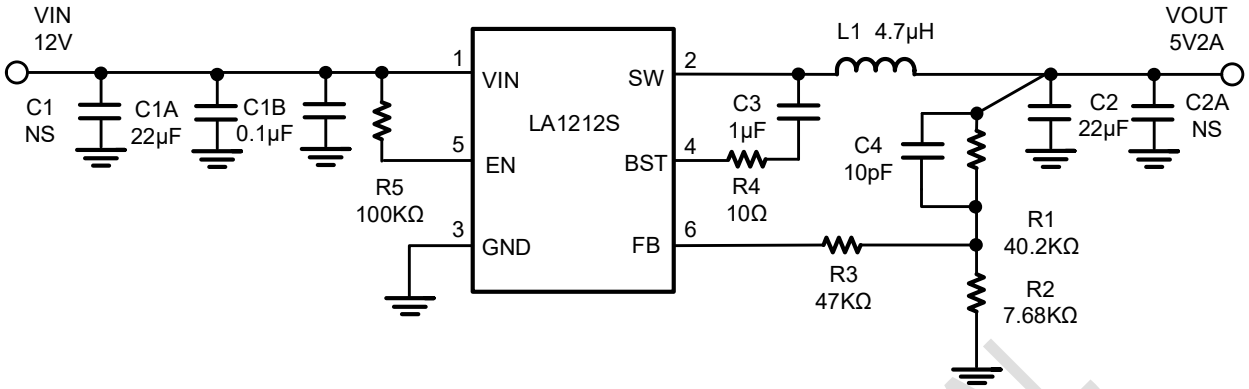
- Place the high-current paths (GND, VIN, and SW) very close to the device with short, direct, and wide traces.
- Place the input capacitor as close to VIN and GND as possible (within 1mm).
- Place the external feedback resistors next to FB.
- Keep the switching node (SW) short and away from the feedback network.



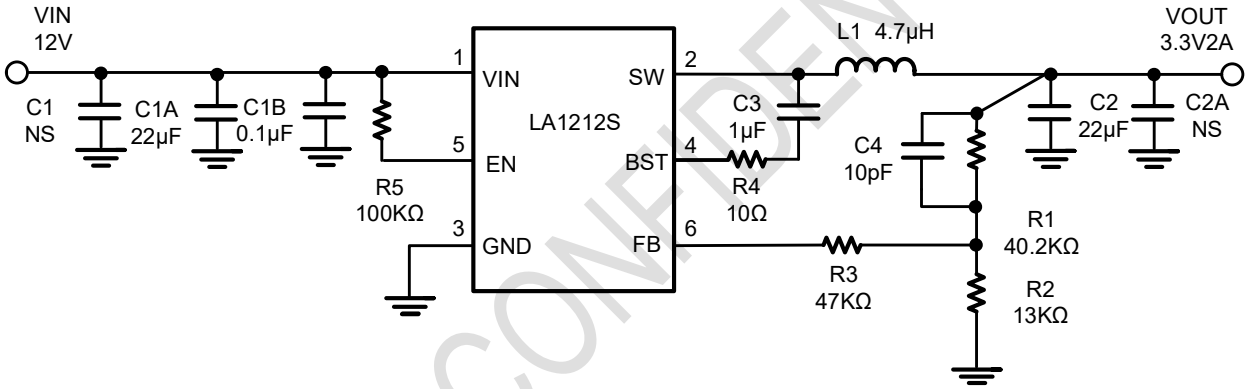
Top layer **Bottom layer**

Figure 4: Recommended Layout

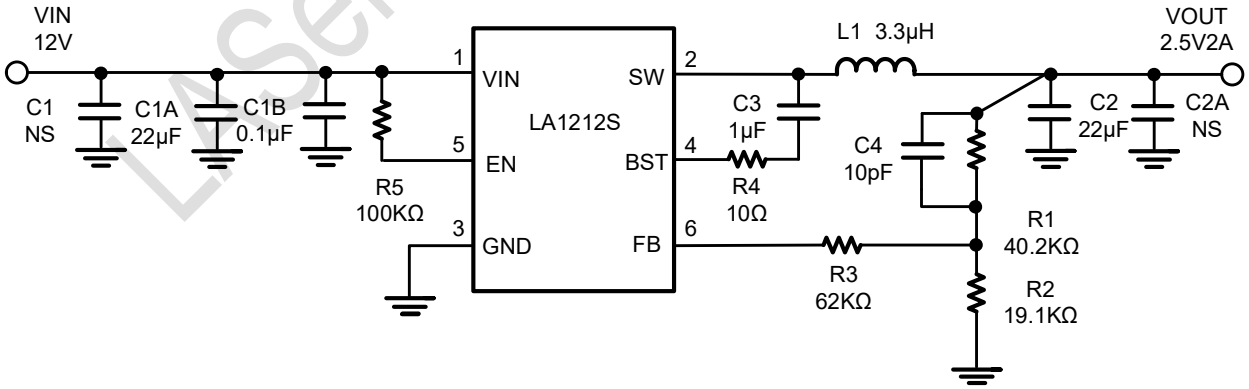
Typical Application Circuits



12VIN, 5V/2A Output

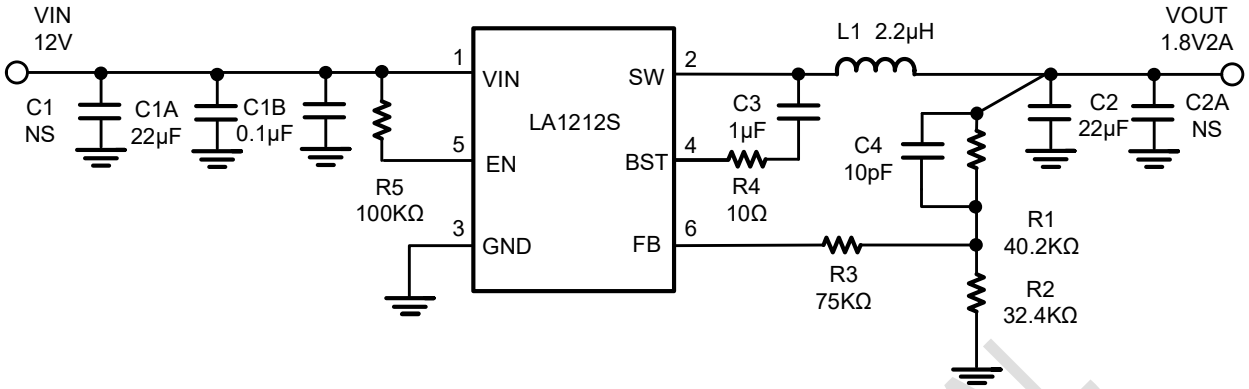


12VIN, 3.3V/2A Output

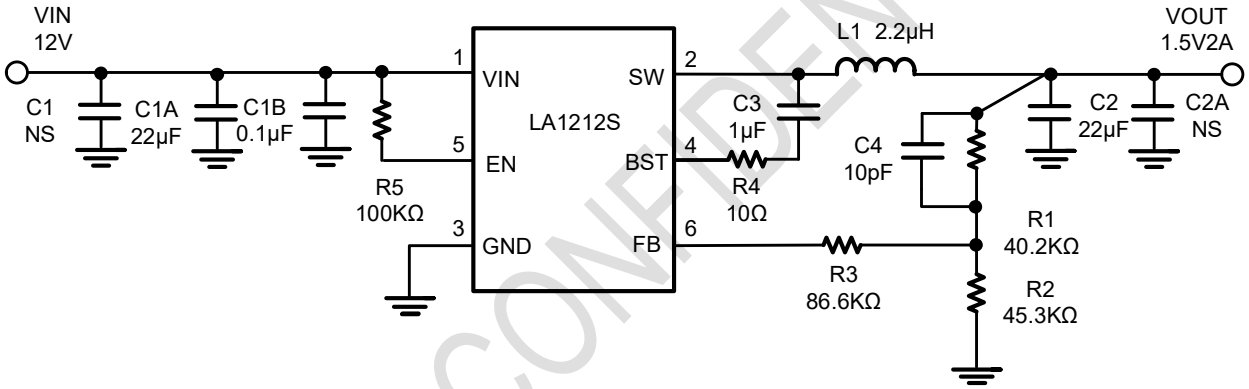


12VIN, 2.5V/2A Output

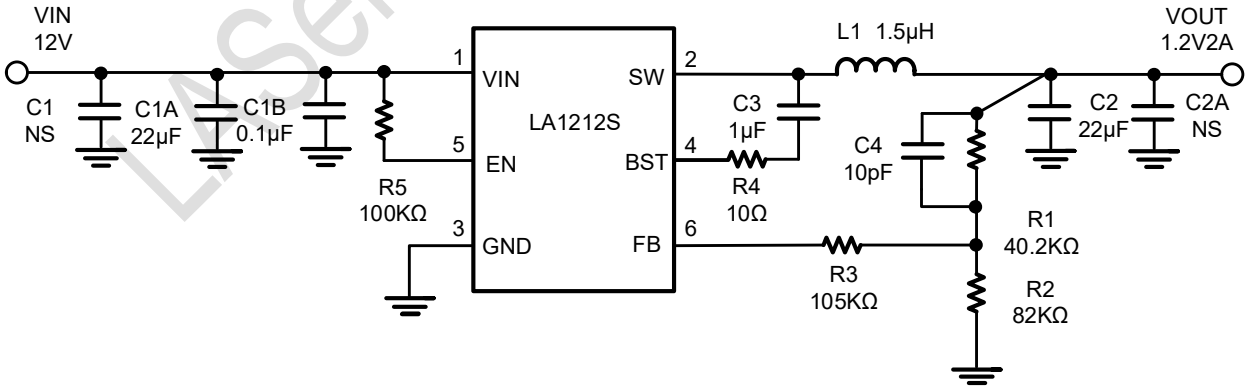
Typical Application Circuits



12VIN, 1.8V/2A Output

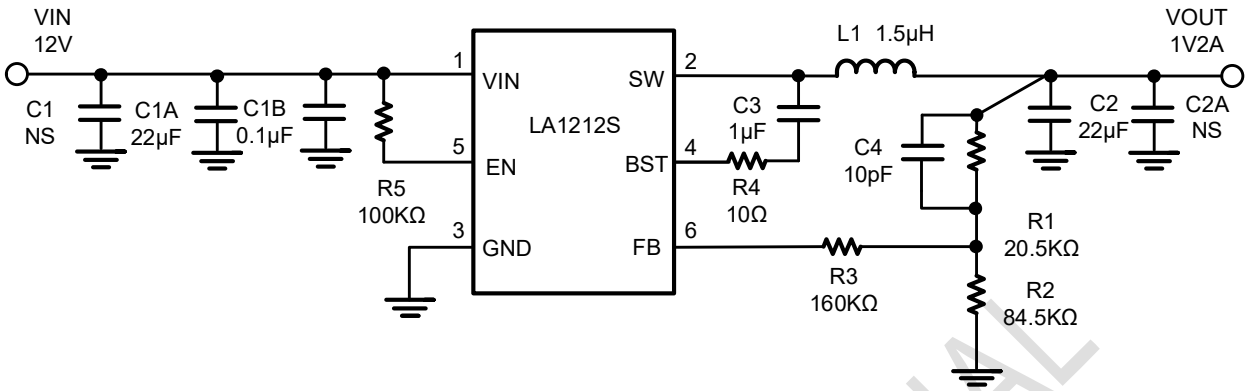


12VIN, 1.5V/2A Output



12VIN, 1.2V/2A Output

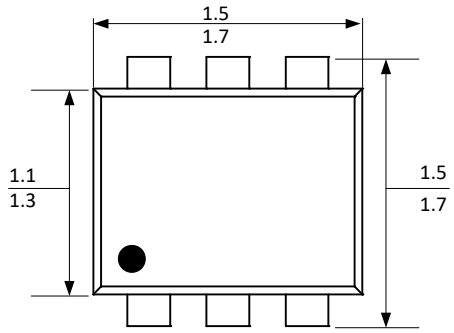
Typical Application Circuits



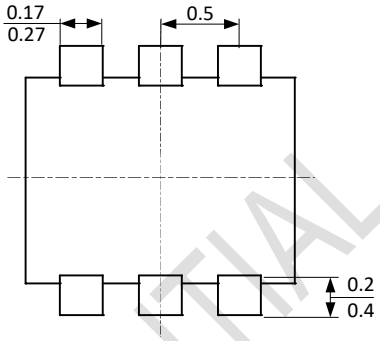
12VIN, 1V/2A Output

Detail Package Outline Drawing

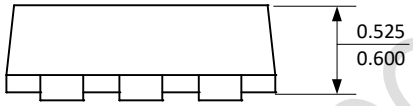
Package type: SOT563



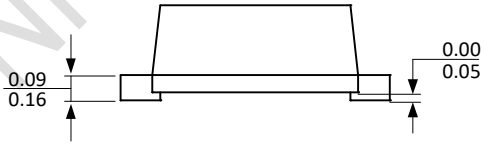
TOP VIEW



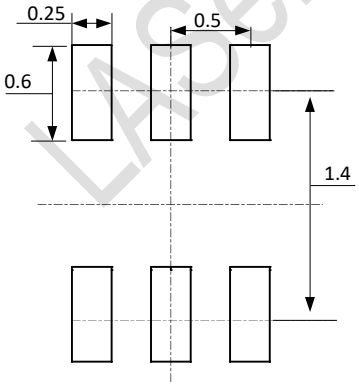
BOTTOM VIEW



FRONT VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1. ALL DIMENSIONS ARE IN MILLMETERS
2. PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION.
3. PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4. LEAD COPLANARITY(BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLMETERS MAX.
5. DRAWING IS NOT TO SCALE.

单击下面可查看定价，库存，交付和生命周期等信息

>>Lattice Art