36V, 3A, 500KHz, Synchronous, Step-Down Converter

LA1413

Overview

The LA1413 is an easy to use synchronous step-down Buck. Which integrated low on resistance high-side and low-side power MOSFETs. The LA1413 can deliver 3A of output current efficiently with constant on time (COT) control for fast loop response.

The LA1413 achieves high power conversion efficiency over a wide load range by scaling down the switching frequency under light-load conditions to reduce switching and gate driving losses.

The LA1413 has built-in protection features, such as cycle-by-cycle current limit, hiccup mode short-circuit protection, FB open short protection and thermal shutdown in case of excessive power dissipation. The LA1413 is available in a space-saving eSOP8L package.

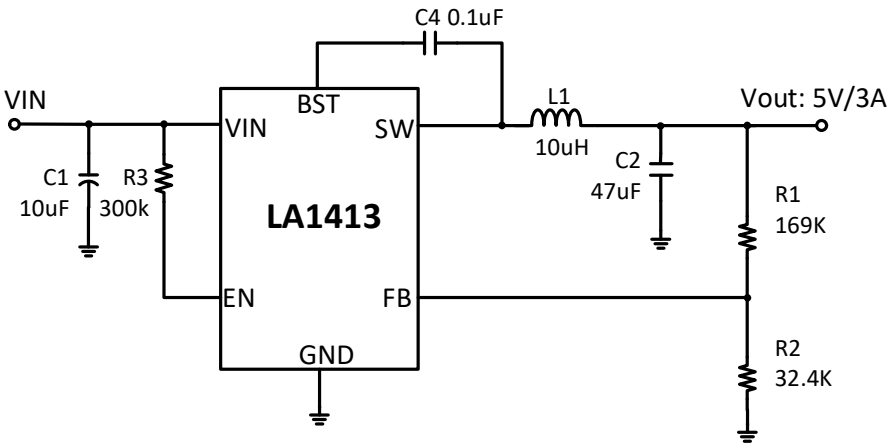
Features

- 4.5V to 36V Wide Input Range
- 3A Continuous Output Current
- 120mΩ/80mΩ Internal Power MOSFETs
- Constant On Time Control for Fast Loop Response
- 500KHz Switching Frequency
- Pulse Frequency Modulation at Light Load
- Support Up to 98% Large Range Duty Cycle
- Internal Soft Start
- Output Voltage adjustable from 0.8V
- Support Pre-Biased Output Startup
- Full Protection, Over Current Protection and Hiccup, Output Over Voltage Protection, FB Open Short Protection, Over Temperature Protection
- Available in an eSOP8L Package

Applications

- Robots
- Home Appliance and Whitegoods
- Multi-functional Printer
- Automotive
- Industrial Control

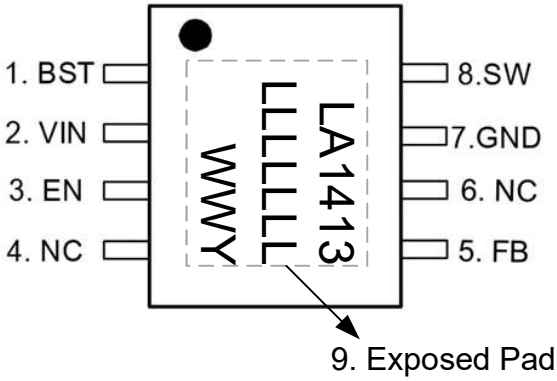
Typical Application



Package Mark and Order Information

Device	Package	Temperature range	Packaging Type	Purchase Contact
LA1413	eSOP8L	-40 to 150℃	T/R 2500pcs/roll	sales@latticeart.com

Pin Diagram

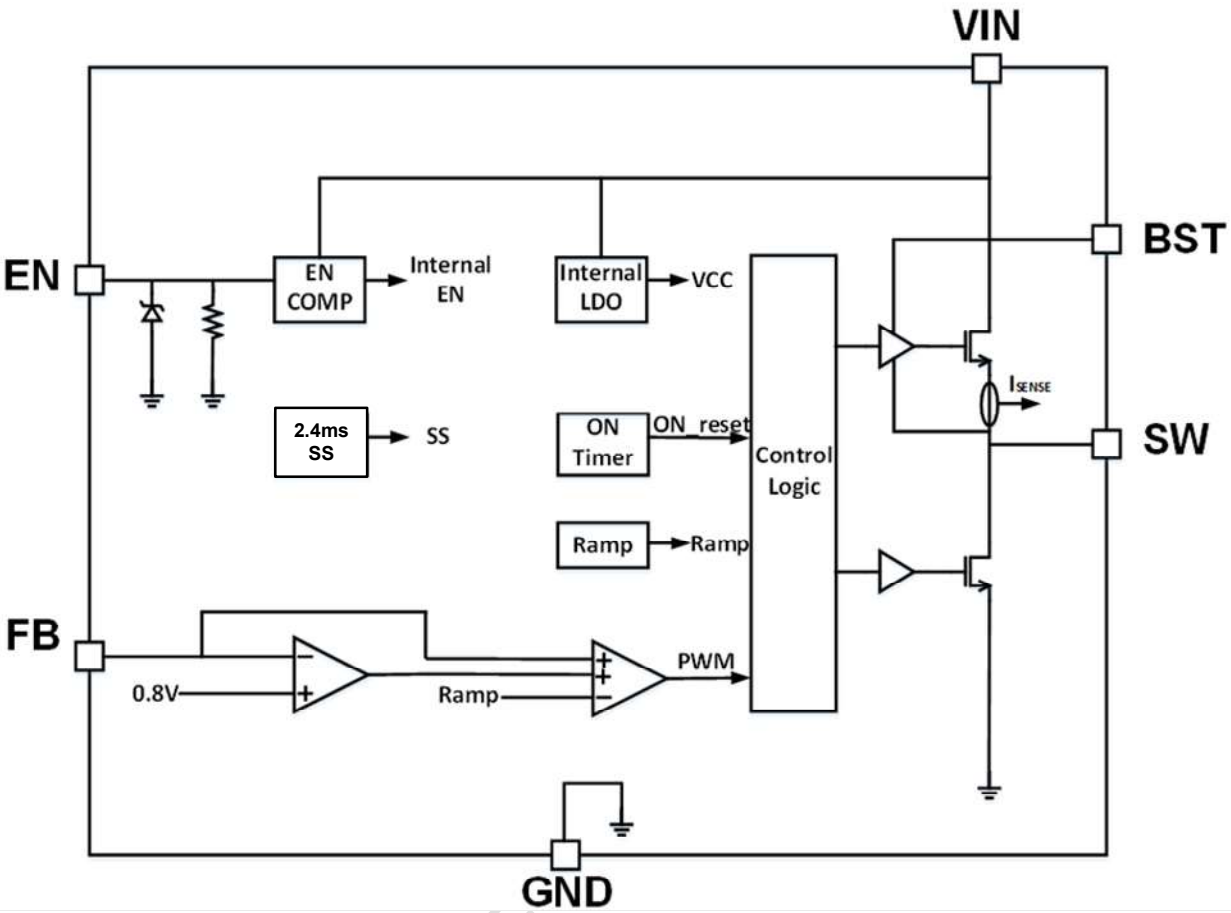


LA1413 : Product code
LLLLLLL: Lot number
WWY: Date Code

Pin Description

Pin No.	Symbol	Pin Description
1	BST	Bootstrap capacitor connection for high-side FET driver. Connect a high quality 100nF capacitor from this pin to the SW pin.
2	VIN	Supply input terminal to internal bias LDO and high-side FET. Connect to input supply and input bypass capacitors CIN. Input bypass capacitors must be directly connected to this pin and GND.
3	EN	Precision enable input to the convertor. Do not float. High = on, Low = off. Can be tied to VIN by a resistor. Precision enable input allows adjustable UVLO by external resistor divider.
4, 6	NC	Not Connected.
5	FB	Feedback input to the convertor. Connect a resistor divider to set the output voltage. Never short this terminal to ground during operation.
7	GND	Power Ground terminal.
8	SW	Switching output of the convertor. Internally connected to source of the high-side FET and drain of the low-side FET. Connect to power inductor.
9	EP	Exposed Pad. Connect exposed pad to the PCB GND plane to achieve good thermal performance.

Block Diagram



Absolute Maximum Ratings (Note 1)

T_A=25^{0}C, unless otherwise specified.

Symbol	Definition	Ratings	Unit
V_{IN}	VIN to GND	-0.3~38	V
SW	SW to GND	-0.7 (-5V in 10ns)~VIN + 0.7	V
EN	Max Input current to EN pin	400	uA
BST	BST to SW	-0.3~6	V
All Other Pins		-0.3~6	V
T_{STG}	Storage temperature	-55 to150	°C
T_j	Junction temperature	-40 to150	°C

Note 1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are not tested at manufacturing.

Recommended Operating Conditions

Symbol	Definition	Ratings	Unit
BST	BST to SW	4~5	V
FB	FB to GND	0~1	V
EN	EN to GND	0~5	V
V_{IN}	VIN to GND	4.5~36	V
V_{OUT}	V_{OUT} to GND	0.8~0.98xVIN or VOUT<18V	V
I_{OUT}	Max Continuous Output Current	3	A

Thermal Resistance (Note 2)

Symbol	Definition	Ratings	Unit
$R_{\theta JC(TOP)}$	Junction to case (top) thermal resistance	52	°C/W
$R_{\theta JC(BOT)}$	Junction to case (bottom) thermal resistance	2.3	°C/W
$R_{\theta JA}$	Junction to ambient thermal resistance	48	°C/W

Note 2: Measured on JESD51-7, 4-Layer PCB, and the PCB has no copper for thermal dissipation. Normal PCB with copper thermal resistance will be smaller.

Electrical Characteristics

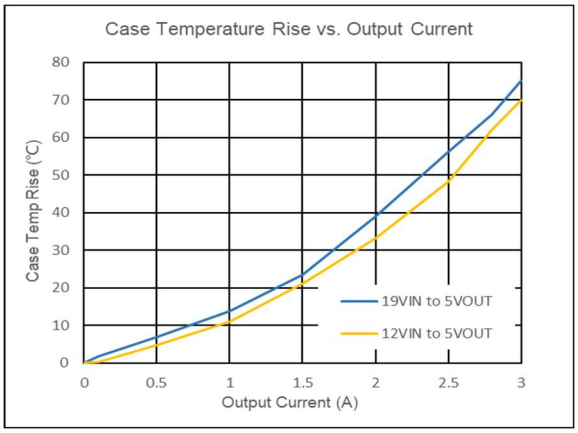
V_{IN}=12V, V_{EN}=2V, T_A=25°C, unless otherwise specified.

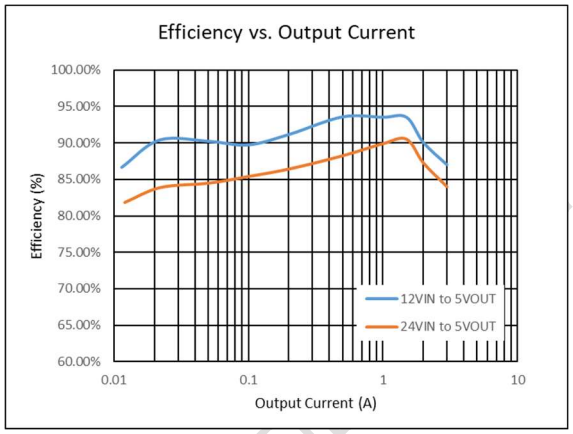
Symbol	Parameter	Condition	Min	Typ	Max	Units
VIN_{UVR}	VIN UVLO rising threshold		4.1	4.2	4.3	V
VIN_{UVF}	VIN UVLO falling threshold		3.8	3.95	4.05	V
VIN_{UV_hys}	VIN UVLO hysteresis			0.3		V
I_{QS}	Shutdown supply current	V_{EN} < 0.3V V_{IN}=24V		1	3	μA
I_Q	Quiescent supply current	No load, VFB = 0.83V, no switching		150		μA
LKG_{HS}	High-side leakage	V_{EN} = 0V, V_{SW} = 0V			1	μA
LKG_{LS}	Low-side leakage	V_{EN} = 0V, V_{SW} = 45V			1	μA
V_{FB}	Feedback voltage		784	800	816	mV
V_{FB_SHORT}	FB short threshold			300		mV
I_{LK_FB}	Feedback leakage	V_{EN} = 1V, V_{FB} = 2V			0.1	μA
R_{ON_HS}	High-side switch on resistance	V_{BST} - V_{SW} = 5V		120		mΩ
R_{ON_LS}	Low-side switch on resistance	V_{IN} = 12V		80		mΩ
I_{LIM_LS}	Low-side Current limit			3.5		A
T_{SS}	Soft-start time	V_{FB} from 0% to 100%		2.4		ms
F_{SW}	Oscillator frequency			0.52		MHz
T_{ONMIN}(3)	Minimum switch on time			80		nS
T_{OFFMIN}(3)	Minimum switch off time			120		nS
D_{MAX}	Max duty cycle			98%		%
V_{EN_R}	Enable rising threshold	Low to high	1.1	1.2	1.3	V
V_{EN_F}	Enable falling threshold	High to low	0.8	0.9	1.0	V
V_{EN_Hys}	Enable Threshold Hysteresis			0.3		V
R_{EN}	Enable input resistor.			1500		kOhm
T_{OTP_R}(3)	Thermal shutdown			150		°C
T_{OTP_Hys}(3)	OTP hysteresis			20		°C

3) Not tested in production and derived from bench characterization.

Typical Performance Characteristic

V_{IN} = 12V, V_{OUT} = 5V, C1 = 10μF, C2 = 22μF, L1 = 10μH, and T_A = +25°C, unless otherwise noted.



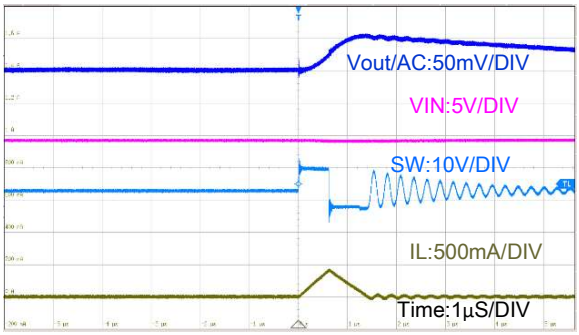


Typical Performance Characteristic *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, C1 = 10μF, C2 = 22μF, L1 = 10μH, and T_A = +25°C, unless otherwise noted.

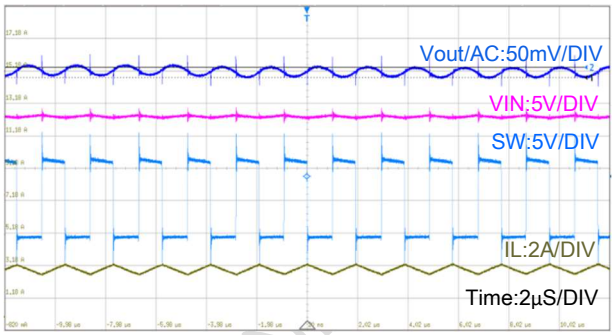
Output Voltage Ripple

IOUT = 0A



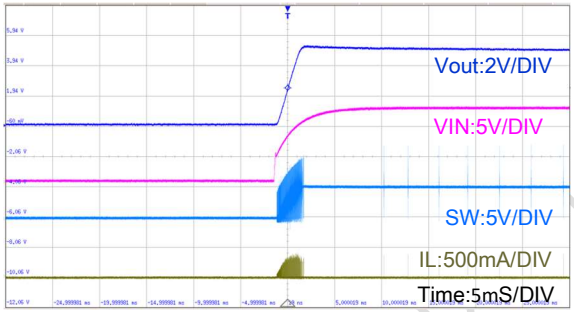
Output Voltage Ripple

IOUT = 3A



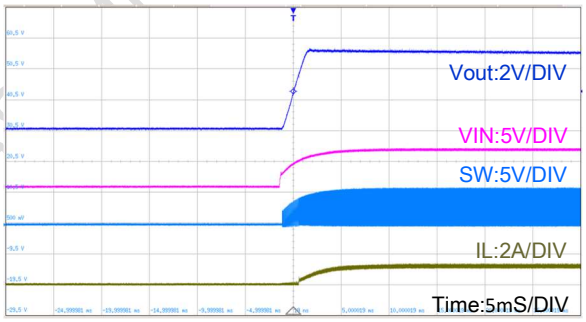
Start-Up through V_{IN}

IOUT = 0A



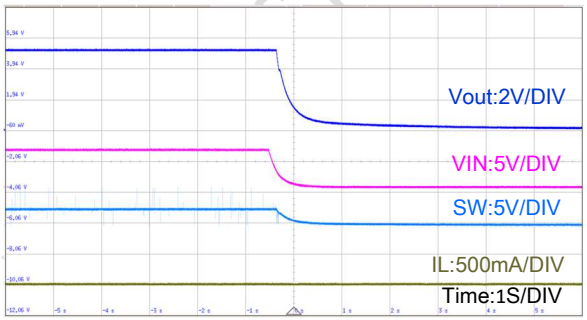
Start-Up through V_{IN}

IOUT = 3A



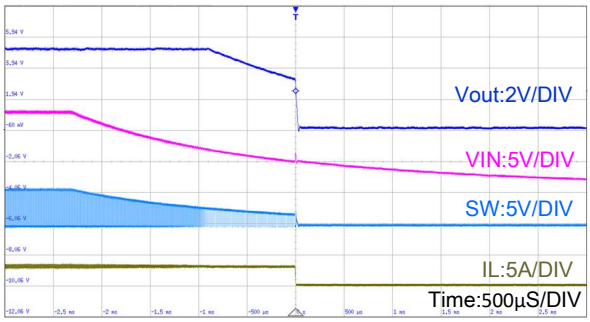
Shut-Down through V_{IN}

IOUT = 0A



Shut-Down through V_{IN}

IOUT = 3A

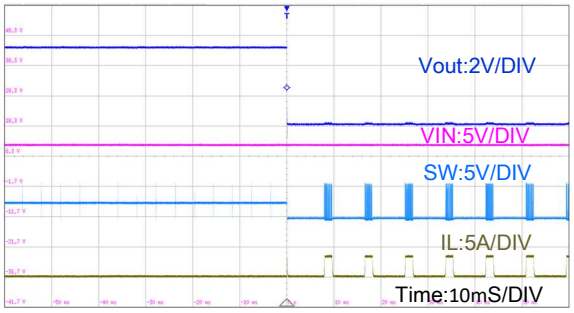


Typical Performance Characteristic *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, C1 = 10μF, C2 = 22μF, L1 = 10μH, and T_A = +25°C, unless otherwise noted.

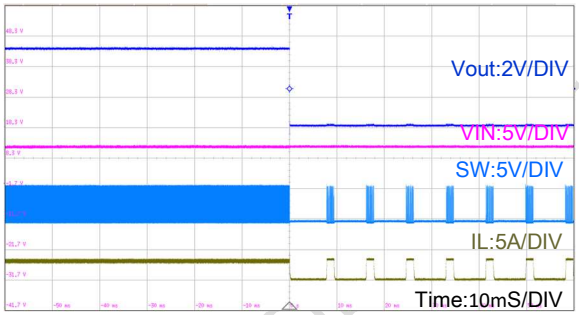
Short-Circuit Entry

IOUT = 0A



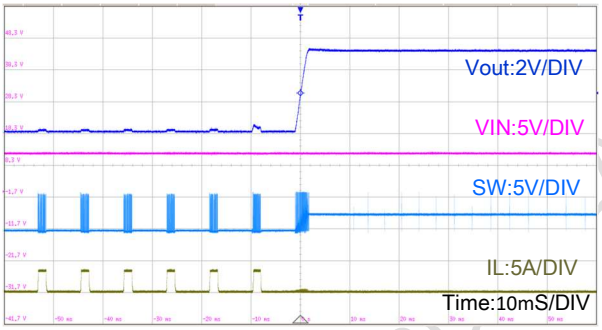
Short-Circuit Entry

IOUT = 3A



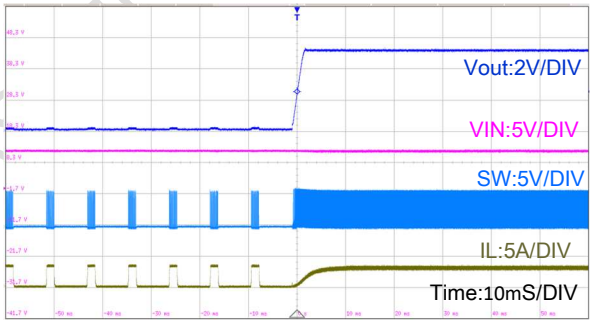
Short-Circuit Recovery

IOUT = 0A



Short-Circuit Recovery

IOUT = 3A



Function Descriptions

Pulse-Width Modulation (PWM) Control

The LA1413 is fully integrated synchronous rectified step-down switch mode converter. Constant-on-time (COT) control is employed to provide fast transient response and easy loop stabilization. At the beginning of each cycle, the high-side MOSFET (HS-FET) is turned ON when the feedback voltage (VFB) is below the reference voltage (VREF), which indicates insufficient output voltage. The ON period is determined by both the output voltage and input voltage to make the switching frequency fairy constant over input voltage range.

After the ON period elapses, the HS-FET is turned off, or becomes OFF state. It is turned ON again when VFB drops below VREF. By repeating operation this way, the converter regulates the output voltage. The integrated low- side MOSFET (LS-FET) is turned on when the HS-FET is in its OFF state to minimize the conduction loss.To avoid shoot-through, a dead-time (DT) is internally generated between HS-FET off and LS-FET on, or LS-FET off and HS-FET on.

An internal compensation is applied for COT control to make a more stable operation even when ceramic capacitors are used as output capacitors, this internal compensation will then improve the jitter performance without affect the line or load regulation.

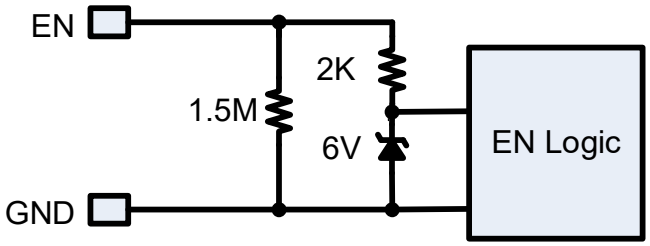
With the load decrease, the inductor current decrease too. Once the inductor current touch zero, the operation is transition from continuous-conduction-mode (CCM) to discontinuous- conduction-mode (DCM).

When the LA1413 works in pulse-frequency modulation (PFM) mode during light-load operation, the LA1413 reduces the switching frequency automatically to maintain high efficiency, and the inductor current drops almost to zero. When the inductor current reaches zero, the low-side will be off. The output capacitors discharge slowly to GND through R1 and R2. When VFB drops below the reference voltage, the HS-FET is turned on again. This operation improves device efficiency greatly when the output current is low.

Enable (EN) Control

Enable (EN) is a digital control pin that turns the regulator on and off. Drive EN high to turn on the regulator. Drive EN low to turn off the regulator. An internal 1.7MΩ resistor from EN to GND allows EN to be floated to shut down the chip. EN is clamped internally using a 6V Zener diode. EN can connected to VIN directly by a resistor.

The EN Pin can connect to VIN by a pull-up resistor, but EN input current need below 100uA. For example, if VIN=24V, the IZener=(24-6)/RPULL-UP<100uA, So, RPULL-UP>180KΩ.



Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The LA1413 UVLO comparator monitors the input voltage. The UVLO rising threshold is about 4.2V, while its falling threshold is consistently 3.9V.

Internal Soft Start (SS)

Soft start (SS) prevents the converter output voltage from overshooting during start-up. When the chip starts, the internal circuitry generates a soft-start voltage (VSS) that ramps up from 0V to 1V. When SS is below REF, SS overrides REF, so the error amplifier uses SS as the reference. When SS exceeds REF, the error amplifier uses REF as the reference. The SS time is set to 1.8ms internally.

Over-Current Protection (OCP) and Short Circuit Protection (SCP)

The LA1413 has a valley current-limit control. During LS-FET on, the inductor current is monitored. If the current is higher than valley current limit, the high side will not turn on again. The output voltage drops until VFB is below the under voltage (UV) threshold (typically 20% below the reference). Once UV is triggered, the LA1413 enters hiccup mode to restart the part periodically.

During OCP, the device attempts to recover from the over-current fault with hiccup mode. In hiccup mode, the chip disables the output power stage, discharges the soft start, and attempts to soft start again automatically. If the over-current condition still holds after the soft start ends, the device repeats this operation cycle until the over-current condition is removed and the output rises back to regulation levels. OCP is a non-latch protection.

Pre-Bias Start-Up

The LA1413 is designed for monotonic start-up into pre-biased loads. If the output is pre-biased to a certain voltage during start-up, the BST voltage is refreshed and charged, and the voltage on the soft start is charged as well. If the BST voltage exceeds its rising threshold voltage and the soft-start voltage exceeds the sensed output voltage at FB, the part works normally.

Large Duty Cycle Operation

When LA1413 will automatically extend the frequency to support the application when VIN is close to VOUT. The frequency extend circuit will be triggered when Toff min time is reached. The LA1413 can support up to 98% maximum duty cycle.

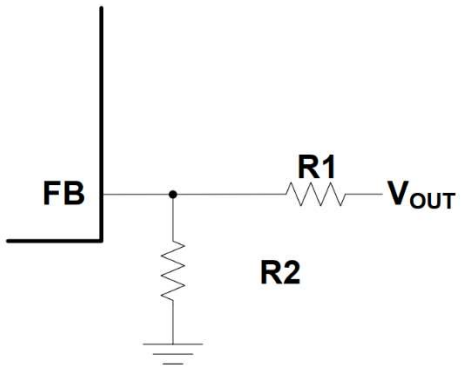
Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the silicon die temperature exceeds 150°C, the entire chip shuts down. When the temperature falls below its lower threshold (typically 130°C), the chip is enabled again.

Application Information

Setting the Output Voltage

The LA1413 output voltage can be set by the external resistor dividers. The reference voltage is fixed at 0.8V. The feedback network is shown below Figure.



Feedback Network

Choose R1 and R2 using Equation:

$$V_{OUT} = V_{FB}(R_1 + R_2) / R_2$$

Selecting the Inductor

For most applications, use a 3.3μH to 47μH inductor with a DC current rating at least 25% higher than the maximum load current. For the highest efficiency, use an inductor with a small DC resistance.

For most designs, the inductance value can be derived from Equation:

$$L = \frac{V_{OUT} * (V_{IN} - V_{OUT})}{V_{IN} * \Delta I_L * F_{OSC}}$$

Where ΔIL is the inductor ripple current.

Choose the inductor ripple current to be approximately 30% of the maximum load current. The maximum inductor peak current can be calculated with Equation:

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2}$$

Table 1 lists the recommended feedback resistor values for common output voltages.

Table 1: Resistor Selection for Common Output Voltages (7)

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	L (μH)	C_{OUT}(uF)
5	169	32.4	10	47
3.3	102	32.4	10	47

Selecting the Output Capacitor

The output capacitor (C2, C3) maintains the DC output voltage ripple. Use ceramic, tantalum, or low-ESR electrolytic capacitors. For best results, use low ESR capacitors to keep the output voltage ripple low. The output voltage ripple can be estimated with Equation:

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{OSC} * L} * (1 - \frac{V_{OUT}}{V_{IN}}) * (R_{ESR} + \frac{1}{8 * F_{OSC} * C_{OUT}})$$

Where L is the inductor value, and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

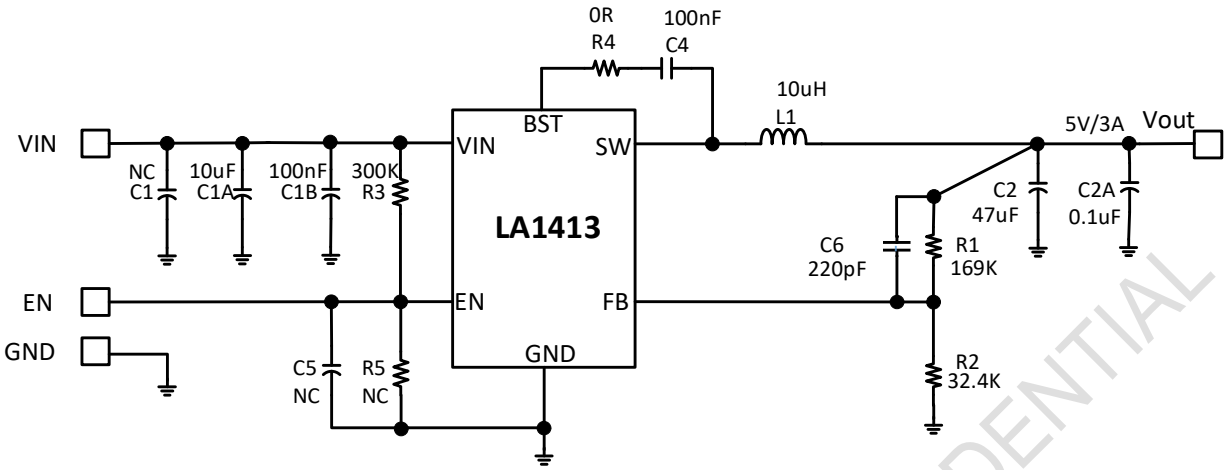
The characteristics of the output capacitor also affect the stability of the regulation system. The LA1413 can be optimized for a wide range of capacitance and ESR values.

PCB layout Guidelines

Efficient layout of the switching power supplies is critical for stable operation. For the high frequency switching converter, poor layout design may cause poor line or load regulation and stable issues. For best results, refer to below figure and follow the guidelines below.

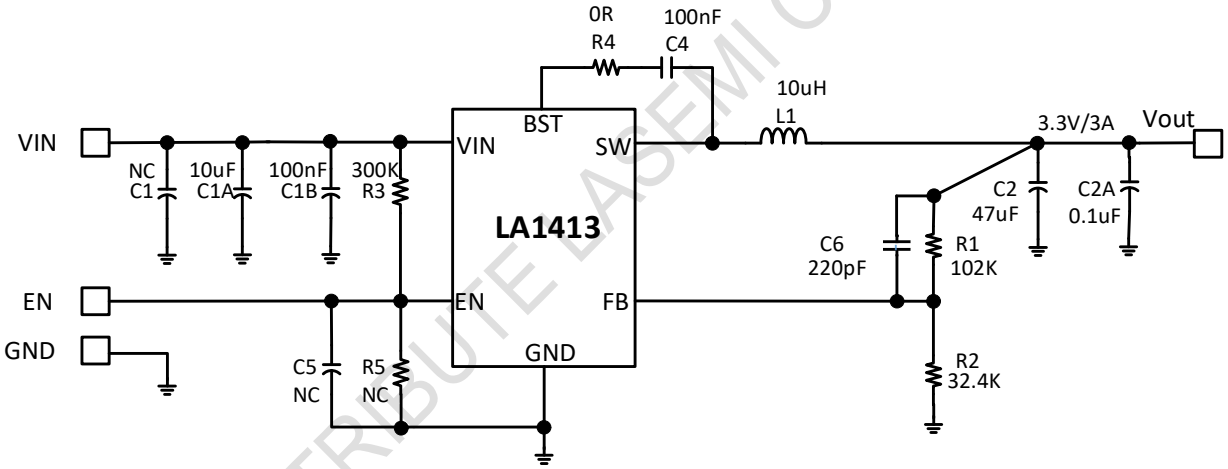
- Place the input capacitor as close to VIN and GND as possible.
- Place the external feedback resistors as close to FB as possible.
- Keep the switching node (such as SW, BST) far away from the feedback network.
- Add a grid of thermal vias under the exposed pad to improve thermal conductivity.

Typical Application Circuits



Note: C6 is optional for better transient performance.

VIN=12V VOUT=5V/3A

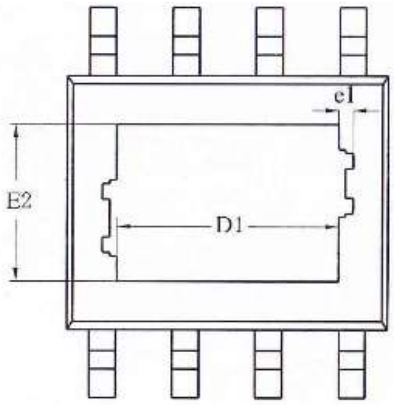


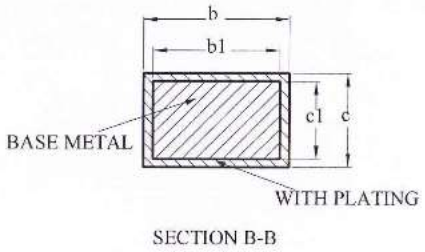
Note: C6 is optional for better transient performance.

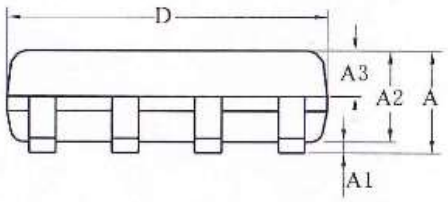
VIN=12V VOUT=3.3V/3A

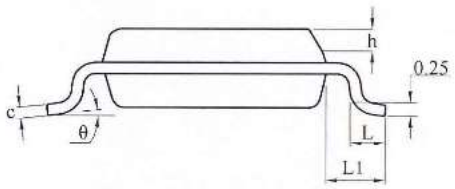
Detail Package Outline Drawing

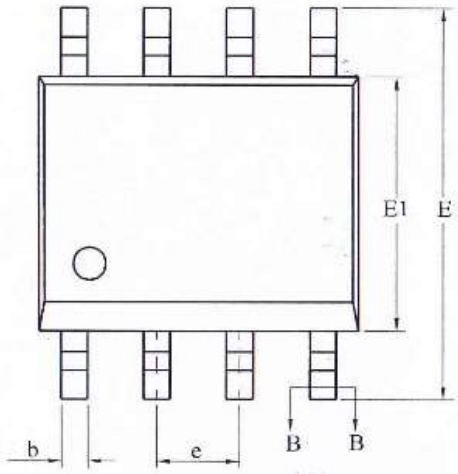
Package type: eSOP8L











SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.65
A1	0.05	—	0.15
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	—	0.47
b1	0.38	0.41	0.44
c	0.20	—	0.24
c1	0.19	0.20	0.21
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27BSC		
h	0.25	—	0.50
L	0.50	0.60	0.80
L1	1.05REF		
θ	0	—	8°

Size (mil) / L/F Size (mil)	D1	E2	e1
90*90	2.09REF	2.09REF	0.16REF
95*130	3.10REF	2.21REF	0.10REF

单击下面可查看定价，库存，交付和生命周期等信息

>>Lattice Art