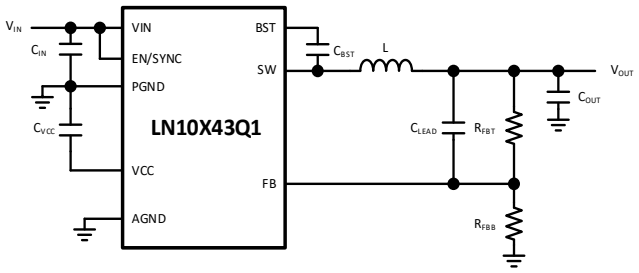
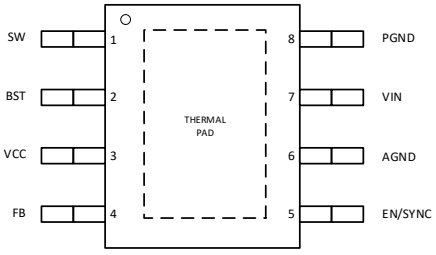
3.5V to 36V, 3A, Synchronous Step-Down Regulator

1 FEATURES

- Automotive AEC-Q100 Grade 1 Compliance
- Wide V_{IN} Range: 3.5V to 36V
- Wide V_{OUT} Range: 1V to V_{IN}
- Integrated both High-Side and Low-Side Power MOSFETs with up to 3A Output Capability
- Frequency Options: 400kHz, 1MHz, 2.1MHz
- PLL Synchronization to External Clock
- High Efficiency Low Load DCM and PFM Operation
- Near 100% Duty Cycle Operation for Low Drop Out Operation
- Forced PWM Option
- Accurate Peak and Valley Clamp and Protection
- Internal Compensation
- Spread Spectrum Option for Low EMI Applications
- Accurate VIN UVLO Protection
- Over-Temperature Shutdown and Recovery
- Operating Junction Temperature -40˚C to 150 ˚C
- Output Short-Circuit Protection with Hiccup Mode
- Thermally Enhanced SOIC-EP8 Package (4.9mm X 3.9mm)



Typical Application Diagram



Package Diagram (SOIC-EP8)

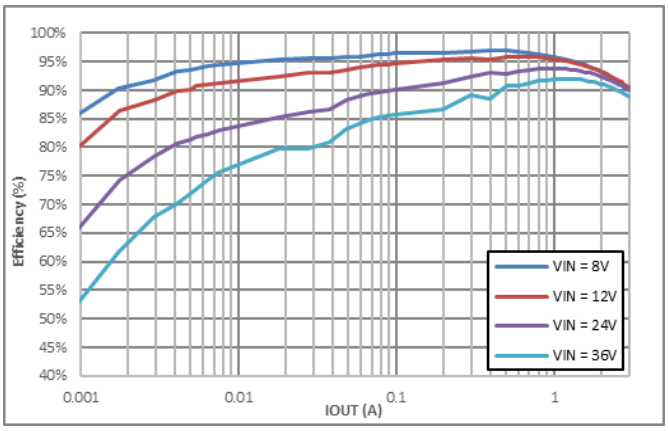
2 APPLICATIONS

- Automotive Power Supplies
- Industrial Power Supplies
- Battery Powered Systems

3 DESCRIPTION

The LN10X43Q1 is a high efficiency, compact, synchronous step-down DC-DC converter employing a constant frequency, peak current mode control architecture with internal compensation. It operates from an input voltage from 3.5V to 36V, provides an adjustable output voltage from 1V to V_{IN}. LN10X43Q1 can deliver up to 3.0A. The nominal switching frequency is fixed on 400kHz, 1MHz or 2.1MHz, or can be synchronized to an external clock. Automatic frequency foldback at light load can improve efficiency.

Additional features such as FPWM option, precision enable, and internal soft start provide both flexible and easy to use solutions for a wide range of applications. Protection features include input undervoltage lockout, thermal shutdown, cycle-by-cycle current limit, and short-circuit protection.



LN10043Q1, V_{OUT}=5V, Efficiency Curve

Table of Contents

4 REVISION HISTORY

Version	Change Description	Date
1.0	Initial Version	2021/10/28
1.1	Update Part Number throughout the document ·····P4 Tighten the min, max and typical limits of electrical parameters·····P8 Add switching waveform in SPREAD SPECTRUM MODULATION·····P13 Update package information ·····P24	2022/4/24

5 ORDER INFORMATION

Part Number	Frequency	Light Load Mode	Spread Spectrum	IC Package	MSL-Peak-Temp (1)	Material	Package	Package Qty	Top Marking (2)
LN10043Q1-EFR	400kHz	PFM	No	SOIC-EP8	Level-3-260C	RoHS	Tape & Reel	3000	LN10043Q1
LN10143Q1-EFR	400kHz	FPWM	No	SOIC-EP8	Level-3-260C	RoHS	Tape & Reel	3000	LN10143Q1
LN10243Q1-EFR	1MHz	PFM	No	SOIC-EP8	Level-3-260C	RoHS	Tape & Reel	3000	LN10243Q1
LN10343Q1-EFR	1MHz	FPWM	No	SOIC-EP8	Level-3-260C	RoHS	Tape & Reel	3000	LN10343Q1
LN10443Q1-EFR	2.1MHz	PFM	No	SOIC-EP8	Level-3-260C	RoHS	Tape & Reel	3000	LN10443Q1
LN10543Q1-EFR	2.1MHz	FPWM	No	SOIC-EP8	Level-3-260C	RoHS	Tape & Reel	3000	LN10543Q1
LN10043Q1SEFR	400kHz	PFM	Yes	SOIC-EP8	Level-3-260C	RoHS	Tape & Reel	3000	10043QS
LN10143Q1SEFR	400kHz	FPWM	Yes	SOIC-EP8	Level-3-260C	RoHS	Tape & Reel	3000	10143QS
LN10243Q1SEFR	1MHz	PFM	Yes	SOIC-EP8	Level-3-260C	RoHS	Tape & Reel	3000	10243QS
LN10343Q1SEFR	1MHz	FPWM	Yes	SOIC-EP8	Level-3-260C	RoHS	Tape & Reel	3000	10343QS
LN10443Q1SEFR	2.1MHz	PFM	Yes	SOIC-EP8	Level-3-260C	RoHS	Tape & Reel	3000	10443QS
LN10543Q1SEFR	2.1MHz	FPWM	Yes	SOIC-EP8	Level-3-260C	RoHS	Tape & Reel	3000	10543QS

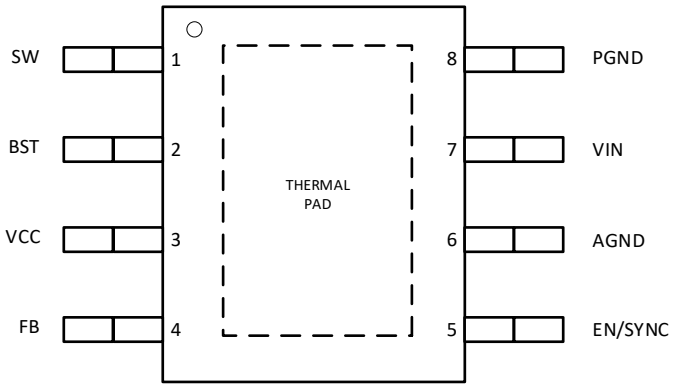
(1) MSL (Moisture Sensitivity Level) is based on JEDEC industrial classification and the tabled temperature is the maximum solder temperature;

(2) There may be additional marking relates to the lot number or date code on the device.

6 PIN CONFIGURATION

6.1 Pin Configuration

SOIC-EP8 (4.9mm X 3.9mm) Top View



6.2 Pin Functions

Name	PIN Number	Type	Description
SW	1	Power	Switch node connection from the internal power MOSFETs to the external inductor.
BST	2	Power	Bootstrapped supply to the high side gate driver. Connect a 0.1 - 0.47µF ceramic capacitor between BST and SW pins.
VCC	3	Power	Voltage source that powers the gate drivers of the internal power MOSFETs and control circuits. Must be decoupled to PGND with a 1 - 4.7µF ceramic capacitor.
FB	4	Signal	Output voltage feedback input. Use an external divider to set the desired output voltage.
EN/SYNC	5	Signal	Enable pin for V_{CC} LDOs, regulator output, and input voltage for V_{IN} UVLO. Connect to V_{IN} directly, to V_{IN} through a divider, or to an external voltage source. This pin is also used for external clock synchronization.
AGND	6	Ground	Analog ground.
VIN	7	Power	Power supply input pin to high side power MOSFET and V_{IN} LDO regulator. Decouple this pin to PGND with ceramic capacitors.
PGND	8	Ground	Power ground. Connect the pins to ground plane.
THERMAL PAD	-	-	Thermal dissipation pad. Solder to ground plane.

7 SPECIFICATIONS

7.1 Absolute Maximum Ratings

Parameters (1)	Min	Max	Unit
VIN to PGND	-0.3	42	V
EN/SYNC to PGND	-0.3	V_{IN} + 0.3	
FB to AGND	-0.3	5.5	
SW to PGND	-1.0	V_{IN} + 0.3	
SW to PGND （Less than 10ns overshoot）	-3.5	42	
BST to SW	-0.3	5.5	
Operating Ambient Temperature	-40	125	˚C
Junction Temperature	-40	150	
Storage Temperature	-55	150	

(1) Exceeding these absolute-maximum-ratings may damage the device.

7.2 ESD Ratings

Parameters	Min	Max	Unit
HBM Human Body Model		±3000	V
CDM Charge Device Model		±750	

7.3 Recommented Operating Condition

Parameters	Min	Max	Unit
VIN	3.5	36	V
EN/SYNC	-0.3	V_{IN}	
FB	-0.3	1.1	
VOUT	1	V_{IN}	
IOUT	0	3	A
Junction Temperature	-40	150	˚C

7.4 Package Thermal Parameters

Parameter (1)		SOIC-EP8	Units
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance	39	˚C/W
ψ_{JT}	Junction-to-Top Characterization Parameter	3	˚C/W

(1) Measurements are based on standard 2s2p PCB defined in JESD 51-7 2s2p, under no wind , 2W loss, and 25 ˚C ambient temperature.

7.5 Electrical Characteristics

Unless otherwise stated, the minimum and maximum limits apply over the recommended operating junction temperature range of -40˚C to 150˚C. Typical values are measured at 25˚C and represent the most likely norm. The default conditions apply: V_{IN} = 12V, V_{OUT} = 5V, F_S = 400kHz。

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE, VOUT (VIN PINS)						
V_{IN}	Operating Input Voltage Range		3.5		36	V
$I_{Q-PFM-NOSW}$	Operating Quiescent Current (Non-Switching)	V_{FB}=1.2V, T_A=25˚C		62		μA
I_{Q-FPWM} (1)	During Regulation In FPWM	V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 0A For LN10143Q1		4.38		mA
I_{SHDN}	Shutdown Quiescent Current	V_{IN} = 12V, V_{EN} = 0V		0.5	4.05	μA
FB PIN						
V_{FB-CCM}	Regulated Feedback Voltage in CCM Mode	Full V_{IN} Range, Full Load Range, @25˚C	0.992	1.0	1.008	V
		Full V_{IN} Range, Full Load Range, Full Operational Temperature Range	0.98	1.0	1.02	V
I_{Q-FB}	Feedback Input Leakage Current	V_{FB} = 1.0 V		0	100	nA
POWER MOSFETS (2)						
$R_{DSON-HS}$	High Side MOSFET ON Resistance	I_{OUT} = 1A, V_{BST}-V_{SW} = 5V		148	260	mΩ
$R_{DSON-LS}$	Low Side MOSFET ON Resistance	I_{OUT} = 1A, V_{CC} = 5V		85	150	mΩ
PWM						
T_{ON-MIN} (1)	Minimum ON Time			103		ns
OSCILLATOR						
$F_{S-400kHz}$	For LN10043Q1& LN10143Q1		320	400	460	kHz
$F_{S-1000kHz}$	For LN10243Q1& LN10343Q1		800	1000	1150	kHz
$F_{S-2100kHz}$	For LN10443Q1& LN10543Q1		1700	2100	2450	kHz

Electrical Characteristics (Continued)

Unless otherwise stated, the minimum and maximum limits apply over the recommended operating junction temperature range of -40˚C to 150˚C. Typical values are measured at 25˚C and represent the most likely norm. The default conditions apply: V_{IN} = 12V, V_{OUT} = 5V, F_S = 400kHz。

SYNCHRONIZATION (EN/SYNC PIN)						
F_{SYNC} (3)	SYNC Frequency Range		0.2		2.1	MHz
$V_{SYNC-HIGH}$ (4)	SYNC High-Level Voltage		2.5			V
$V_{SYNC-LOW}$	SYNC Low-Level Voltage				0.4	V
SPREAD SPECTRUM MODULATION (5)						
$\%\Delta F_S$	Spread Spectrum Modulation Frequency Range			-20		%
F_{SSM}	Spread Spectrum Modulation Frequency			13		kHz
ENABLE V_{IN} UVLO (EN PIN)						
$EN_{VOUT-ON}$	V_{IN} UVLO Rising Threshold	V_{EN} Rising	1.70	1.88	2.05	V
$EN_{VOUT-HYS}$	V_{IN} UVLO Hysteresis	V_{EN} Falling		350		mV
I_{Q-EN}	EN Pin Current	V_{EN} = 3.3V		0	100	nA
INTERNAL VCC LDOS (VCC PIN)						
$V_{CC-TARGET}$	V_{CC} Regulation Target			4.75		V
BOOTSTRAP (BST PIN) (1)						
$t_{REFRESH-PER}$	Auto-Refresh Period			29		µs
$t_{REFRESH-PUL}$	Auto-Refresh Pulse Width			200		ns

Electrical Characteristics (Continued)

Unless otherwise stated, the minimum and maximum limits apply over the recommended operating junction temperature range of -40˚C to 150˚C. Typical values are measured at 25˚C and represent the most likely norm. The default conditions apply: V_{IN} = 12V, V_{OUT} = 5V, F_S = 400kHz。

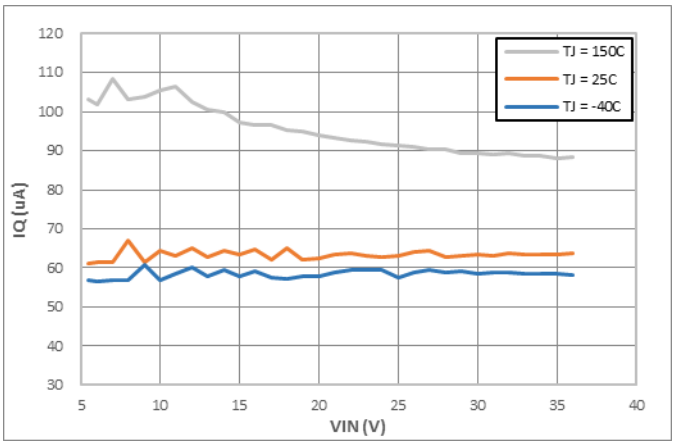
OVER CURRENT PROTECTION (6)						
$I_{LIM-PEAK-PFM}$	Peak Current Limit Threshold in PFM	V_{IN} = 12V	3.9	4.7	5.5	A
$I_{LIM-PEAK-FPWM}$	Peak Current Limit Threshold in FPWM	V_{IN} = 12V	3.9	4.7	5.5	A
$I_{LIM-Valley-PFM}$	Valley Current Limit Threshold in PFM	V_{IN} = 12V	2.9	3.2	3.5	A
$I_{LIM-Valley-FPWM}$	Valley Current Limit Threshold in FPWM	V_{IN} = 12V	2.9	3.2	3.5	A
$I_{NLIM-Valley-FPWM}$ (1)	Negative Valley Current Limit Threshold in FPWM	V_{IN} = 12V		-1.5		A
THERMAL SHUTDOWN (1)						
OT	Thermal Shutdown Threshold			170		˚C
OT_{HYS}	Thermal Shutdown Recovery Hysteresis			-10		˚C
INTERNAL SOFT START (7)						
t_{SS-INT}	Soft-Start Time			6		ms

(1) Guaranteed by design.
(2) Measured at pins.
(3) Tested with a 0V to +5Vpp, 50% duty cycle square wave.
(4) The average voltage on EN/SYNC pin must exceed $EN_{VOUT-ON}$.
(5) This function is available on LN10X43Q1S only.
(6) This current limit was tested as the internal comparator trigger point, the current limits measured in a close loop application may be different.
(7) Measured from $EN_{VOUT-ON}$ to internal soft start completed.

7.6 Typical Characteristics

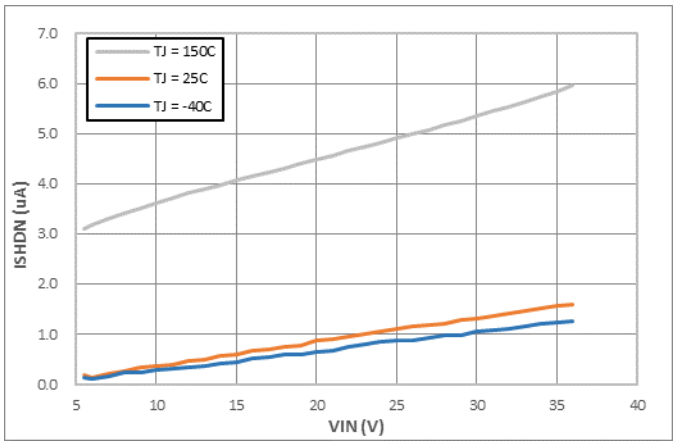
7.6.1 Characteristics Over Temperature

Unless otherwise stated, the test conditions are the same as Chapter 7.5. T_J = -40˚C 到 150˚C。



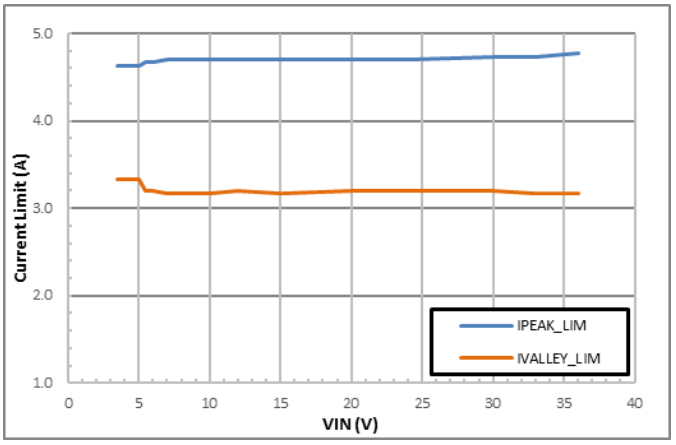
LN10043Q1, PFM, EN=5V, V_{OUT} = 5V, No load

Figure 1. Operating Quiescent Current I_Q



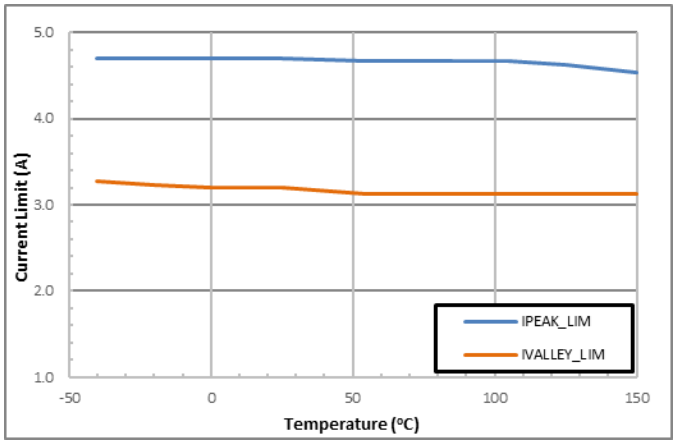
V_{EN} = 0V

Figure 2. Shutdown Current I_{SHDN}



LN10043Q1, PFM, F_S = 400kHz, V_{OUT} = 5V

Figure 3. Peak Current and Valley Current Limit Vs. V_{IN}

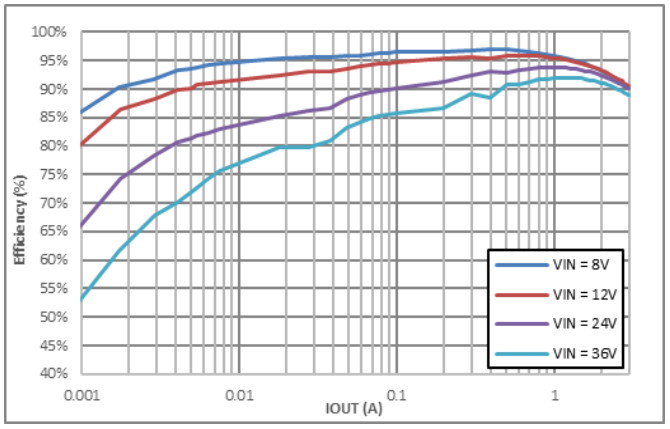


LN10043Q1, PFM, F_S = 400kHz, V_{OUT} = 5V

Figure 4. Peak Current and Valley Current Limit Vs. Temperature

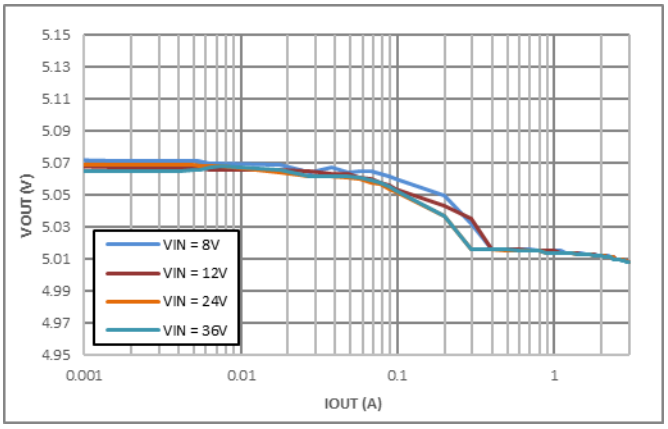
7.6.2 Typical Characteristics

Unless otherwise stated, the test conditions are: V_{IN} = 12V, V_{OUT} = 5V, F_S = 400kHz, L = 10µH, C_{OUT} = 100uF, T_A = 25 ˚C.



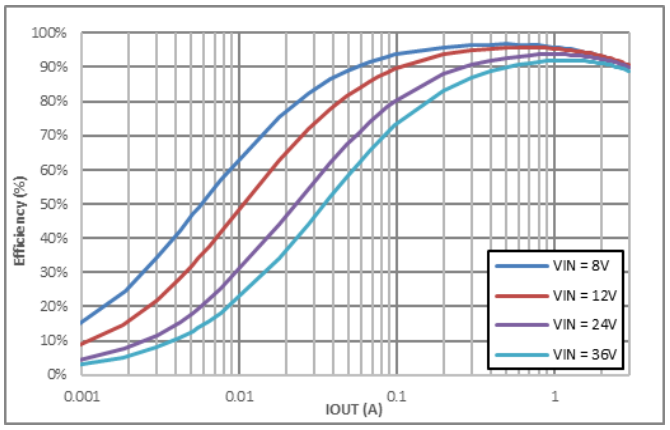
LN10043Q1, PFM, F_S = 400kHz, V_{OUT} = 5V

Figure 5. Efficiency Curves



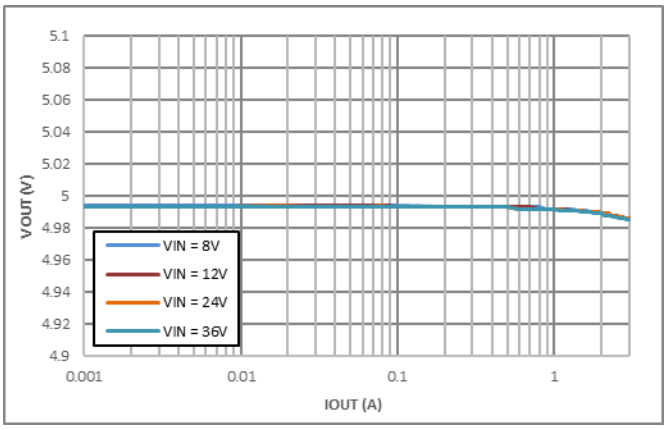
LN10043Q1, PFM, F_S = 400kHz, V_{OUT} = 5V

Figure 6. Load Regulation



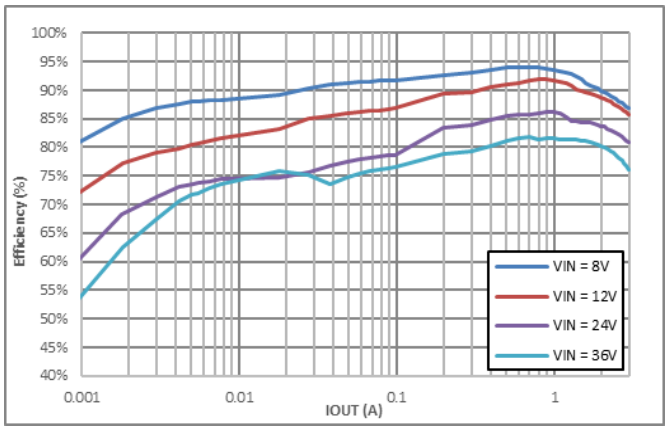
LN10143Q1, FPWM, F_S = 400kHz, V_{OUT} = 5V

Figure 7. Efficiency Curves



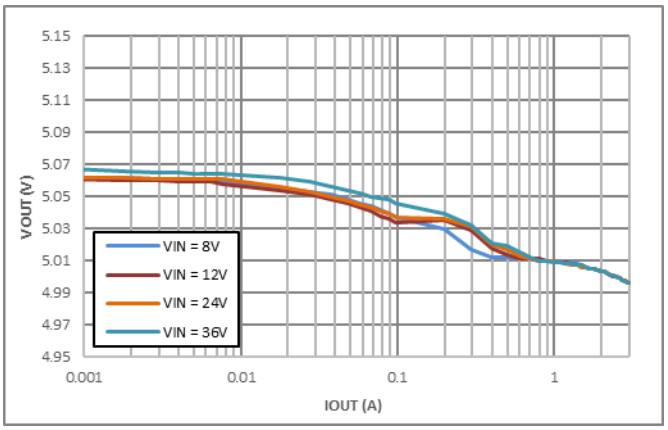
LN10143Q1, FPWM, F_S = 400kHz, V_{OUT} = 5V

Figure 8. Load Regulation



LN10443Q1, PFM, F_S = 2.1MHz, V_{OUT} = 5V

Figure 9. Efficiency Curves

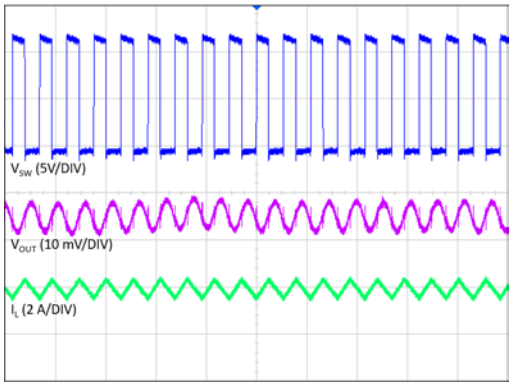


LN10443Q1, PFM, F_S = 2.1MHz, V_{OUT} = 5V

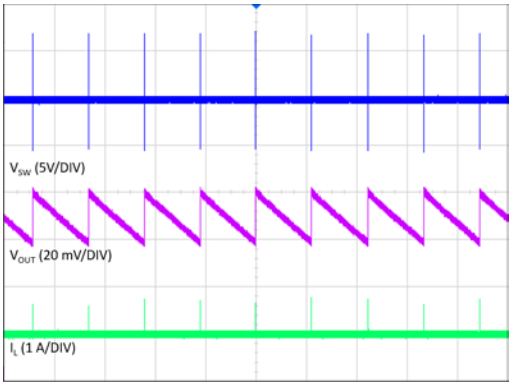
Figure 10. Load Regulation

7.6.3 Typical Waveforms

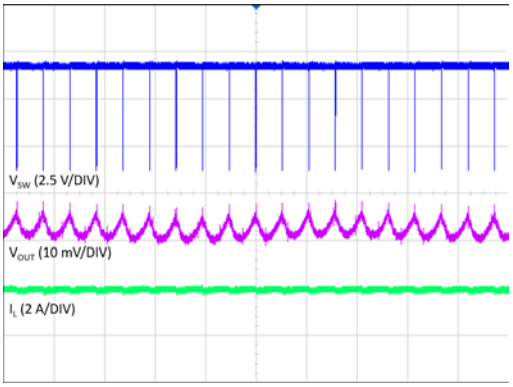
Unless otherwise stated, the test conditions are: V_{IN} = 12V, V_{OUT} = 5V, F_S = 400kHz, L = 10µH, C_{OUT} = 100uF, T_A = 25 ˚C.



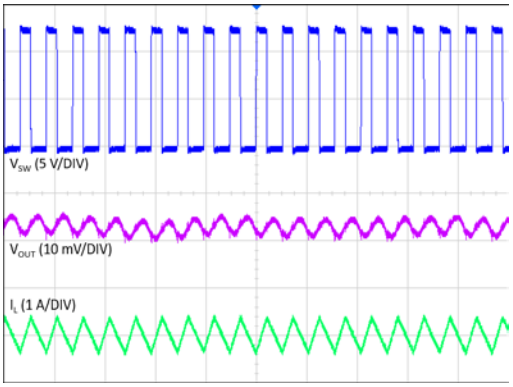
Time (5 µs/DIV)
LN10043Q1, F_S = 400kHz, V_{IN} = 12V, I_{OUT} = 3A
Figure 11. Switching Waveform in CCM Operation



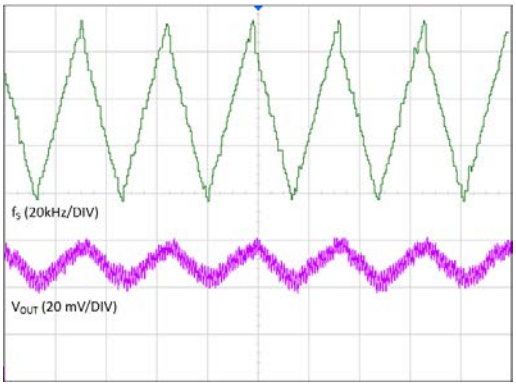
Time (100 ms/DIV)
LN10043Q1, V_{IN} = 12V, I_{OUT} = 0A
Figure 12. Switching Waveform in PFM Operation



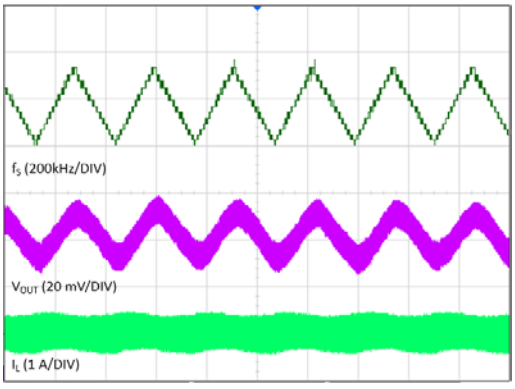
Time (50 µs/DIV)
LN10043Q1, V_{IN} = 5V, I_{OUT} = 3A
Figure 13. Switching Waveform in Dropout Operation



Time (5 µs/DIV)
LN10143Q1, F_S = 400kHz, V_{IN} = 12V, I_{OUT} = 0A
Figure 14. Switching Waveform in FPWM Operation



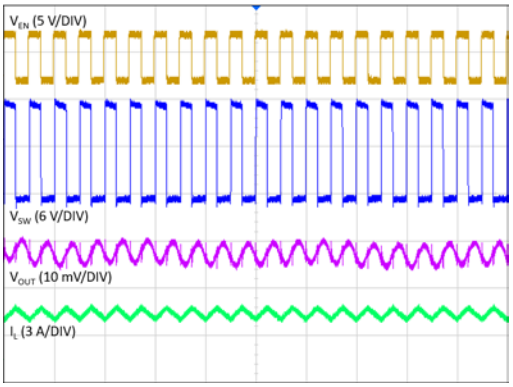
Time (50 µs/DIV)
LN10143Q1S, F_S = 400kHz, V_{IN} = 12V, I_{OUT} = 0A
Figure 15. Switching Waveform in SPREAD SPECTRUM MODULATION



Time (50 µs/DIV)
LN10543Q1S, F_S = 2.1MHz, V_{IN} = 12V, I_{OUT} = 0A
Figure 16. Switching Waveform in SPREAD SPECTRUM MODULATION

Typical Waveforms (Continued)

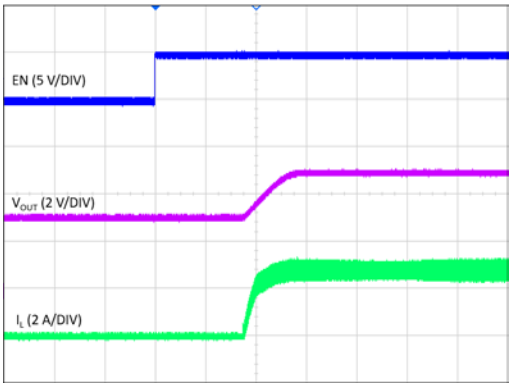
Unless otherwise stated, the test conditions are: V_{IN} = 12V, V_{OUT} = 5V, F_S = 400kHz, L = 10µH, C_{OUT} = 100uF, T_A = 25 ˚C.



Time (5 µs/DIV)

LN10043Q1, F_S = 400kHz, V_{IN} = 12V, I_{OUT} = 3A

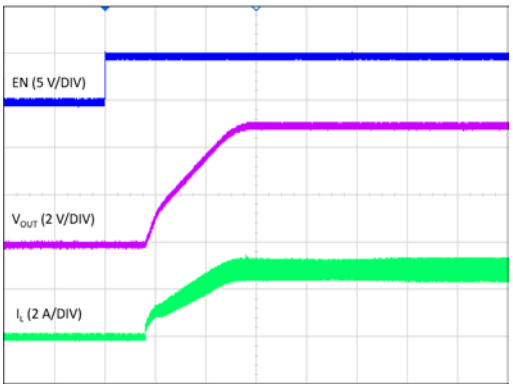
Figure 17. Sync to External Clock



Time (1 ms/DIV)

LN10043Q1, F_S = 400kHz, V_{IN} = 12V, I_{OUT} = 3A

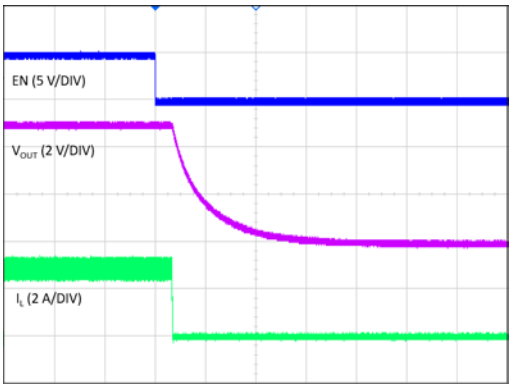
Figure 18. Startup with Pre-Charged Voltage



Time (1 ms/DIV)

LN10043Q1, F_S = 400kHz, V_{IN} = 12V, I_{OUT} = 3A

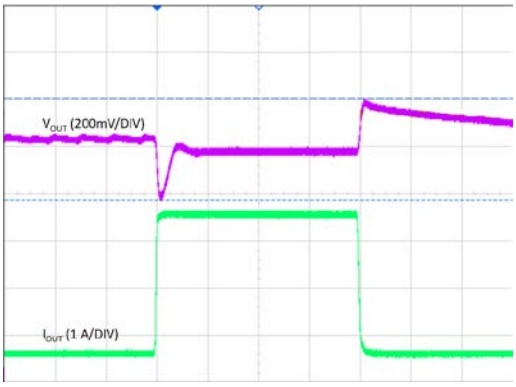
Figure 19. Startup through EN



Time (200 µs/DIV)

LN10043Q1, F_S = 400kHz, V_{IN} = 12V, I_{OUT} = 3A

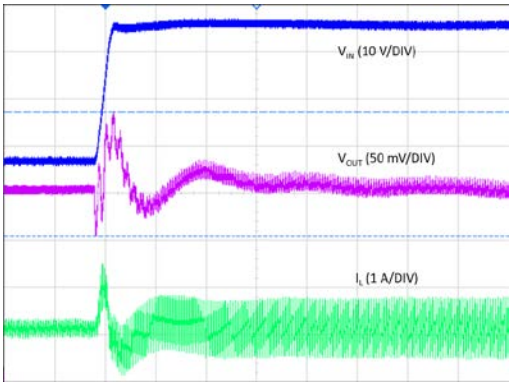
Figure 20. Shutdown through EN



Time (100 µs/DIV)

LN10043Q1, F_S = 400kHz, V_{IN} = 12V

Figure 21. Load Transient 0.0 <-> 3.0A, Slew Rate = 0.3A/µs



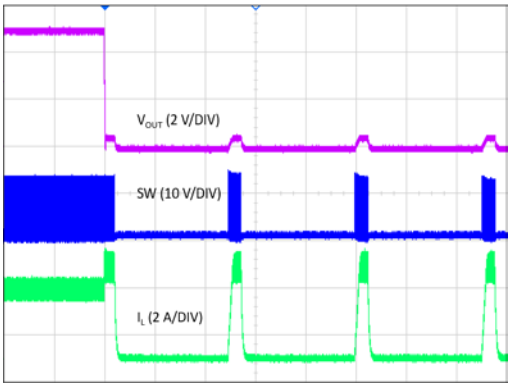
Time (50 µs/DIV)

LN10043Q1, F_S = 400kHz, I_{OUT} = 3A

Figure 22. VIN Transient 7V <-> 36V, Slew Rate = 3V/µs

Typical Waveforms (Continued)

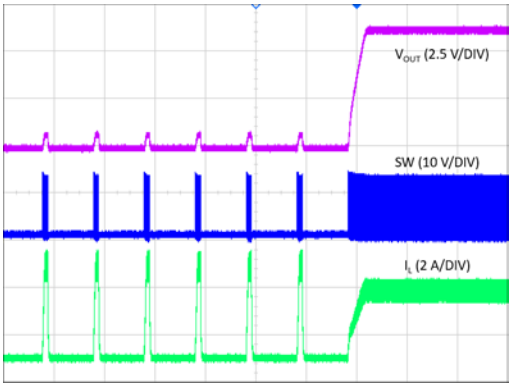
Unless otherwise stated, the test conditions are: V_{IN} = 12V, V_{OUT} = 5V, F_S = 400kHz, L = 10µH, C_{OUT} = 100uF, T_A = 25 ˚C.



Time (2 ms/DIV)

LN10043Q1, F_S = 400kHz, V_{IN} = 12V, I_{OUT} = 3A to SCP

Figure 23. Into Output Short and Hiccup



Time (5 ms/DIV)

LN10043Q1, F_S = 400kHz, V_{IN} = 12V, I_{OUT} = SCP to 3A

Figure 24. Out of Output Short and Recovery

8 FUNCTIONAL DESCRIPTION

8.1 Overview

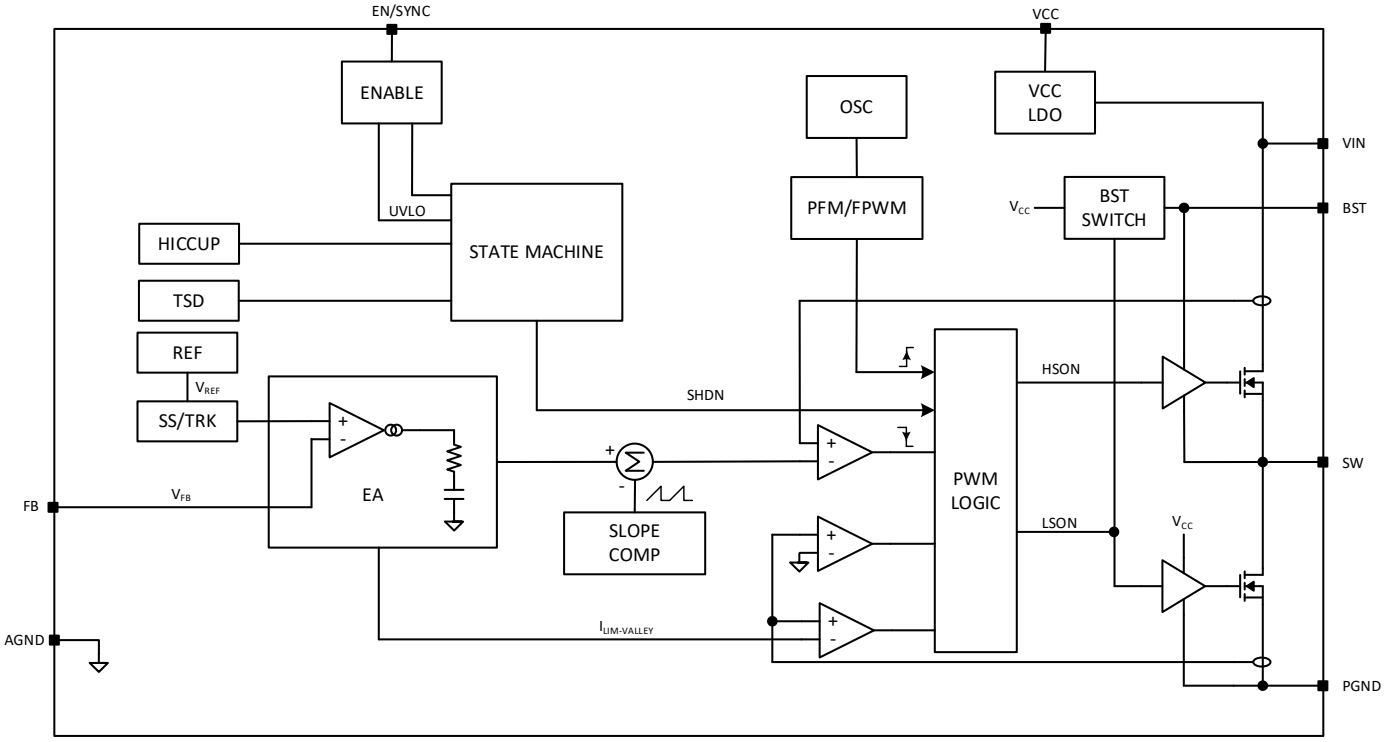
The LN10X43Q1 is a high efficiency, compact, synchronous step-down DC-DC converter employing a constant frequency, peak current mode control architecture with internal compensation. It operates from an input voltage from 3.5V to 36V, provides an adjustable output voltage from 1V to V_{IN}. LN10X43Q1 can deliver up to 3.0A.

The LN10X43Q1 has three frequency options: 400kHz, 1MHz and 2.1MHz, or synchronization with an external clock range from 200kHz to 2.1MHz. With a low minimum on-time, it enables a very compact solution with small inductor and capacitor size and offers constant-frequency operation with very high step-down ratio. In addition, the LN10X43Q1 achieves the lowest possible dropout voltage with 100% maximum duty cycle operation. During light load operation, LN10043Q1, LN10243Q1 and LN10443Q1 operate at DCM and PFM to maximize efficiency. LN10143Q1, LN10343Q1 and LN10543Q1 are forced to operate at CCM mode even under zero load.

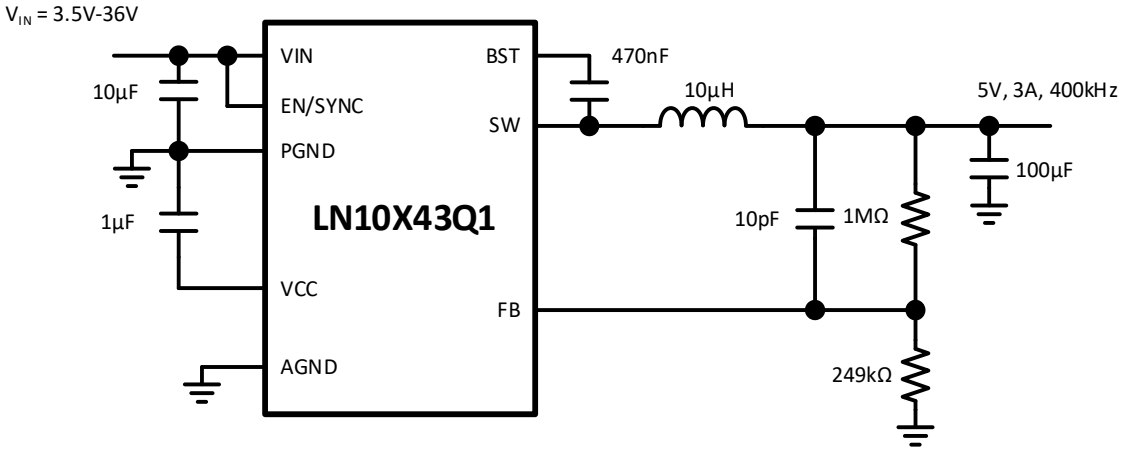
The LN10X43Q1 also offers a plural of features include programmable output voltage, internal soft start, cycle-by-cycle peak and valley current limit, output short circuit protection with hiccup mode, over temperature shutdown and recovery, and adjustable system UVLO.

The LN10X43Q1S offers a spread spectrum feature to optimize EMI performance. Emissions at the operating frequency and its sub-harmonics are mitigated by spreading the single-point operating frequency over an extended range.

8.2 Funtional Diagram



8.3 Application Diagram with Full Features



8.4 Funtional Description

8.4.1 Voltage Regulation Loop and FB pin

The LN10X43Q1 employs a peak current mode control to regulate the output voltage. For highly efficient operation cross the whole load range. The LN10043Q1, LN10243Q1 and LN10443Q1 utilizes Discontinuous Conduction Mode (DCM) and Pulse Frequency Modulation (PFM) at light load.

To adjust the output voltage, connect a voltage divider between V_{OUT} and GND, and connect the center of the divider to FB pin. The steady state V_{FB} is typically 1V. The output voltage can be derived from:

$$V_{OUT} = (1 + \frac{R_{FBT}}{R_{FBB}}) \times V_{FB}$$

Based on the output voltage requirements, the above equation can be re-written as:

$$R_{FBB} = \frac{V_{FB}}{V_{OUT} - V_{FB}} \times R_{FBT}$$

In general, R_{FBT} < 1MΩ is recommended. The tolerance of the divider resistance should be less than 1%, and the temperature coefficients should be less than 100ppm.

The LN10X43Q1 uses an internal compensation scheme to stabilize the control loop, an external RC lead compensation network can be connected between VOUT and FB to improve transient response. An external lead compensation can be achieved by adding a capacitor in parallel with the upper leg resistor of the voltage divider between V_{OUT} and FB pins.

The zero frequency of the external lead compensator is at:

$$f_z = \frac{1}{2\pi \times R_{FBT} \times C_{LEAD}}$$

While the pole frequency of the external lead compensator is at:

$$f_p = \frac{1}{2\pi \times (R_{FBT} // R_{FBB}) \times C_{LEAD}}$$

The added external lead compensator can increase the loop gain by $(1 + \frac{R_{FBT}}{R_{FBB}})$.

8.4.2 Internal V_{CC} Regulators, VCC Pin

V_{CC} powers the internal control circuits and the gate drivers for the internal power MOSFETs. VCC must be decoupled to PGND with a 1 -4.7µF ceramic capacitor.

8.4.3 V_{IN} UVLO and EN/SYNC Pin

An accurate threshold is placed at $EN_{VOUT-ON}$, when EN rises above this threshold, it turns on the switching regulator. This accurate threshold serves to provide an accurate system V_{IN} UVLO level. In the application, an enable divider can be added between V_{IN} and GND. The switching regulator can thus be turned on and off at programmable precise input voltages. The VIN UVLO threshold can be determined by:

$$V_{IN-RISING} = (1 + \frac{R_{ENT}}{R_{ENB}}) \times EN_{VOUT-ON}$$

8.4.4 Synchronization to External Clock and EN/SYNC Pin

LN10X43Q1 is capable of being synchronized to an external clock between 200kHz to 2.1MHz. Connect the external clock signal to EN/SYNC pin.

8.4.5 Over-Current Protection

8.4.5.1 Peak Current Protection

Peak current protection is a cycle-by-cycle protection inherited from the peak current mode control. The peak current command is clamped to the Peak Current Limit Threshold.

8.4.5.2 Valley Current Protection

During low side conduction, the low side power MOSFET current is sensed and compared to valley current threshold. When low side current is higher than the valley current threshold, high side power MOSFET is not allowed to turn on for the next cycle.

8.4.5.3 Hiccup Mode

When low side current is higher than the valley current threshold for 32 cycles, it shuts down the switching regulator. The switching regulator automatically turns back on after 5ms if EN is high. When the switching regulator turns back on, the regulator goes through the soft start process.

8.4.6 Thermal Shutdown and Auto-Recovery

When the junction temperature exceeds 170˚C, LN10X43Q1 shuts down the switching regulator to reduce thermal dissipation. It automatically restarts the switching regulator after junction temperature drops back below 160 ˚C. The VCC LDO regulators remain operational during over-temperature event.

8.4.7 Bootstrap Voltage, BST and SW Pin

The internal gate driver for the high side Power MOSFET uses a bootstrapped supply from an external capacitor C_{BST} connected between BST pin and SW. The voltage on C_{BST} is charged from V_{CC} through an internal switch when the low side power MOSFET conducts.

8.4.8 Low Drop-Out

When input voltage is close to the output target voltage, LN10X43Q1 enters Low Drop-Out mode. The high-side MOSFET can be turned on for more than a switching period to maintain the output voltage regulation. When the input voltage is lower than the target voltage, the high-side power MOSFET is turned on for maximum allowable on time: $t_{REFRESH-PER}$. The low-side power MOSFET turns on briefly for $t_{REFRESH-PUL}$ to refresh the charge on C_{BST}.

9 APPLICATION INFORMATON

9.1 Typical Applications

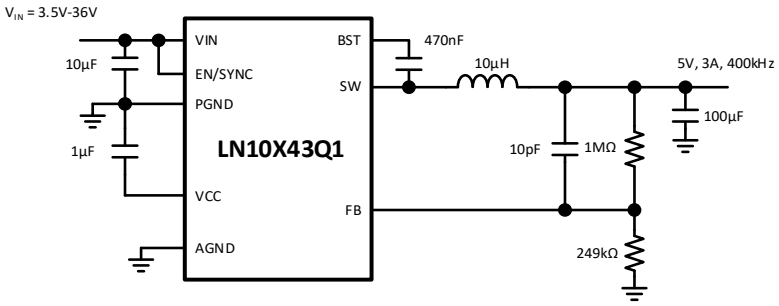


Figure 23. LN10X43Q1, 400kHz, 5V, 3A Typical Application Diagram

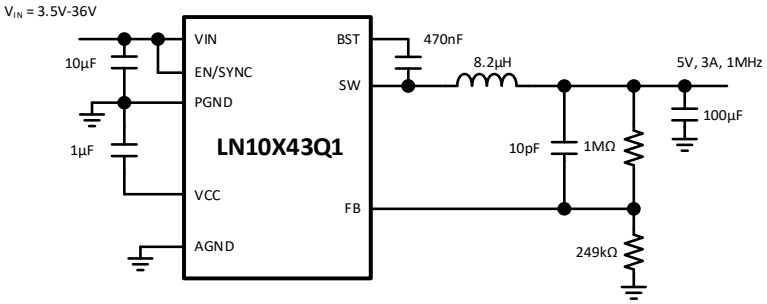


Figure 24. LN10X43Q1, 1MHz, 5V, 3A Typical Application Diagram

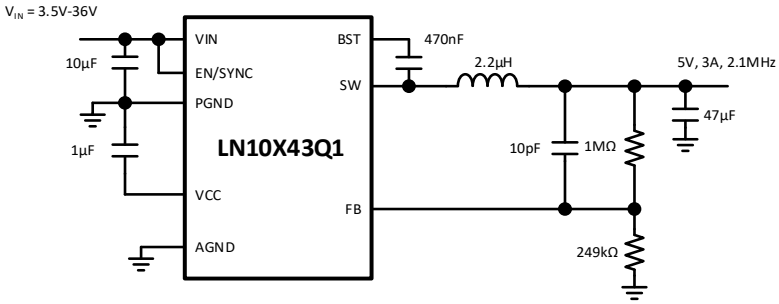


Figure 25. LN10X43Q1, 2.1MHz, 5V, 3A Typical Application Diagram

10 LAYOUT

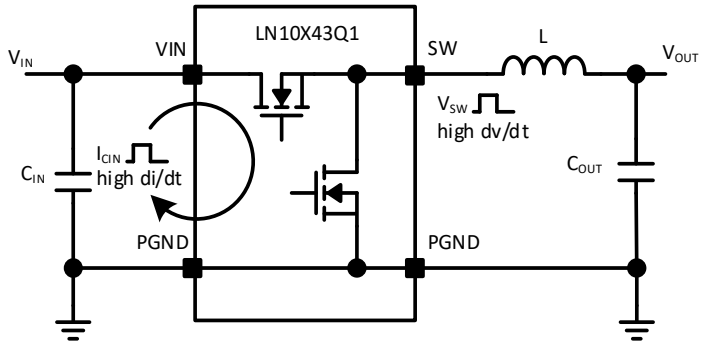
10.1 Layout Guidelines

The performance of any switching converter depends as much upon the layout of the PCB as the component selection. The LN10X43Q1 is designed to meet the optimization requirements of PCB layout in the pin assignment. For example, VIN and PGND pins are adjacent to each other, which is convenient for placing VIN bypass capacitors.

Radiated EMI is generated by the high di/dt components in pulsing currents in switching converters. The larger area covered by the path of a pulsing current; the more electromagnetic emission is generated. As shown in the figure below, this part of the current flows from the VIN side of the input capacitors to high side switch, to the low side switch, and then returns to the ground of the input capacitors.

The key to minimize radiated EMI is to minimize the area of this pulsing current path, thus, placing high frequency ceramic bypass capacitor(s) as close as possible to the VIN and PGND pins is necessary.

In addition, high dv/dt occurs on SW node during switching, so the trace between SW pin and inductor should be as short as possible, and just wide enough to carry the load current without excessive heating. Short and thick traces are highly recommended to minimize parasitic resistance. Besides, sensitive signal lines should be kept away from SW traces.



The following guidelines will help users design a PCB with the best power conversion performance, thermal performance, and minimized generation of unwanted EMI.

1. Place high frequency ceramic bypass C_{IN} as close as possible to the LN10X43Q1 VIN and PGND pins; a ceramic capacitor in small package (such as 0603) is still needed even if multiple input capacitors are implemented;

2. The high-current loop consisting of VIN, SW, VOUT and GND should be as compact as possible;

3. The bypass capacitors of VCC should be arranged close to the pins, and return to the PGND pin with the shortest connection;

4. It is recommended to use a four-layer board with a top and bottom layer of 2oz copper, and a complete ground plane on middle layer. Use a minimum 2 by 4 arrays of 0.2-millimeter thermal vias to connect the thermal pad of LN10X43Q1 to the system ground plane for heat sinking;

5. The SW and BST nodes contains a lot of high-frequency noise, so
the connection of the pins should be as short as possible, meanwhile, there should be sufficient width to conduct the current;

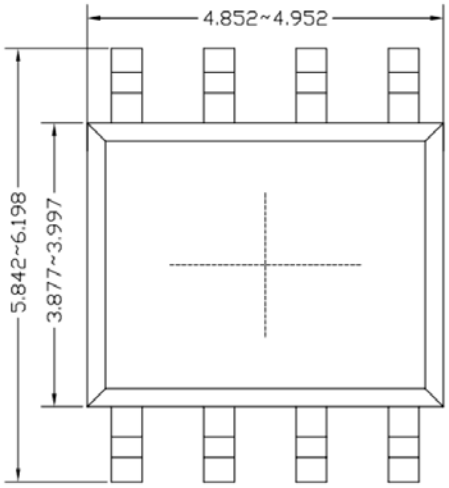
6. Sensitive analog signals, such as FB, need to be far away from the noisy nodes, ground plane can be used as a shielding layer while routing these sensitive signals;

7. The feedback resistance of the FB connection must be located as close to the pin as possible, If V_{OUT} accuracy at the load is important, make sure V_{OUT} sense is made at the load;

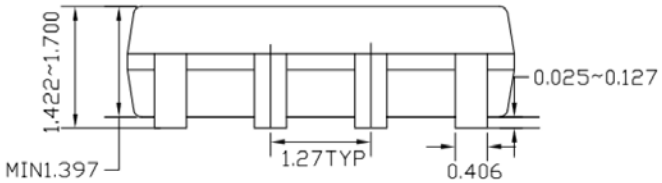
8. For the peripheral components connected to FB and EN pins, a single point ground connection to the plane is recommended.

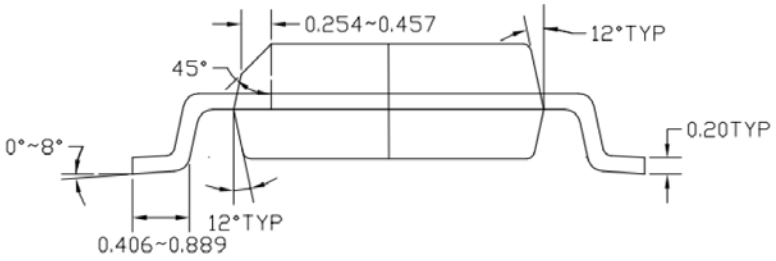
11 PACKAGE INFORMATION

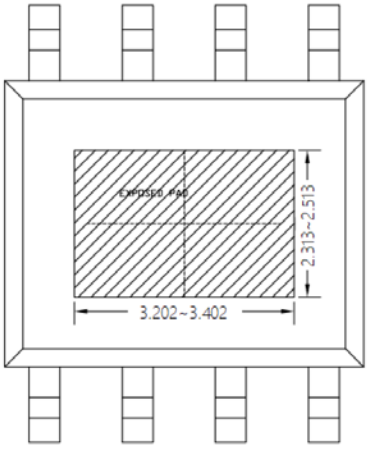
11.1 Package Outline



TOP VIEW







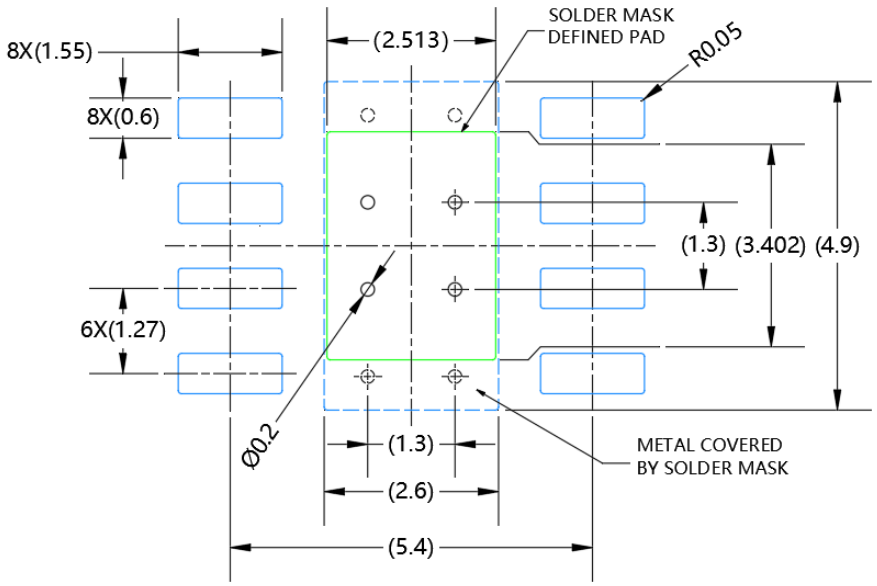
BOTTOM VIEW

Notes:

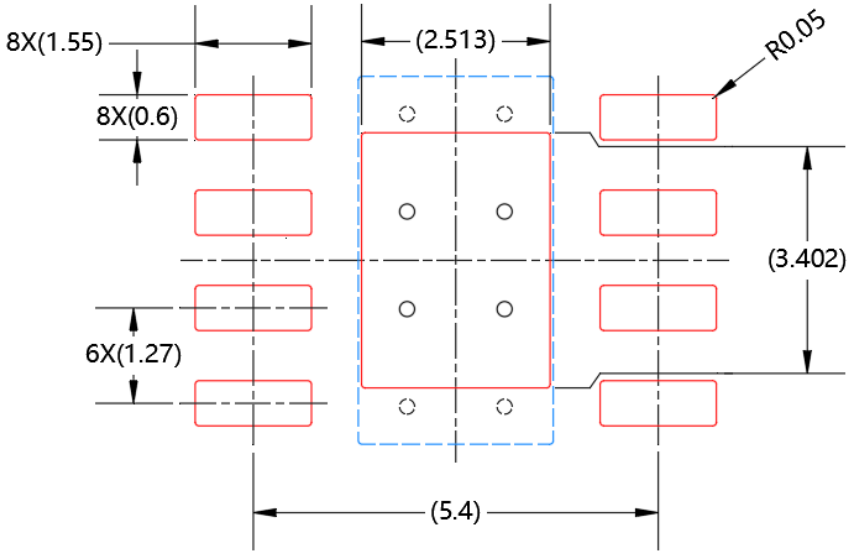
1. Both package length and width do not include mold flash.
2. Controlling dimension: mm
3. Reference JEDEC MS-013, MS-012
4. The size label of length and width in the drawing belong to the bottom size of the package.

11.2 Footprint Example

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL



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