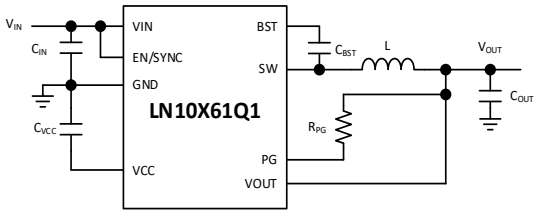
60V, 0.6A/1A/1.5A, Synchronous Step-Down Regulator

1 FEATURES

- AEC-Q100 Grade 1 Qualified for automotive applications
- Wide V_{IN} Range: 3.5V to 60V
- ±2%, 3.3V and 5V Fixed Outputs or 1V to V_{IN} Adjustable Output
- Integrated both High-Side and Low-Side Power MOSFETs with up to 1.5A Output Capability
- Frequency Options: 400kHz, 1MHz, 2.1MHz
- High Efficiency PFM Operation
- Near 100% Duty Cycle Operation for Low Drop Out Operation
- Power Good Indicator
- PLL Synchronization to External Clock
- Accurate Peak and Valley Clamp
- Internal Compensation
- Output Short-Circuit Protection with Hiccup Mode
- Accurate VIN UVLO Protection
- Over-Temperature Shutdown and Recovery
- Operating Junction Temperature -40˚C to 150 ˚C
- Thermally Enhanced SOIC-EP8 Package (4.9mm X 3.9mm)

2 APPLICATIONS

- Automotive Power Supplies
- Industrial Power Supplies
- Battery Powered Systems



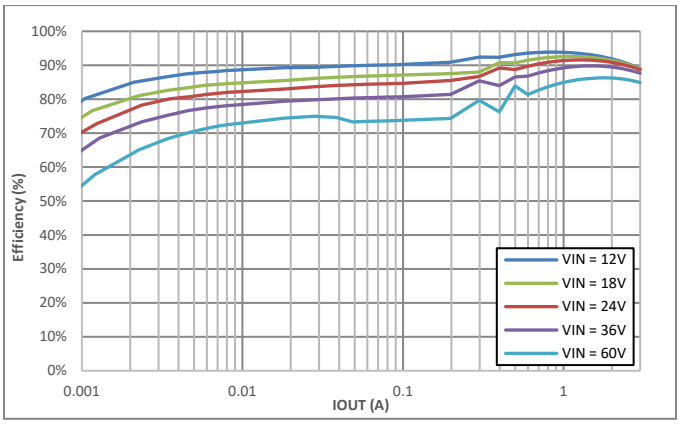
Typical Application Diagram

3 DESCRIPTION

The LN10X61Q1 is a high efficiency, compact, synchronous step-down DC-DC converter employing a constant frequency, peak current mode control architecture with internal compensation. It operates from an input voltage from 3.5V to 60V and integrates both high-side and low-side power MOSFETs with up to 0.6A/1A/1.5A output capability. The nominal switching frequency is fixed on 400kHz, 1MHz or 2.1MHz, or can be synchronized to an external clock. Automatic frequency foldback at light load improves efficiency.

The LN10X61Q1 with VOUT pin provides a fixed output of 3.3V or 5V, and can achieve higher output accuracy, minimum number of peripheral components as well as lower quiescent current and higher system efficiency. The LN10X61Q1 with FB pin provides an adjustable output voltage from 1V to VIN.

Additional features such as precision enable, power good indicator and internal soft start provide both flexible and easy to use solutions for a wide range of applications. Full protection features include input UVLO, over temperature shutdown, cycle-by-cycle current limit, and short-circuit protection.



LN10161Q1-12-EFR, Effciency Curve

Table of Contents

4 REVISION HISTORY

Version	Change Description	Date
1.0	Initial Version	2022/01/25
1.1	Update Package Information ·····P28	2022/04/26

5 PRODUCT AND ORDER INFORMATION

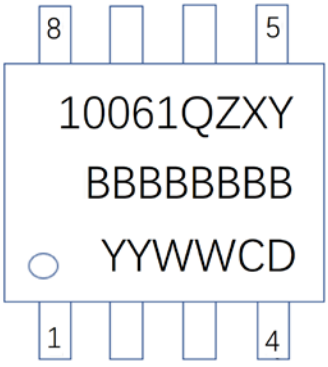
5.1 Product Information

Part Number	Function	X	Y	Z	IC Package	MSL-Peak-Temp (1)	Material	Package / Qty	Top Marking (3)
LN10061Q1ZXY	Fixed V_{OUT}, Adjustable frequency	1: 1.5A, PFM 2: 1A, PFM 3: 0.6A, PFM	1: 3.3V 2: 5V	-: Normal S: SST (2)	SOIC-EP8	Level-3-260C	RoHS	Tape & Reel / 3000	10061QZXY
LN10161Q1ZXY	Fixed V_{OUT}, Fixed frequency, PG		1: 3.3V, 400kHz 2: 5V, 400kHz 3: 3.3V, 1MHz 4: 5V, 1MHz 5: 3.3V, 2.1MHz 6: 5V, 2.1MHz	-: Normal S: SST (2)	SOIC-EP8	Level-3-260C	RoHS	Tape & Reel / 3000	10161QZXY
LN10261Q1ZXY	Adjustable V_{OUT}, Adjustable frequency		1	-: Normal S: SST (2)	SOIC-EP8	Level-3-260C	RoHS	Tape & Reel / 3000	10261QZXY
LN10361Q1ZXY	Adjustable V_{OUT}, Fixed frequency, PG		1: 400kHz 2: 1MHz 3: 2.1MHz	-: Normal S: SST (2)	SOIC-EP8	Level-3-260C	RoHS	Tape & Reel / 3000	10361QZXY

(1) MSL (Moisture Sensitivity Level) and the highest solder temperature are based on JEDEC industrial standard.

(2) Part numbers with **SPREAD SPECTRUM (SST)** function.

(3) Top Marking:



Line 1: Product Mark Code

Line 2: Lot ID

Line 3: Date Code

5.2 Order Information

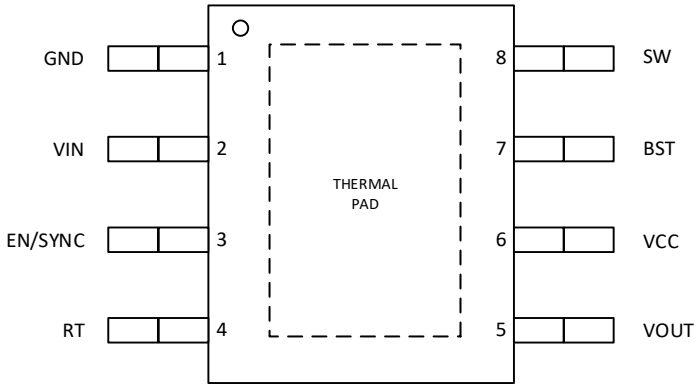
Part Number	Output	Output Current	Frequency	PG	Spread Spectrum	Package	Package Qty
LN10161Q1-11-EFR	3.3V	1.5A	Fixed，400kHz	Yes	No	Tape & Reel	3000
LN10161Q1-12-EFR	5V	1.5A	Fixed，400kHz	Yes	No	Tape & Reel	3000
LN10261Q1-11-EFR	Adjustable V_{OUT}	1.5A	Adjustable Frequency 200k~2.5MHz	No	No	Tape & Reel	3000
LN10161Q1S11EFR	3.3V	1.5A	Fixed，400kHz	Yes	Yes	Tape & Reel	3000
LN10161Q1S12EFR	5V	1.5A	Fixed，400kHz	Yes	Yes	Tape & Reel	3000
LN10261Q1S11EFR	Adjustable V_{OUT}	1.5A	Adjustable Frequency 200k~2.5MHz	No	Yes	Tape & Reel	3000

6 PIN CONFIGURATION

6.1 Pin Configuration

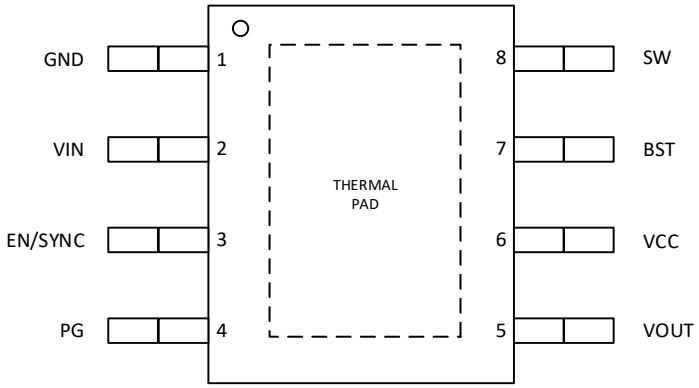
6.1.1 LN10061Q1 with VOUT and RT pins

SOIC-EP8 Top View



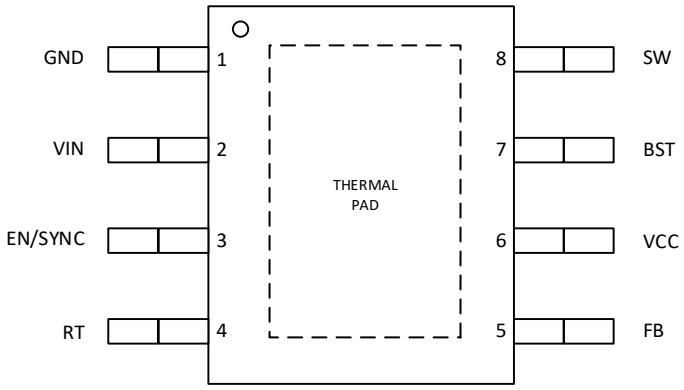
6.1.2 LN10161Q1 with VOUT and PG pins

SOIC-EP8 Top View



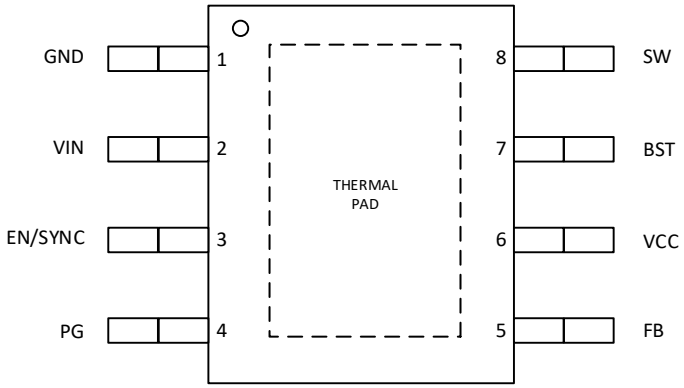
6.1.3 LN10261Q1 with FB and RT pins

SOIC-EP8 Top View



6.1.4 LN10361Q1 with FB and PG pins

SOIC-EP8 Top View



6.2 Pin Functions

Number	PIN Name				Type	Description
	10061	10161	10261	10361		
1	GND				Ground	Power ground. Connect the pin to ground plane.
2	VIN				Power	Power supply input pin to high side power MOSFET and V_{IN} LDO regulator. Decouple this pin to GND with ceramic capacitors.
3	EN/SYNC				Signal	Enable pin for V_{CC} LDOs, regulator output, and input voltage for V_{IN} UVLO. Connect to V_{IN} directly, to V_{IN} through a divider, or to an external voltage source. This pin is also used for external clock synchronization.
4		PG		PG	Signal	Open-drain power good output. V_{FB} is monitored and when V_{FB} is not within the regulation window. PG pin is pulled low.
	RT		RT		Signal	Switching frequency control pin. Place a resistor between this pin and GND to set the switching frequency between 200kHz and 2.5MHz.
5	VOUT	VOUT			Signal	Output voltage feedback, connect to the system output directly. This pin is also used as the second input of internal LDO, decouple this pin to GND with ceramic capacitors.
			FB	FB	Signal	Output voltage feedback input. Use an external divider to set the desired output voltage.
6	VCC				Power	Voltage source that powers the gate drivers of the internal power MOSFETs and control circuits. Must be decoupled to GND with 1µF to 4.7µF ceramic capacitor. This voltage source is provided by one of the two internal LDO regulators with input from V_{IN} or V_{OUT}.
7	BST				Power	Bootstrapped supply to the high side gate driver. Connect a 100nF to 470nF ceramic capacitor between BST and SW pins.
8	SW				Power	Switch node connection from the internal power MOSFETs to the external inductor.
THERMAL PAD	-				-	Thermal dissipation pad. Solder to ground plane.

7 SPECIFICATIONS

7.1 Absolute Maximum Ratings

Parameters	Min	Max	Unit
VIN to GND	-0.3	65	V
EN/SYNC to GND	-0.3	V_{IN}	
FB to GND	-0.3	5.5	
VCC to GND	-0.3	5.5	
PG to GND	-0.3	36	
RT to GND	-0.3	5.5	
VOUT to GND	-0.3	36	
SW to GND	-1.0	V_{IN}+0.3	
SW to GND （Overshoot voltage less than 10ns）	-3.5	65	
BST to SW	-0.3	5.5	
Ambient Temperature	-40	125	˚C
Junction Temperature	-40	150	
Storage Temperature	-65	150	

7.2 ESD Ratings

Parameters	Min	Max	Unit
HBM Human Body Model		±3000	V
CDM Charge Device Model		±750	

7.3 Recommented Operating Condition

Parameters	Min	Max	Unit
VIN	3.5	60	V
EN/SYNC	-0.3	V_{IN}	
FB	-0.3	1.1	
PG	-0.3	30	
IOUT （1.5A version）	0	1.5	A
IOUT （1.0A version）	0	1.0	
IOUT （0.6A version）	0	0.6	
Ambient temperature	-40	125	˚C
Junction temperature	-40	150	

7.4 Package Thermal Parameters

Parameters (1)		SOIC-EP8	Units
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance	39	˚C/W
ψ_{JT}	Junction-to-Top Characterization Parameter	6	˚C/W

(1) Measurements are based on standard 2s2p PCB defined in JESD 51-7 2s2p, under no wind , 2W loss, and 25 ˚C ambient temperature.

7.5 Electrical Characteristics

Unless otherwise stated, the minimum and maximum limits are applied over the recommended operating junction temperature range of -40˚C to 150˚C. Typical values are measured at 25˚C and represent the most likely norm. The default conditions are applied: V_{IN} = 24V, V_{OUT} = 5V, F_S = 400kHz.

SYMBOL	PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY VOLTAGE (VIN PIN)						
V_{IN}	Operating Input Voltage Range		3.5		60	V
$I_{Q-5V-PFM}$	During Regulation in PFM	V_{EN} = 5V, V_{IN} = 24V, I_{OUT} = 0A		19		μA
$I_{Q-3.3V-PFM}$	During Regulation in PFM	V_{EN} = 5V, V_{IN} = 24V, I_{OUT} = 0A		12		μA
$I_{Q-ADJ-PFM}$	During Regulation in PFM	V_{EN} = 5V, V_{IN} = 24V, I_{OUT} = 0A		70		μA
I_{SHDN}	Shutdown Quiescent Current	V_{EN} = 0V, V_{IN} = 24V		1.2		μA
FB PIN						
V_{FB}	Regulated Feedback Voltage in CCM Mode	V_{IN} = 3.5V to 60V, T_J = 25˚C	0.992	1	1.008	V
		V_{IN} = 3.5V to 60V, T_J = 25˚C to 150 ˚C	0.98	1	1.02	V
I_{Q-FB}	Feedback Input Leakage Current	V_{FB} = 1V		0	100	nA
VOUT PIN						
$V_{VOUT-5V}$	Regulated VOUT Voltage	Full V_{IN} Range, Full Load Range, @25˚C	4.96	5	5.04	V
		Full V_{IN} Range, Full Load Range, Full Operational Temperature Range	4.9	5	5.1	V
$V_{VOUT-3.3V}$	Regulated VOUT Voltage	Full V_{IN} Range, Full Load Range, @25˚C	3.27	3.3	3.33	V
		Full V_{IN} Range, Full Load Range, Full Operational Temperature Range	3.23	3.3	3.37	V
PWM (1)						
T_{ON-MIN}	Minimum ON Time	Guaranteed by design		150		ns
$T_{OFF-MIN}$	Minimum OFF Time	Guaranteed by design		250		ns
POWER MOSFETS (2)						
$R_{DSON-HS}$	High Side MOSFET ON Resistance	I_{OUT} = 0.5A, V_{BST} - V_{SW} = 5V		346	650	mΩ
$R_{DSON-LS}$	Low Side MOSFET ON Resistance	I_{OUT} = 0.5A, V_{CC} = 5V		200	400	mΩ

(1) Guaranteed by design.

(2) Measured at pins.

Electrical Characteristics（Continued）

Unless otherwise stated, the minimum and maximum limits are applied over the recommended operating junction temperature range of -40˚C to 150˚C. Typical values are measured at 25˚C and represent the most likely norm. The default conditions are applied: V_{IN} = 24V, V_{OUT} = 5V, F_S = 400kHz.

OSCILLATOR (3)						
$F_{S-400kHz}$	PWM Switching Frequency	V_{IN} = 24V, V_{OUT} = 5V	320	400	480	kHz
$F_{S-1000kHz}$	PWM Switching Frequency	V_{IN} = 24V, V_{OUT} = 5V		1000		kHz
$F_{S-2100kHz}$	PWM Switching Frequency	V_{IN} = 12V, V_{OUT} = 5V		2100		kHz
RT (RT PIN) (4)						
$F_{S-RT-400kHz}$	PWM Switching Frequency	V_{IN} = 24V, V_{OUT} = 5V, R_T = 232kOhm	320	400	480	kHz
$F_{S-RT-1000kHz}$	PWM Switching Frequency	V_{IN} = 24V, V_{OUT} = 5V, R_T = 71.5kOhm		1000		kHz
$F_{S-RT-2500kHz}$	PWM Switching Frequency	V_{IN} = 12V, V_{OUT} = 5V, R_T = 12.4kOhm		2500		kHz
SPREAD SPECTRUM (SST) (5)						
$\%\Delta F_S$	Spread Spectrum Modulation Frequency Range			-17		%
F_{SST}	Spread Spectrum Modulation Frequency			16		kHz
ENABLE V_{IN} UVLO (EN PIN)						
$EN_{VOUT-ON}$	V_{IN} UVLO Rising Threshold	V_{EN} Rising	1.9	2.08	2.25	V
$EN_{VOUT-HYS}$	V_{IN} UVLO Hysteresis	V_{EN} Falling		250		mV
EN_{VCC-ON}	V_{EN} High-Level Threshold	V_{EN} Rising	1.8			V
$EN_{VCC-OFF}$	V_{EN} Low-Level Threshold	V_{EN} Falling			0.4	V
I_{Q-EN}	EN Pin Current	V_{EN} = 3.3V		0	0.2	μA
INTERNAL VCC LDOS (VCC, VIN, VOUT PINS)						
$V_{CC-TARGET}$	V_{CC} Regulation Target			4.75		V
BOOTSTRAP (BST PIN) (1)						
t_{ON-MAX}	Auto-Refresh Period			9		μs
INTERNAL SOFT START (6)						
t_{SS-INT}	Internal Soft-Start Time			6.6	10	ms

(3) This parameter is for LN10161Q1ZXY and LN10361Q1ZXY both with internal fixed frequency.

(4) This parameter is for LN10061Q1ZXY and LN10261Q1ZXY both with externally adjustable frequency

(5) This parameter is only available on part numbers with spread spectrum function.

(6) Measured from $EN_{VOUT-ON}$ to internal soft start completed.

Electrical Characteristics（Continued）

Unless otherwise stated, the minimum and maximum limits are applied over the recommended operating junction temperature range of -40˚C to 150˚C. Typical values are measured at 25˚C and represent the most likely norm. The default conditions are applied: V_{IN} = 24V, V_{OUT} = 5V, F_S = 400kHz.

OVER CURRENT PROTECTION (7)(8)						
$I_{PEAK-1.5A}$	Peak Current Limit Threshold	V_{IN} = 24V, V_{OUT} = 5V	1.75	2.2	2.5	A
$I_{VALLEY-1.5A}$	Valley Current Limit Threshold	V_{IN} = 24V, V_{OUT} = 5V	1.15	1.6	1.95	A
$I_{PEAK-1.0A}$	Peak Current Limit Threshold	V_{IN} = 24V, V_{OUT} = 5V		1.6		A
$I_{VALLEY-1.0A}$	Valley Current Limit Threshold	V_{IN} = 24V, V_{OUT} = 5V		1.1		A
$I_{PEAK-0.6A}$	Peak Current Limit Threshold	V_{IN} = 24V, V_{OUT} = 5V		1.0		A
$I_{VALLEY-0.6A}$	Valley Current Limit Threshold	V_{IN} = 24V, V_{OUT} = 5V		0.65		A
POWER GOOD (PG and FB PINs)						
$\%V_{PG-OV}$	Power Good Over-Voltage Rising Threshold	V_{FB} Ramping Up	105	110	115	%
$\%V_{PG-OV-HYS}$	Power Good Over-Voltage Recovery Hysteresis	% Of PG Voltage		5.5		%
$\%V_{PG-UV}$	Power Good Under-Voltage Falling Threshold	V_{FB} Ramping Down	82	87	92	%
$\%V_{PG-UV-HYS}$	Power Good Under-Voltage Recovery Hysteresis	% Of PG Voltage		3.7		%
V_{PG-PD}	Power Good Pull-Down Strength	I_{PG} = 1mA， V_{EN} = 3.3V		40	100	mV
$t_{PG-RISING}$	Power Good Flag Rising Delay			300		μs
$t_{PG-FALLING}$	Power Good Flag Falling Delay			310		μs
THERMAL SHUTDOWN (1)						
OT	Thermal Shutdown Threshold			170		˚C
OT_{HYS}	Thermal Shutdown Recovery Hysteresis			-10		˚C

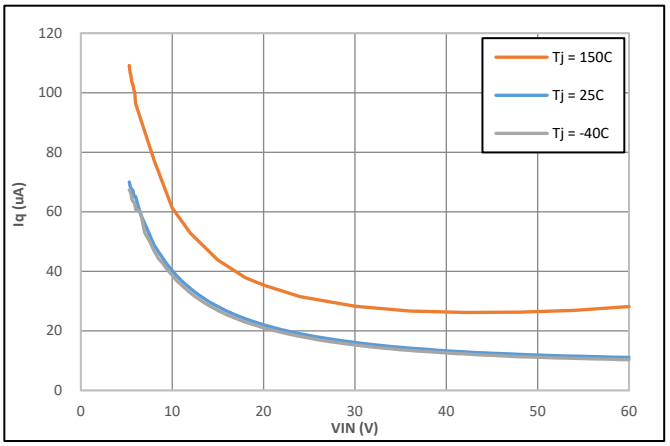
(7) This current limit was tested as the internal comparator trigger point, the current limits measured in a closed loop application may be different.

(8) Subscripts indicate different output current capabilities in the product family.

7.6 Typical Characteristics

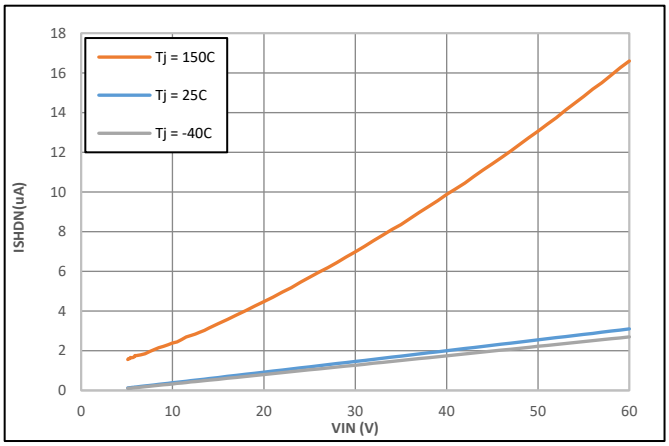
7.6.1 Characteristics Over Temperature

Unless otherwise stated, the test conditions are the same as Chapter 7.5. T_J = -40˚C to 150˚C.



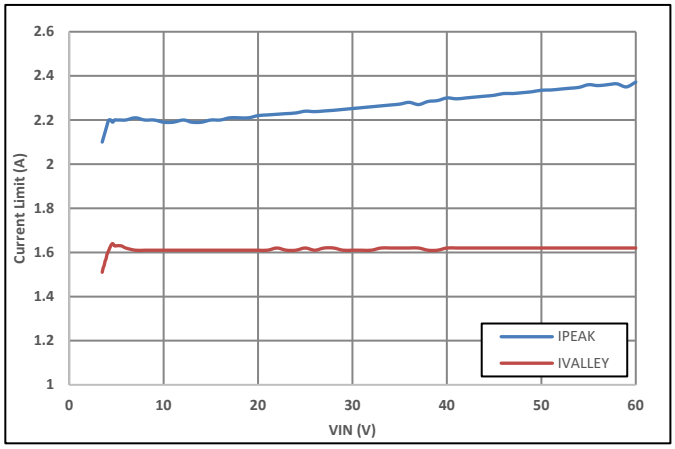
LN10161Q1-12, EN = 5V, V_{OUT} = 5V, No load

Figure 1. Operating Quiescent Current I_Q



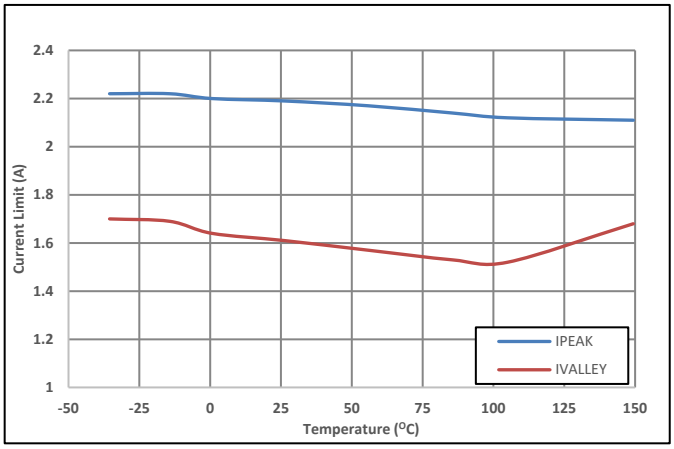
LN10161Q1-12, V_{EN} = 0V

Figure 2. Shutdown Current I_{SHDN}



LN10161Q1-12, PFM, F_S = 400kHz, V_{OUT} = 5V

Figure 3. Peak Current and Valley Current Limit Vs. V_{IN}

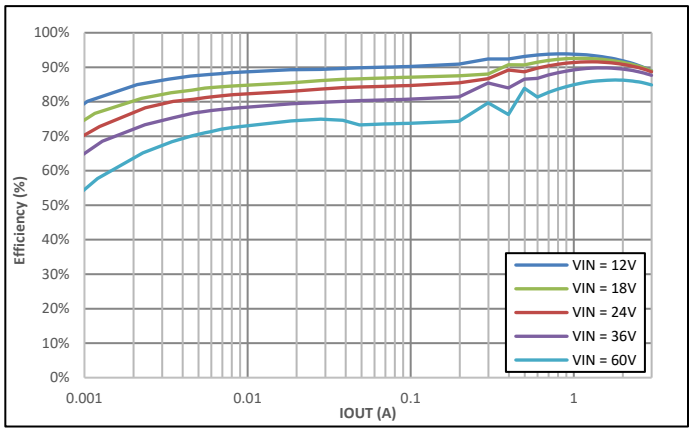


LN10161Q1-12, PFM, F_S = 400kHz, V_{OUT} = 5V

Figure 4. Peak Current and Valley Current Limit Vs. Temperature

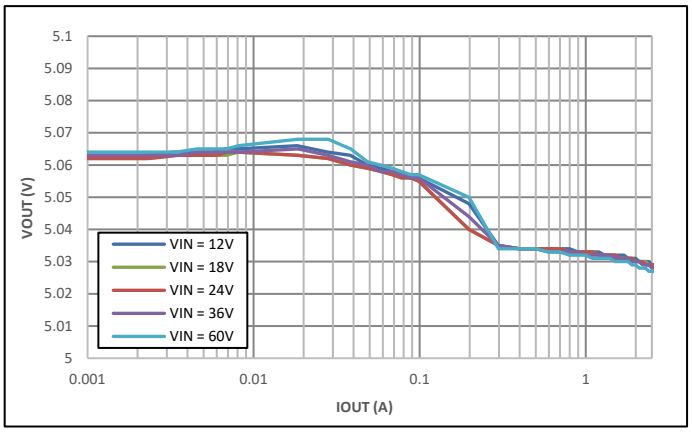
7.6.2 Typical Characteristics

Unless otherwise stated, the test conditions are applied: V_{IN} = 24V, V_{OUT} = 5V, F_S = 400kHz, L = 15µH, C_{OUT} = 47uF, T_A = 25˚C.



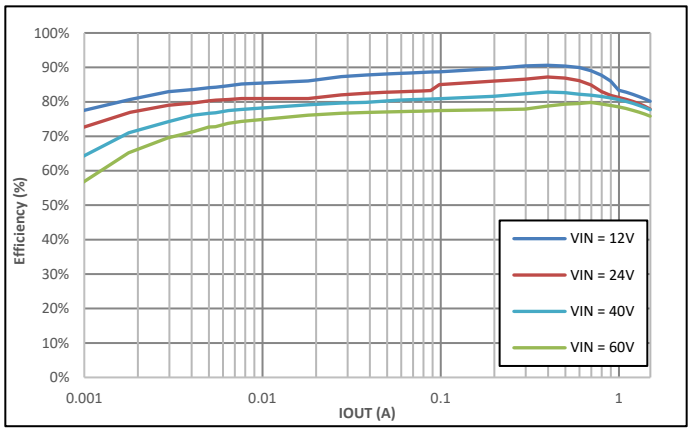
LN10161Q1-12, PFM, F_S = 400kHz, V_{OUT} = 5V

Figure 5. Efficiency Curves



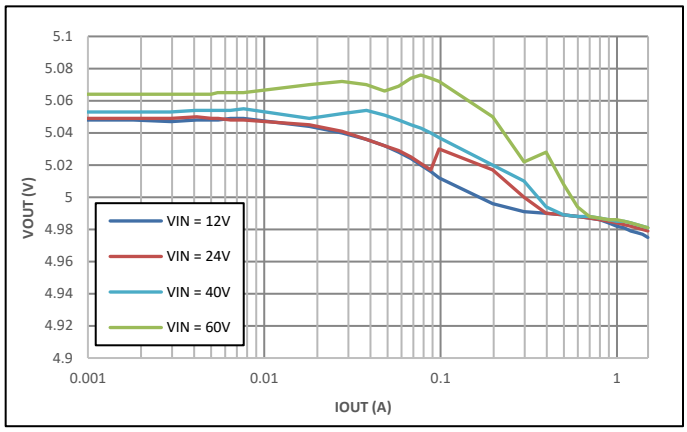
LN10161Q1-12, PFM, F_S = 400kHz, V_{OUT} = 5V

Figure 6. Load Regulation



LN10161Q1-16, PFM, F_S = 2.1MHz, V_{OUT} = 5V

Figure 7. Efficiency Curves

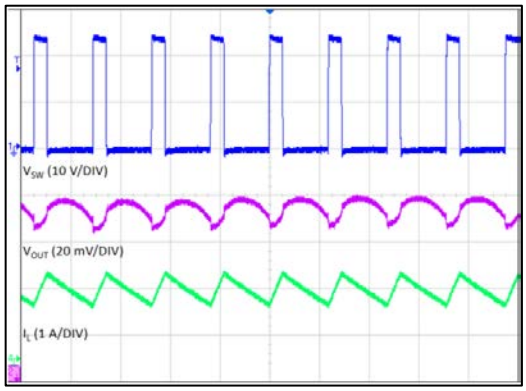


LN10161Q1-16, PFM, F_S = 2.1MHz, V_{OUT} = 5V

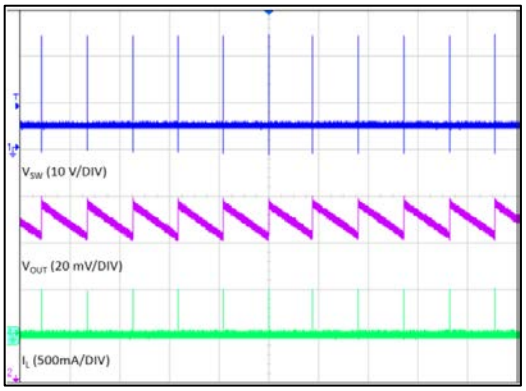
Figure 8. Load Regulation

7.6.3 Typical Waveforms

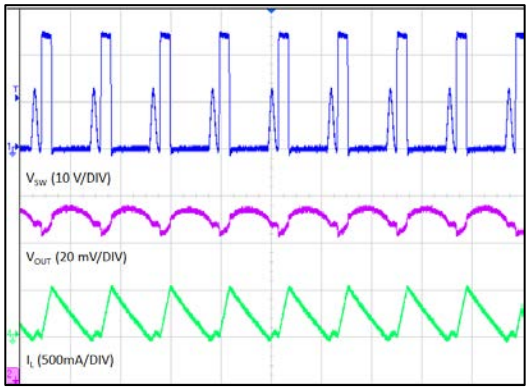
Unless otherwise stated, the test conditions are applied: V_{IN} = 24V, V_{OUT} = 5V, F_S = 400kHz, L = 15µH, C_{OUT} = 47uF, T_A = 25˚C.



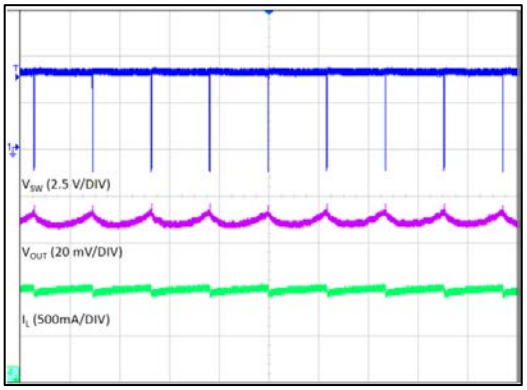
Time (2 µs/DIV)
LN10161Q1-12, F_S = 400kHz, V_{IN} = 24V, I_{OUT} = 1.5A
Figure 9. Switching Waveform in CCM Operation



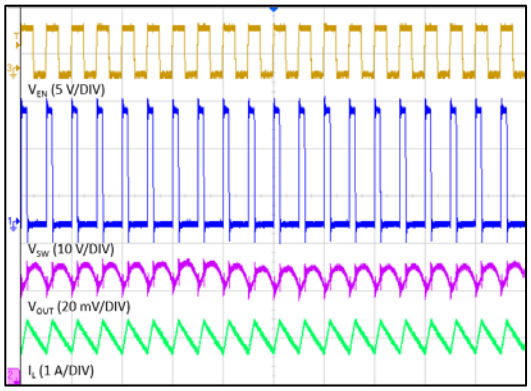
Time (20 ms/DIV)
LN10161Q1-12, V_{IN} = 24V, I_{OUT} = 0A
Figure 10. Switching Waveform in PFM Operation



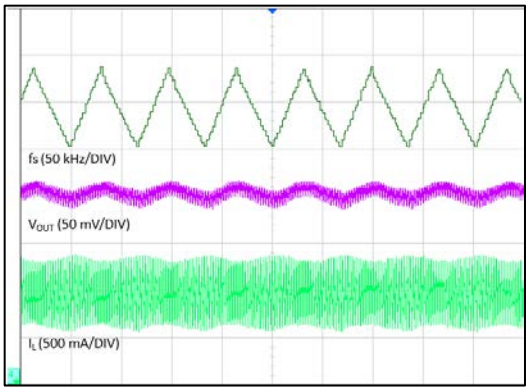
Time (2 µs/DIV)
LN10161Q1-12, V_{IN} = 24V, I_{OUT} = 200mA
Figure 11. Switching Waveform in DCM Operation



Time (20 µs/DIV)
LN10161Q1-12, V_{IN} = 5V, I_{OUT} = 1.5A
Figure 12. Switching Waveform in Dropout Operation



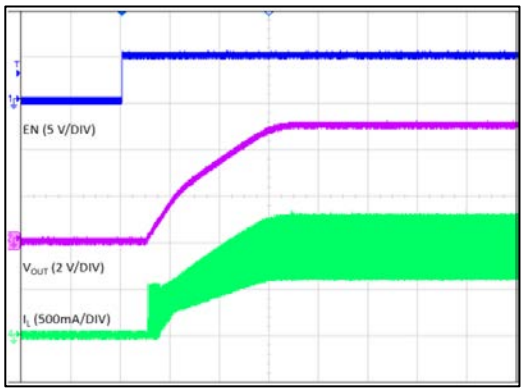
Time (5 µs/DIV)
LN10161Q1-12, F_S = 400kHz, V_{IN} = 24V, I_{OUT} = 1.5A
Figure 15. Sync to External Clock



Time (50 µs/DIV)
LN10161Q1S12, F_S = 400kHz, I_{OUT} = 1.5A
Figure 16. Spread Spectrum

Typical Waveforms (Continued)

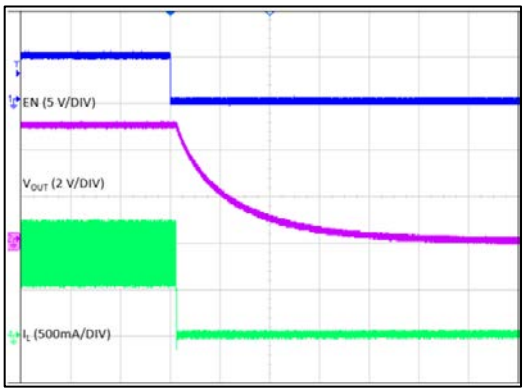
Unless otherwise stated, the test conditions are applied: V_{IN} = 24V, V_{OUT} = 5V, F_S = 400kHz, L = 15µH, C_{OUT} = 47uF, T_A = 25˚C.



Time (2 ms/DIV)

LN10161Q1-12, F_S = 400kHz, V_{IN} = 24V, I_{OUT} = 1A

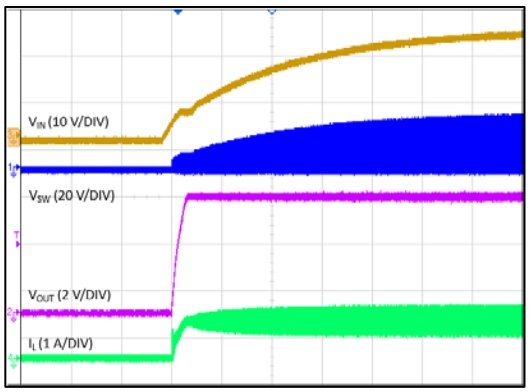
Figure 15. Startup through EN



Time (200 µs/DIV)

LN10161Q1-12, F_S = 400kHz, V_{IN} = 24V, I_{OUT} = 1A

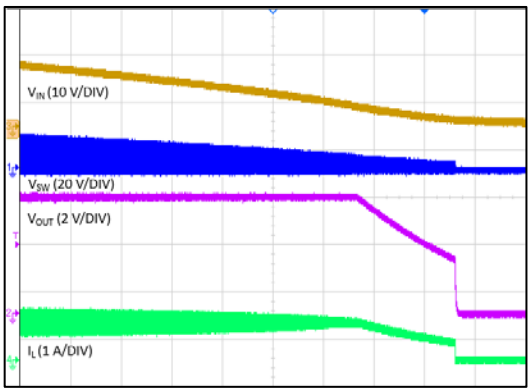
Figure 16. Shutdown through EN



Time (20 ms/DIV)

LN10161Q1-12, F_S = 400kHz, V_{IN} = 24V

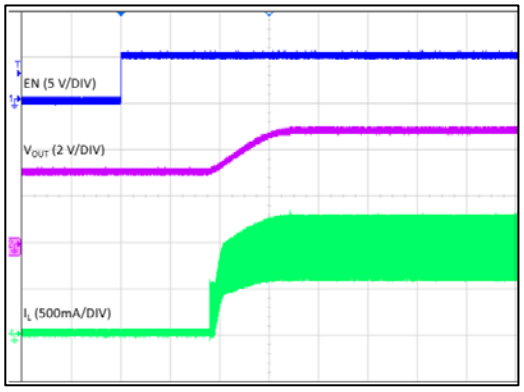
Figure 17. Startup through V_{IN}



Time (20 ms/DIV)

LN10161Q1-12, F_S = 400kHz, V_{IN} = 24V

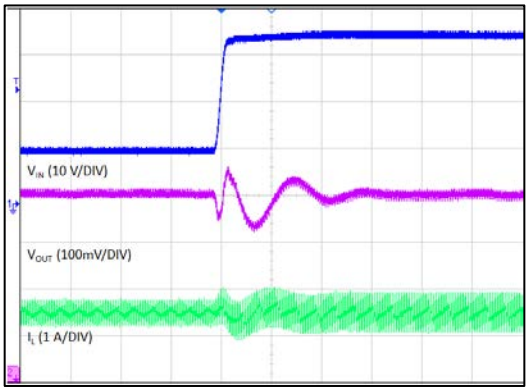
Figure 18. Shutdown through V_{IN}



Time (2 ms/DIV)

LN10161Q1-12, F_S = 400kHz, V_{IN} = 24V, I_{OUT} = 1A

Figure 19. Startup with Pre-Charged Voltage



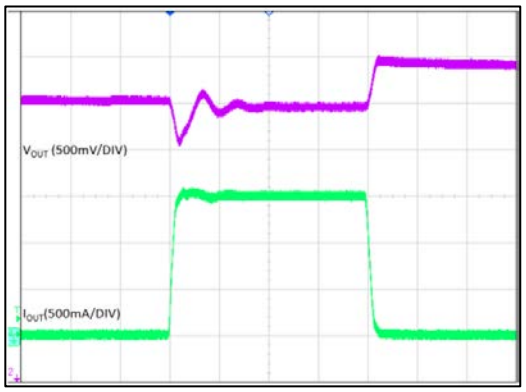
Time (50 µs/DIV)

LN10161Q1-12, F_S = 400kHz, I_{OUT} = 1.5A

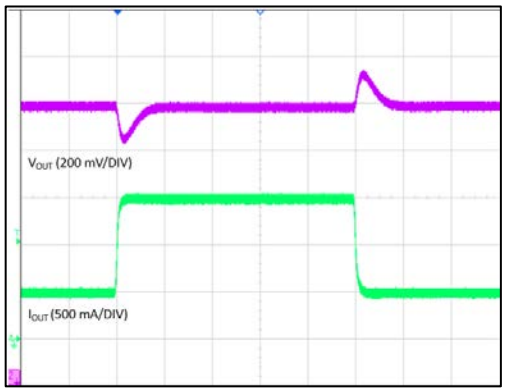
Figure 20. VIN Transient 12V <-> 36V, Slew Rate = 3V/µs

Typical Waveforms（Continued）

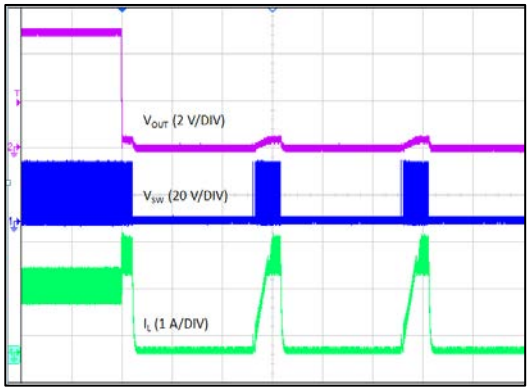
Unless otherwise stated, the test conditions are applied: V_{IN} = 24V, V_{OUT} = 5V, F_S = 400kHz, L = 15µH, C_{OUT} = 47uF, T_A = 25˚C.



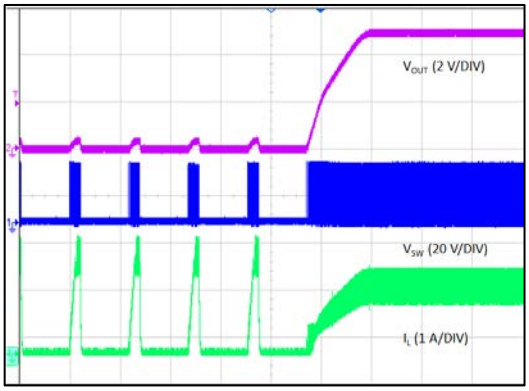
Time (100 µs/DIV)
LN10161Q1-12, F_S = 400kHz, V_{IN} = 24V
Figure 21. Load Transient 0A <-> 1.5A, Slew Rate = 0.1A/µs



Time (100 µs/DIV)
LN10161Q1-12, F_S = 400kHz, V_{IN} = 24V
Figure 22. Load Transient 0.5A <-> 1.5A, Slew Rate = 0.1A/µs



Time (2 ms/DIV)
LN10161Q1-12, F_S = 400kHz, V_{IN} = 24V, I_{OUT} = 1.5A to SCP
Figure 23. Into Output Short and Hiccup



Time (5 ms/DIV)
LN10161Q1-12, F_S = 400kHz, V_{IN} = 24V, I_{OUT} = SCP to 1.5A
Figure 24. Out of Output Short and Recovery

8 FUNCTIONAL DESCRIPTION

8.1 Overview

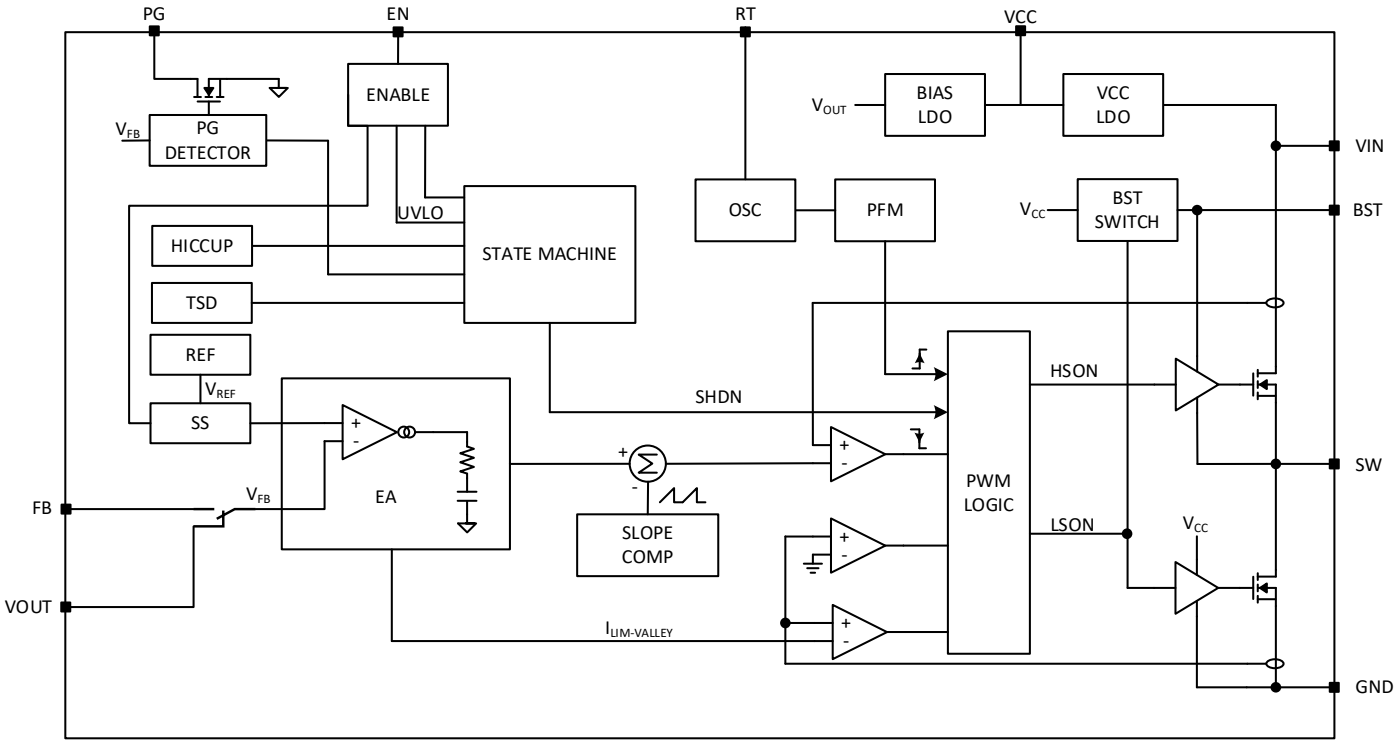
The LN10X61Q1 is a high efficiency, compact, synchronous step-down DC-DC converter employing a constant frequency, peak current mode control architecture with internal compensation. It operates from an input voltage from 3.5V to 60V and integrates both high-side and low-side power MOSFETs with up to 0.6A/1A/1.5A output current capabilities. The LN10X61Q1 with FB pin provides an adjustable output voltage from 1V to VIN. In addition, the LN10X61Q1 with VOUT pin provides a fixed output of 3.3V or 5V and enables higher accuracy and minimum peripheral components as well as lower quiescent current.

The LN10X61Q1 has three switching frequency options: 400kHz, 1MHz and 2.1MHz, and can be synchronized to an external clock ranging from 200kHz to 2.5MHz. The LN10X61Q1 with RT pin features an adjustable switching frequency through an external resistor connected between RT pin and GND pin. With a small minimum on-time, it enables a compact solution with small inductor and capacitor size and offers constant-frequency operation with high step-down ratio. Moreover, the LN10X61Q1 achieves the lowest possible dropout voltage with near 100% maximum duty cycle operation. During light load operation, LN10X61Q1 operates at DCM and PFM to maximize efficiency.

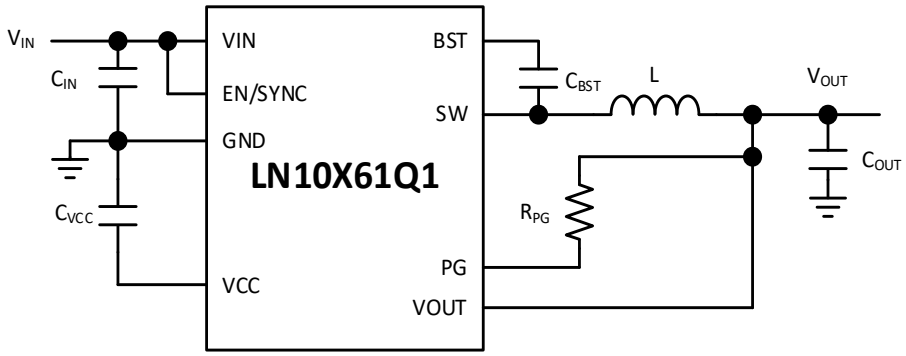
The LN10X61Q1 also features programmable output voltage, internal soft start, and a wide array of protection functions such as cycle-by-cycle peak current limit, output short- circuit protection with hiccup mode, over temperature shutdown and recovery, and adjustable system UVLO.

The LN10X61Q1 offers a spread spectrum feature to optimize EMI performance. Emissions at the operating frequency and its sub-harmonics are mitigated by spreading the single-point operating frequency over an extended range.

8.2 Funtional Diagram



8.3 Application Diagram with Full Features



8.4 Funtional Description

8.4.1 Voltage Regulation Loop and FB/VOUT pin

The LN10X61Q1 employs a peak current mode Control to regulate the output voltage. For highly efficient operation cross the whole load range, the LN10X61Q1 utilizes Discontinuous Conduction Mode (DCM) and Pulse Frequency Modulation (PFM) at light load.

To adjust the output voltage, connect a voltage divider between V_{OUT} and GND, and connect the center of the divider to FB pin. The steady state V_{FB} is typically 1V. The output voltage can be derived from:

$$V_{OUT} = (1 + \frac{R_{FBT}}{R_{FBB}}) \times V_{FB}$$

Based on the output voltage requirements, the above equation can be re-written as:

$$R_{FBB} = \frac{V_{FB}}{V_{OUT} - V_{FB}} \times R_{FBT}$$

In general, R_{FBT} < 1MΩ is recommended. The tolerance of the divider resistance should be less than 1%, and the temperature coefficients should be less than 100ppm.

The LN10X61Q1 uses an internal compensation scheme to stabilize the control loop, an external RC lead compensation network can be connected between VOUT and FB to improve transient response. An external lead compensation can be achieved by adding a capacitor in parallel with the upper leg resistor of the voltage divider between V_{OUT} and FB pin.

The zero frequency of the external lead compensator is at:

$$f_z = \frac{1}{2\pi \times R_{FBT} \times C_{LEAD}}$$

While the pole frequency of the external lead compensator is at:

$$f_p = \frac{1}{2\pi \times (R_{FBT} // R_{FBB}) \times C_{LEAD}}$$

The added external lead compensator can potentially increase the loop gain by $(1 + \frac{R_{FBT}}{R_{FBB}})$.

For the fixed VOUT products, there is no external divider, connect VOUT pin to system output directly. The VOUT pin is also used as the second input of internal LDO, decouple this pin to GND with ceramic capacitors.

8.4.2 Internal LDO and V_{CC} Pin

V_{CC} powers the internal control circuits and the gate drivers for the internal power MOSFETs. V_{CC} must be decoupled to GND with a 1μF to 4.7μF ceramic capacitor.

8.4.3 V_{IN} UVLO and EN/SYNC Pin

EN pin turns on and off the switching regulator and internal V_{CC} LDO. When the voltage on EN pin is below $EN_{VCC-OFF}$, it shuts down V_{CC} LDO and the chip goes into shutdown mode. When the voltage on EN pin is above EN_{VCC-ON}, it turns on V_{CC} LDO.

When EN rises above a precise threshold, $EN_{VOUT-ON}$, it turns on the switching regulator. In order to achieve an accurate system V_{IN} UVLO function, an enable divider can be added between VIN and GND. The switching regulator can thus be turned on at the programmable precise input voltage level, which is determined by:

$$V_{IN-RISING} = (1 + \frac{R_{ENT}}{R_{ENB}}) \times EN_{VOUT-ON}$$

8.4.4 Synchronization to External Clock and EN/SYNC Pin

LN10X61Q1 is capable of being synchronized to an external clock between 200kHz to 2.5MHz. Connect the external clock signal to EN/SYNC pin.

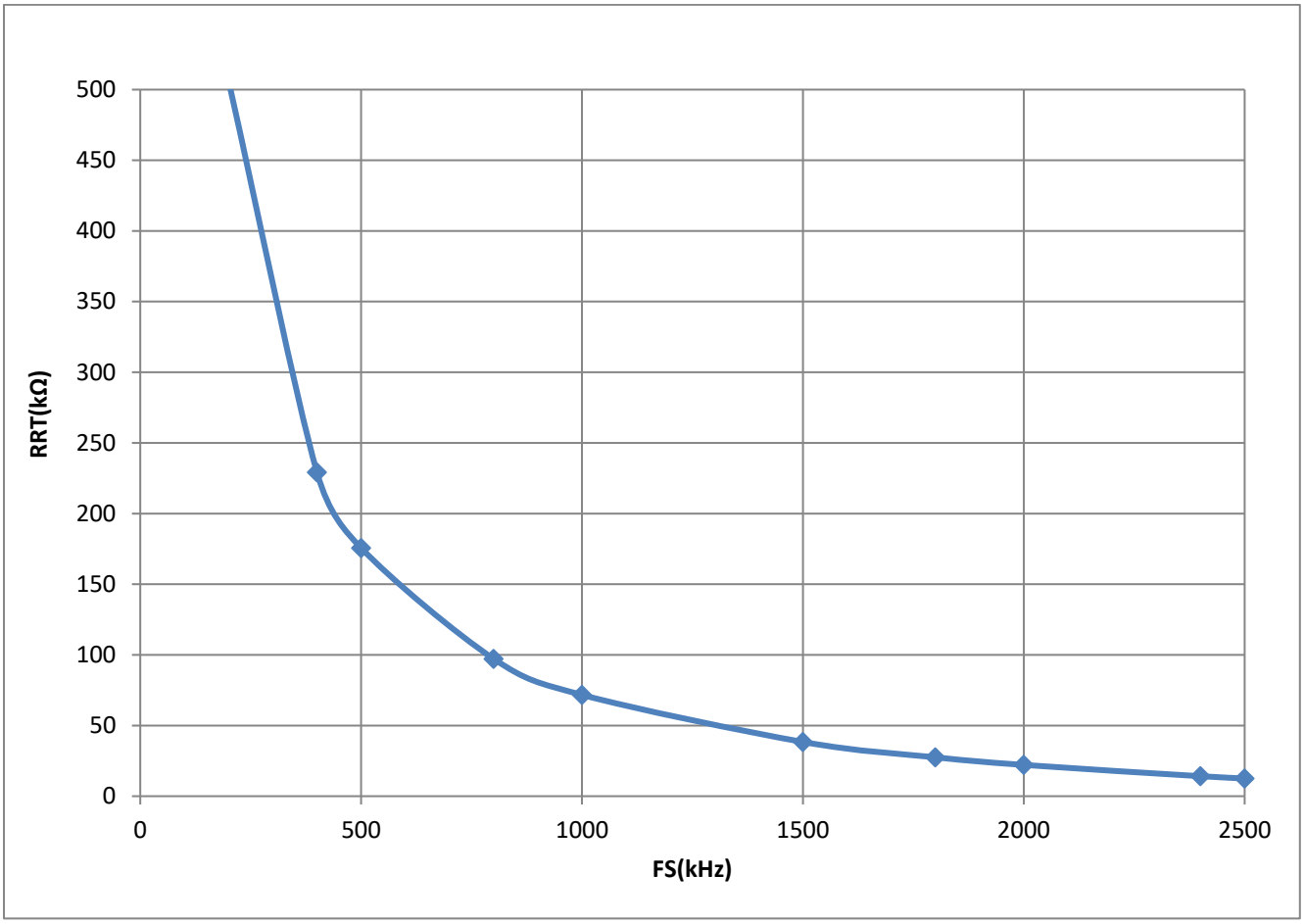
8.4.5 Switching Frequency and RT Pin

The LN10X61Q1 has three fixed frequency options: 400kHz, 1MHz and 2.1MHz. Meanwhile, the switching frequency of the LN10X61Q1 with RT pin can be programmable between 200kHz to 2.5MHz by an external resistor connected between RT pin and GND pin.

R_{RT} is calculated from:

$$R_{RT}(k\Omega) = \frac{152504}{F_S(kHz)^{1.069}} - 23$$

R_{RT} vs. Switching frequency is plotted as:



The following table lists some typical switching frequency and corresponding R_{RT}.

R_{RT} (kΩ)	F_S (kHz)
12.4	2500
22.1	2000
38.3	1500
71.5	1000
178	500
232	400
499	200

8.4.6 Power Good and PG Pin

The PG pin is connected to the open drain of an internal N-MOSFET. Externally, the PG pin needs to be pulled up to a voltage source by a resistor. PG goes high when V_{EN} is high and the feedback voltage V_{FB} is within the power good window defined by PG rising threshold and PG falling threshold. There is a power good rising delay $T_{PG-RISING}$ of 320µs in response to V_{FB} voltage going into the power good window and a power good falling delay $T_{PG-FALLING}$ of 320µs in response to V_{FB} voltage going outside of the window. PG pin immediately goes low when V_{EN} goes low.

8.4.7 Over-Current Protection

8.4.7.1 Peak Current Protection

Peak current protection is a cycle-by-cycle protection inherited from the peak current mode control. The peak current is clamped to the peak current limit threshold.

8.4.7.2 Valley Current Protection

During the low side conduction, the low side power MOSFET current is sensed and compared to the valley current threshold. When the low side current is higher than the valley current threshold, the high side power MOSFET is not allowed to turn on for the next cycle.

8.4.7.3 Hiccup Mode

When low side current is higher than the valley current threshold for 32 cycles, it shuts down the switching regulator. The switching regulator automatically turns back on after 5ms if EN is high. During the shutdown period, the soft start ramp capacitor is discharged by an internal FET; when the switching regulator turns back on, the regulator goes through the soft start process.

8.4.8 Thermal Shutdown and Auto-Recovery

When the junction temperature exceeds 170˚C, LN10X61Q1 shuts down the switching regulator to reduce thermal dissipation. It automatically restarts the switching regulator after the junction temperature drops back below 160 ˚C. The V_{CC} LDO regulator remains operational during over-temperature event.

8.4.9 Bootstrap Voltage, BST, and SW Pins

The internal gate driver for the high side Power MOSFET uses a bootstrapped supply from an external capacitor C_{BST}. C_{BST} connects between BST pin and SW. The voltage on C_{BST} is charged from V_{CC} through an internal switch when the low side power MOSFET conducts.

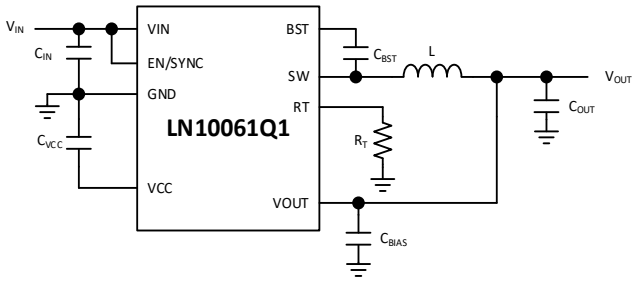
8.4.10 Low Drop-Out Operation

When input voltage is close to the output target voltage, LN10X61Q1 enters Low Drop-Out mode. The high-side MOSFET can be turned on for more than a switching period to maintain the output voltage regulation. When the input voltage is lower than the target voltage, the high-side power MOSFET is turned on for maximum allowable on time: t_{ON-MAX}. The low-side power MOSFET turns on briefly for $T_{OFF-MIN}$ to refresh the charge on C_{BST}.

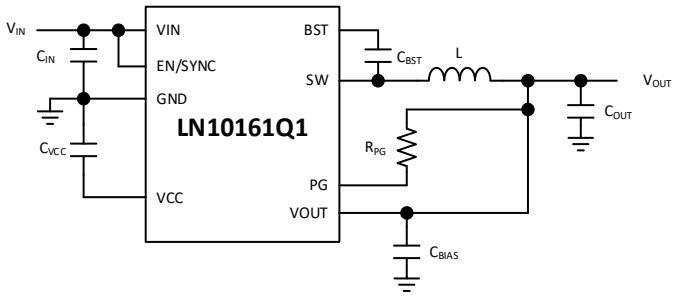
9 APPLICATION INFORMATON

9.1 Typical Applications

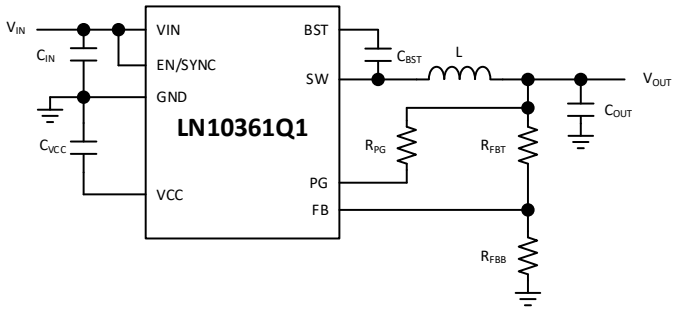
9.1.1 Fixed output 3.3V or 5V with adjustable switching frequency



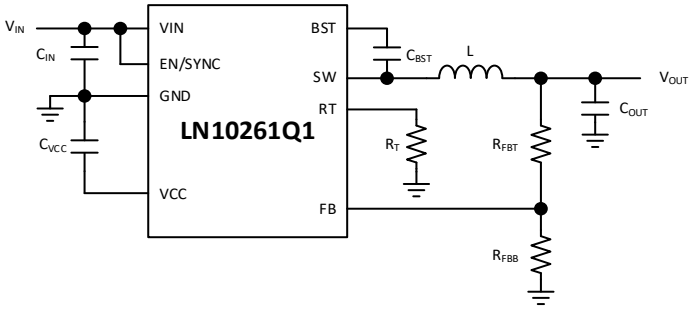
9.1.2 Fixed output 3.3V or 5V with PG pin



9.1.3 Adjustable output with PG pin



9.1.4 Adjustable output and adjustable switching frequency



10 LAYOUT

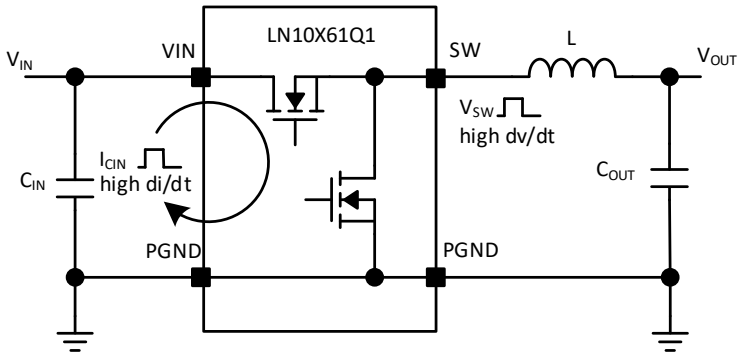
The performance of any switching converter depends as much upon the layout of the PCB as the component selection. The LN10X61Q1 is designed to meet the optimization requirements of PCB layout in the pin assignment. For example, VIN and GND pins are adjacent to each other, which is convenient for placing VIN bypass capacitors.

10.1 Layout Guidelines

Radiated EMI is generated by the high di/dt components in pulsing currents in switching converters. The larger area covered by the path of a pulsing current; the more electromagnetic emission is generated. As shown in the figure below, this part of the current flows from the VIN side of the input capacitors to high side switch, to the low side switch, and then returns to the ground of the input capacitors.

The key to minimize radiated EMI is to minimize the area of this pulsing current path, thus, placing high frequency ceramic bypass capacitor(s) as close as possible to the VIN and GND pins is necessary.

In addition, high dv/dt occurs on SW node during switching, so the trace between SW pin and inductor should be as short as possible, and just wide enough to carry the load current without excessive heating. Short and thick traces are highly recommended to minimize parasitic resistance. Besides, sensitive signal lines should be kept away from SW traces.



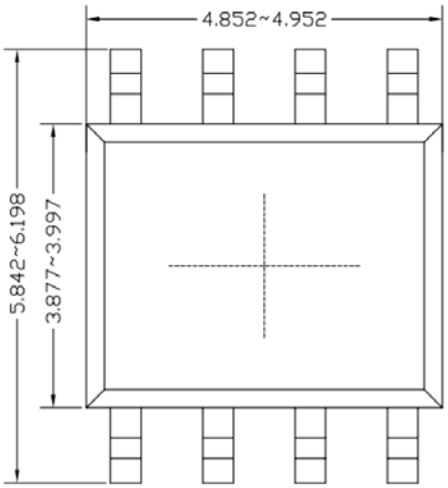
The following guidelines are provided to help users design a PCB with the best power conversion performance, thermal performance, and minimized generation of unwanted EMI.

1. Place high frequency ceramic bypass C_{IN} as close as possible to the LN10X61Q1 VIN and GND pins; a ceramic capacitor in small package (such as 0603) is still needed even if multiple input capacitors are implemented;
2. The high-current loop consisting of V_{IN}, V_{OUT} and GND should be as compact as possible;
3. The bypass capacitors of VOUT and VCC should be arranged close to the pin, and return to the GND pin with the shortest connection;
4. It is recommended to use a four-layer board with 2oz top and bottom layers, and a dedicate ground plane on middle layer. Use a minimum 3 by 4 arrays of 10 mil thermal vias to connect the thermal pad of LN10X61Q1 to the system ground plane for heat sinking purpose;
5. The SW and BST nodes contains a lot of high-frequency noise, so the connection of the pins should be as short as possible, meanwhile, there should be sufficient width to conduct the current;

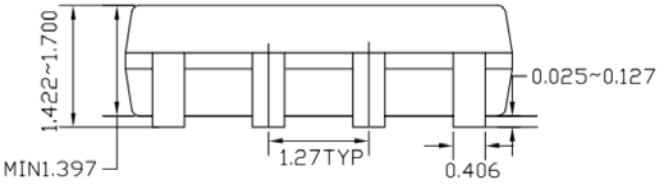
6. Sensitive analog signals, such as FB and RT, need to be far away from the noisy nodes, ground plane can be used as a shielding layer while routing these sensitive signals;
7. The feedback resistance of the FB connection must be located as close to the pin as possible, If V_{OUT} accuracy at the load is important, make sure V_{OUT} sense is made at the load;
8. For the peripheral components connected to FB, RT and EN pins, a single point ground connection to the plane is recommended.

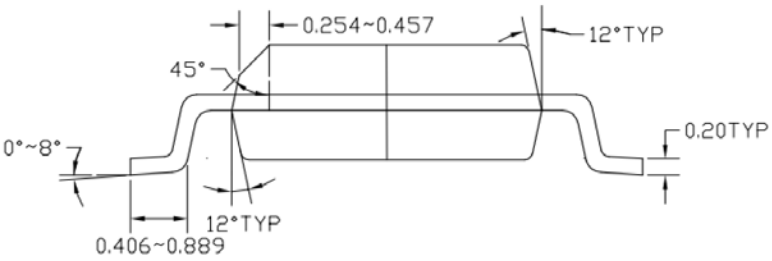
11 PACKAGE INFORMATION

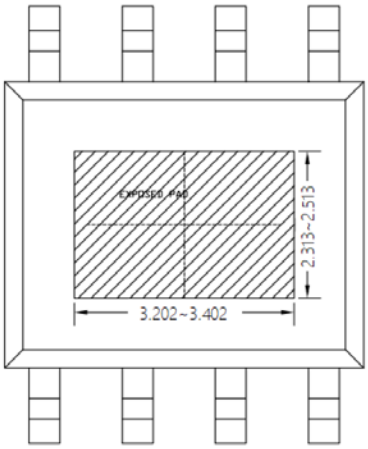
11.1 Package Outline



TOP VIEW







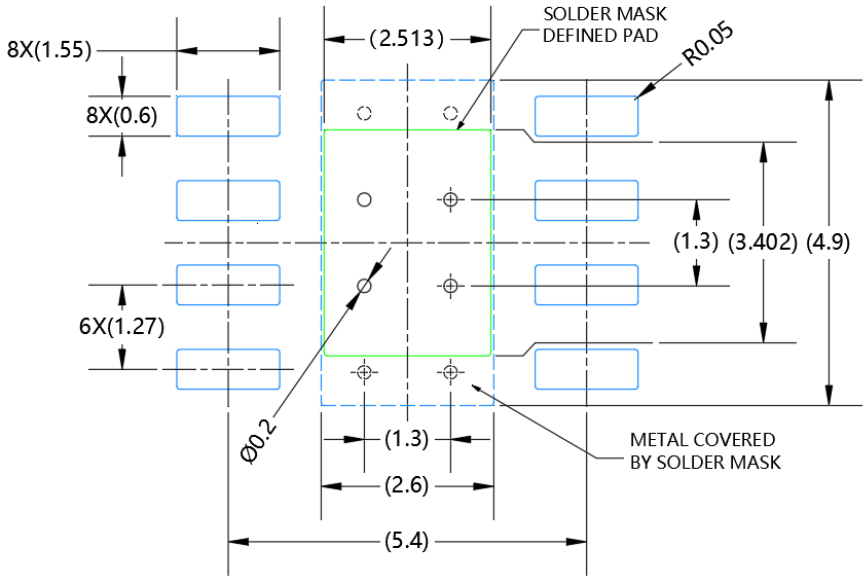
BOTTOM VIEW

Notes:

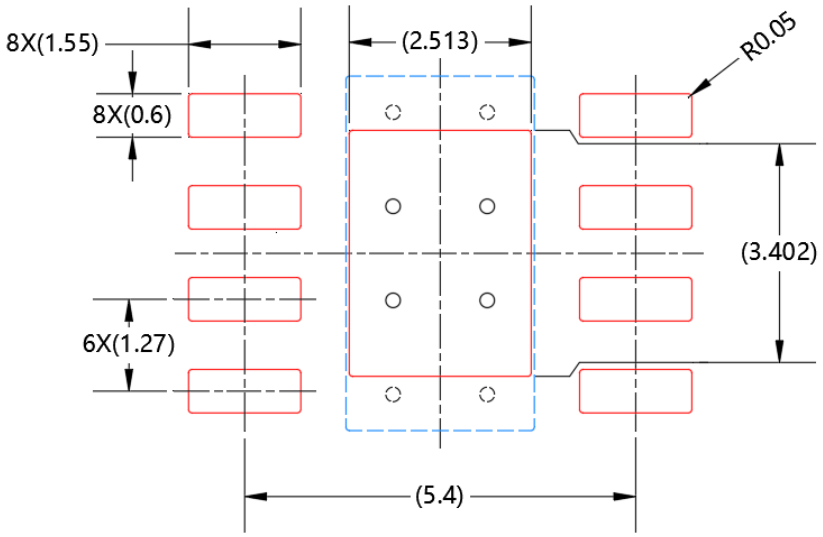
1. Both package length and width do not include mold flash.
2. Controlling dimension: mm
3. Reference JEDEC MS-013, MS-012
4. The size label of length and width in the drawing belong to the bottom size of the package.

11.2 Footprint Example

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL



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