

General Description

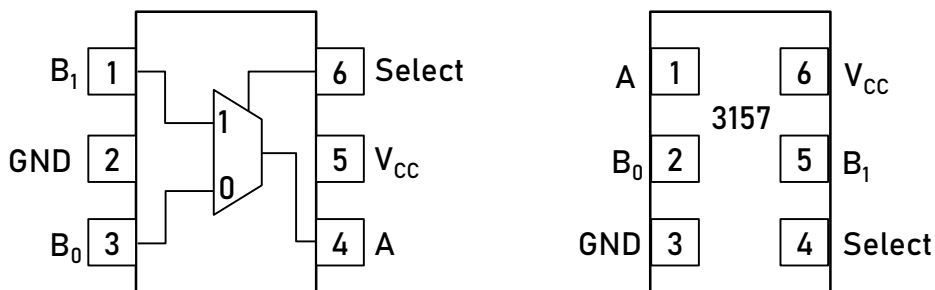
The LTC3157 is an advanced CMOS analog switch fabricated with silicon gate CMOS technology. It achieves very low propagation delay while maintaining CMOS low power dissipation. Analog and digital voltages that may vary across the full power-supply range (from V_{CC} to GND).

The Select pin has over voltage protection that allows voltages above V_{CC} , up to 7.0 V to be present on the pin without damage or disruption of operation of the part, regardless of the operating voltage.

Features

- Low power dissipation: 1uA
- High bandwidth: 350MHz
- Standard CMOS logic levels
- High speed with improved linearity
- Switches Standard NTSC/PAL Video, Audio, SPDIF and HDTV
- Suitable for Clock Switching, Data Mux'ing, etc.
- Low $R_{DS(ON)}$
- Break Before Make Circuitry, Prevents Inadvertent Shorts
- Operating temperature $-55^{\circ}\text{C} \sim +125^{\circ}\text{C}$
- Available packages: SC70-6, DFN-6

Pin Configuration



TOP VIEW

Order Information

Model	Package	Ordering Number	MARKING
LTC3157	SC70-6	LTC3157XC6	3157
	DFN-6	LTC3157XF6	3157

Pin Function

Pin	I/O	Pin Function
A, B ₀ , B ₁	I/O	Data port
Select	I	Controlling choice
V _{CC}	—	Power supply port
GND	—	Ground

Functions Description

Select input port	Pin Function
L	B ₀ Connected to A
H	B ₁ Connected to A

Absolute Maximum Ratings

Characteristic	Symbol	Value	Unit
Supply Voltage	V _{CC}	-0.5 ~ +7.0	V
DC Switch Voltage (Note 1)	V _S	-0.5 ~ V _{CC} +0.5	V
DC Input Voltage (Note 1)	V _{IN}	-0.5 ~ +7.0	V
DC Input Diode Current @V _{IN} <0V	I _{IK}	-50	mA
DC Output Current	I _{out}	128	mA
DC V _{CC} or Ground Current	I _{CC} / I _{GND}	100	mA
Storage Temperature Range	T _{stg}	-65 ~ +150	°C
Junction Temperature Under Bias	T _J	150	°C
Junction Lead Temperature (Soldering, 10 Seconds)	T _L	260	°C
Power Dissipation @ +85°C	P _D	180	mW

Maximum ratings are DC values beyond which the device may be damaged or have its useful life impaired. The data sheet specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Don't recommend operation outside data sheet specifications.

1. The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed

Absolute Maximum Ratings

Characteristic	Symbol	Min	Max	Unit
Supply Voltage Operating	V _{CC}	1.65	5.5	V
Select Input Voltage	V _{IN}	0	V _{CC}	V
Switch Input Voltage	V _{IN}	0	V _{CC}	V
Output Voltage	V _{OUT}	0	V _{CC}	V
Operating Temperature	T _A	-55	+125	°C
Input Rise and Fall Time	t _r , t _f			ns/V
Control Input V _{CC} = 2.3 V–3.6 V		0	10	
Control Input V _{CC} = 4.5 V–5.5 V		0	5.0	

2. Select input must be held HIGH or LOW, it must not float.

Block Diagram

Symbol	Parameter	Test Conditions	V_{CC}	$T_A = 25\text{ }^\circ\text{C}$			$T_A = -40\text{ }^\circ\text{C} \sim +85\text{ }^\circ\text{C}$		Unit
				Min	Typ	Max	Min	Max	
<i>DC ELECTRICAL CHARACTERISTICS</i>									
V_{IH}	HIGH Level Input Voltage		1.65-1.95				$0.75V_{CC}$		V
			2.3-2.8				1.5		
			3-4.2				2.4		
			4.5-5.5				$0.6 V_{CC}$		
V_{IL}	LOW Level Input Voltage		1.65-1.95				$0.25V_{CC}$		V
			2.3-2.8				0.4		
			3-5.5				$0.3 V_{CC}$		
I_{IN}	Input Leakage Current	$0 < V_{IN} < 5.5V$	0-5.5		± 0.05	± 0.1		± 1	μA
I_{OFF}	OFF State Leakage Current	$0 < A, B < V_{CC}$	1.65-5.5		± 0.05	± 0.1		± 1	μA
I_{CC}	Quiescent Supply	$V_{IN} = V_{CC}$ or GND $I_{OUT} = 0$	5.5			1.0		10	μA
	Analog Signal Range		V_{CC}	0		V_{CC}	0	V_{CC}	V
R_{ON}	Switch On Resistance (Note 3)	$V_{IN} = 0V$, $I_O = 30mA$				3.0		7.0	Ω
		$V_{IN} = 2.4V$, $I_O = -30mA$	4.5			5.0		12	Ω
		$V_{IN} = 4.5V$, $I_O = -30mA$				7.0		15	Ω
		$V_{IN} = 0V$, $I_O = 24mA$	3.0			4.0		9.0	Ω
		$V_{IN} = 3V$, $I_O = -24mA$				10		20	Ω
		$V_{IN} = 0V$, $I_O = 8mA$				5.0		12	Ω
		$V_{IN} = 2.3V$, $I_O = -8mA$	2.3			13		30	Ω
		$V_{IN} = 0V$, $I_O = 4mA$				6.5		20	Ω
		$V_{IN} = 1.65V$, $I_O = -4mA$	1.65			17		50	Ω
R_{RANGE}	On Resistance Over Signal Range (Note)	$I_A = -30mA$ $0 \leq V_{Bn} \leq V_{CC}$	4.5					25	Ω
		$I_A = -24mA$	3					50	Ω

CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.

Linearin and designs are registered trademarks of Linearin Technology Corporation.

© Copyright Linearin Technology Corporation. All Rights Reserved.

All other trademarks mentioned are the property of their respective owners. Downloaded From [Onyiac.com](http://www.onyiac.com)

		$0 \leq V_{Bn} \leq V_{CC}$			
3) (Note 7)		$I_A = -8mA$	2.3	100	Ω
		$0 \leq V_{Bn} \leq V_{CC}$			
ΔRON	On Resistance Match Between Channels (Note 3) (Note 4) (Note 5)	$I_A = -4mA$	1.65	300	Ω
		$0 \leq V_{Bn} \leq V_{CC}$			
		$I_A = -30mA$ $V_{Bn} = 3.15$	4.5	0.15	Ω
		$I_A = -24mA$ $V_{Bn} = 2.1$	3	0.2	Ω
R_{FLAT}	On Resistance Flatness (Note 3) (Note 4) (Note 6)	$I_A = -8mA$ $V_{Bn} = 1.6$	2.3	0.5	Ω
		$I_A = -4mA$ $V_{Bn} = 1.15$	1.65	0.5	Ω
		$I_A = -30mA$ $0 \leq V_{Bn} \leq V_{CC}$	5	6.0	Ω
		$I_A = -24mA$ $0 \leq V_{Bn} \leq V_{CC}$	3.3	12	Ω
		$I_A = -8mA$ $0 \leq V_{Bn} \leq V_{CC}$	2.5	28	Ω
		$I_A = -4mA$ $0 \leq V_{Bn} \leq V_{CC}$	1.8	125	Ω

AC ELECTRICAL CHARACTERISTICS

t_{PHL} t_{PLH}	Propagation Delay Bus to Bus (Note 8)	Figure 1 $V_I = OPEN$	1.65-1.95				nS	
			2.3-2.7	1.2			nS	
			3.0-3.5	0.8			nS	
			4.5-5.5	0.3			nS	
t_{PZL} t_{PZH}	Output Enable Time, Turn On Time (A to Bn)	Figure 1 $V_I = 2 * V_{CC}$ for t_{PZL} $V_I = 0V$ for t_{PZH}	1.65-1.95	23	7.0	24	nS	
			2.3-2.7	13	3.5	14	nS	
			3.0-3.5	6.9	2.5	7.6	nS	
			4.5-5.5	5.2	1.7	5.7	nS	
t_{PLZ} t_{PHZ}	Output Disable Time, Turn Off Time (A Port to B Port)	Figure 1 $V_I = 2 * V_{CC}$ for t_{PLZ} $V_I = 0V$ for t_{PHZ}	1.65-1.95	12.5	3.0	13	nS	
			2.3-2.7	7.0	2.0	7.5	nS	
			3.0-3.5	5.0	1.5	5.3	nS	
			4.5-5.5	3.5	0.8	3.8	nS	
t_{B-M}	Break Before Make Time (Note 7)	Figure 2 $C_L = 50pF$ $R_L = 600\Omega$	1.65-1.95				0.5	nS
			2.3-2.7				0.5	nS
			3.0-3.5				0.5	nS
			4.5-5.5				0.5	nS

CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
Linearin and designs are registered trademarks of Linearin Technology Corporation.
© Copyright Linearin Technology Corporation. All Rights Reserved.
All other trademarks mentioned are the property of their respective owners. Downloaded From [Onyiac.com](http://www.onyiac.com)



Q	Charge Injection (Note 7)	Figure 3, $C_L=0.1nF$, $V_{GEN}=0V$, $R_{GEN}=0\Omega$	5.0	7.0	pC
			3.3	3.0	pC
OIRR	Off Isolation (Note 9)	Figure 4, $R_L=50\Omega$ $f=10MHz$	1.65-5.5	-57	dB
Xtalk	Crosstalk	Figure 5 $R_L=50\Omega$ $f=10MHz$	1.65-5.5	-54	dB
BW	-3 dB Bandwidth	Figure 8, $R_L=50\Omega$	1.65-5.5	350M	Hz
THD	Total Harmonic Distortion (Note 7)	$R_L=600\Omega,0.5V_{p-p}$ $f=600Hz-20k Hz$	5.0	0.011	%
C_{IN}	Select Pin Input Capacitance (Note 10)		0	2.3	pF
C_{IO-B}	B Port Off Capacitance (Note 10)	Figure 6	5.0	5.0	pF
C_{IOA-ON}	A Port Capacitance when Switch is Enabled (Note 10)	Figure 7	5.0	15.5	pF

3. Measured by the voltage drop between A and B pins at the indicated current through the switch. On Resistance is determined by the lower of the voltages on the two (A or B Ports).

4. Parameter is characterized but not tested in production.

5. $\Delta R_{ON} = R_{ON\ max} - R_{ON\ min}$ measured at identical V_{CC} , temperature and voltage levels.

6. Flatness is defined as the difference between the maximum and minimum value of On Resistance over the specified range of conditions.

7. Guaranteed by Design.

8. This parameter is guaranteed by design but not tested. The bus switch contributes no propagation delay other than the RC delay of the On Resistance of the switch and the 50 pF load capacitance, when driven by an ideal voltage source (zero output impedance).

9. Off Isolation = $20 \log_{10} [V_A/V_{Bn}]$.

10. $T_A = +25^\circ C$, $f = 1 MHz$, Capacitance is characterized but not tested in production.

NOTE: Input driven by 50Ω source terminated in 50Ω
 NOTE: C_L includes load and stray capacitance
 NOTE: Input PRR=1.0MHz; $t_w = 500$ ns

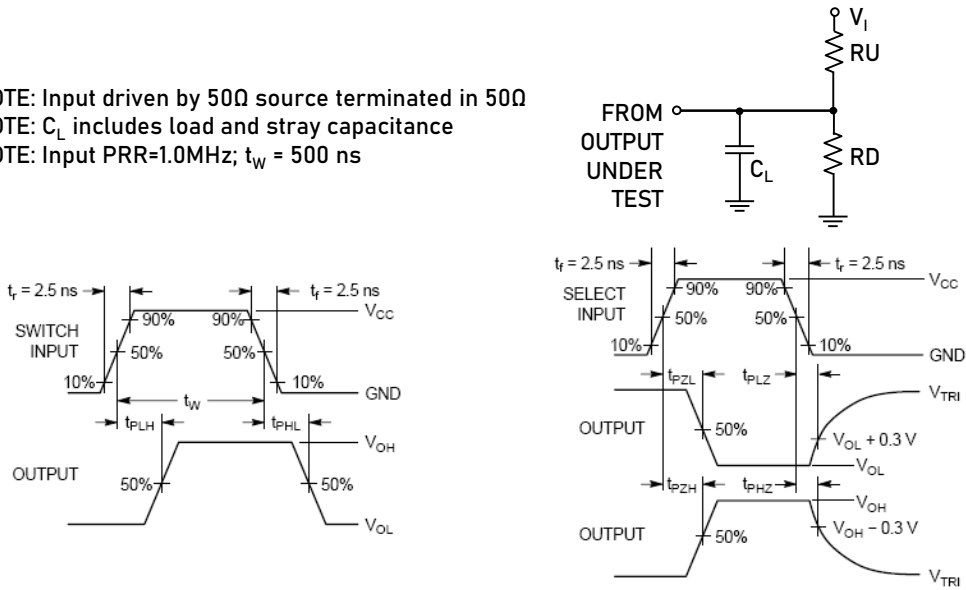


Figure 1. AC Test Circuit ,AC Waveforms

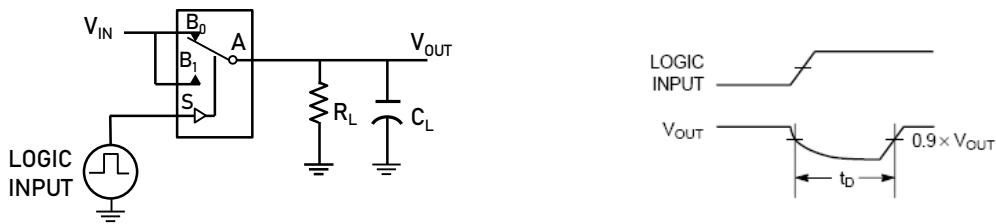


Figure 2. Break Before Make Interval Timing

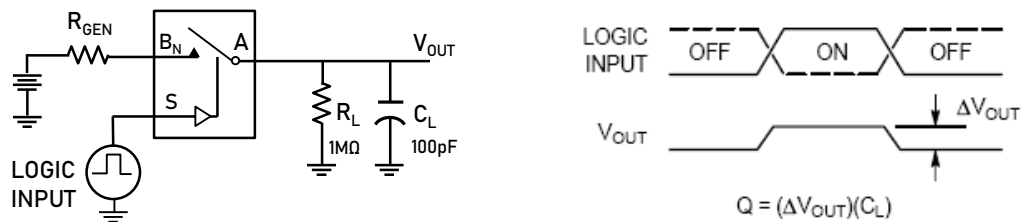


Figure 3. Charge Injection Test

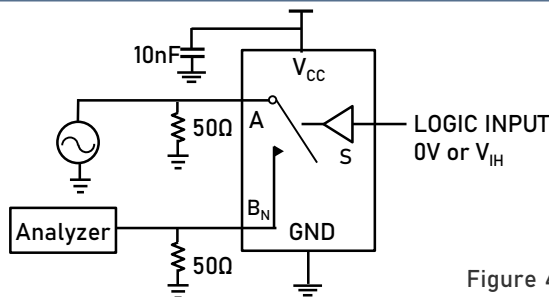


Figure 4. Off Isolation

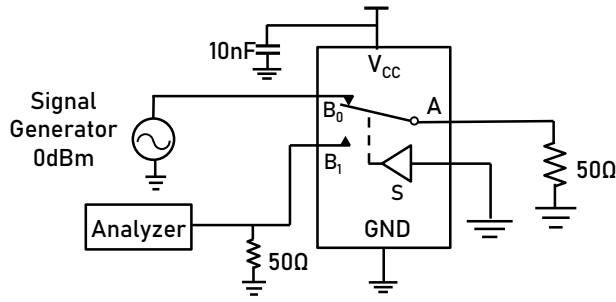


Figure 5. Crosstalk

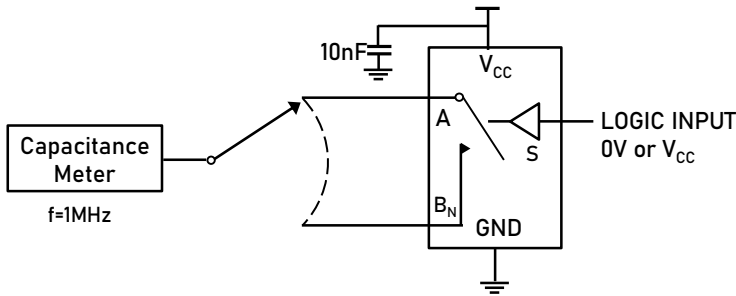


Figure 6. Channel Off Capacitance

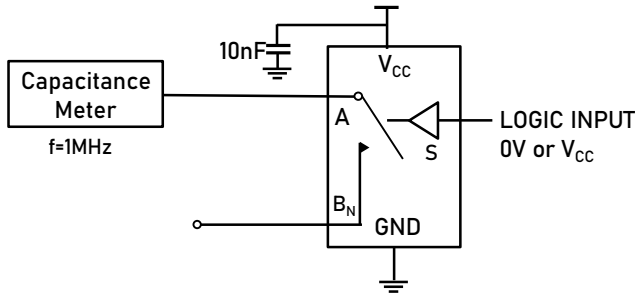


Figure 7. Channel On Capacitance

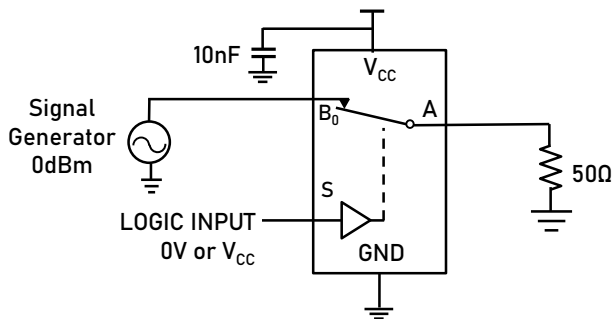
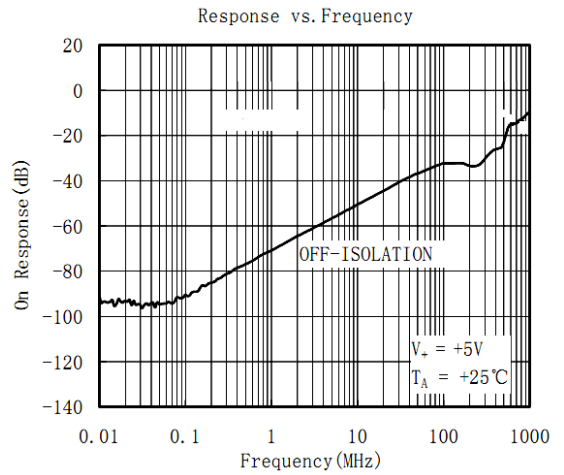
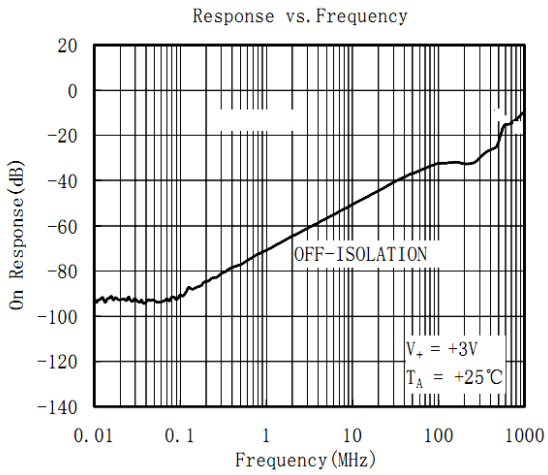
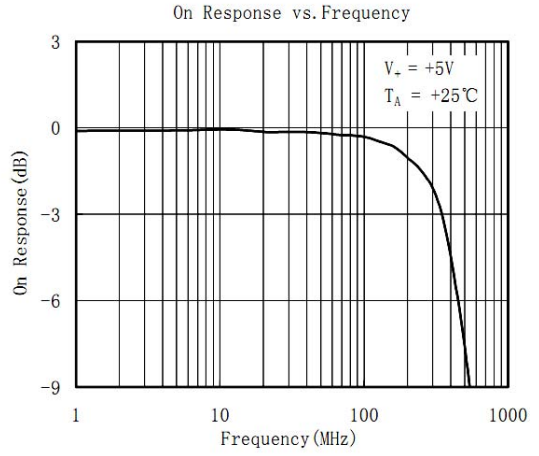
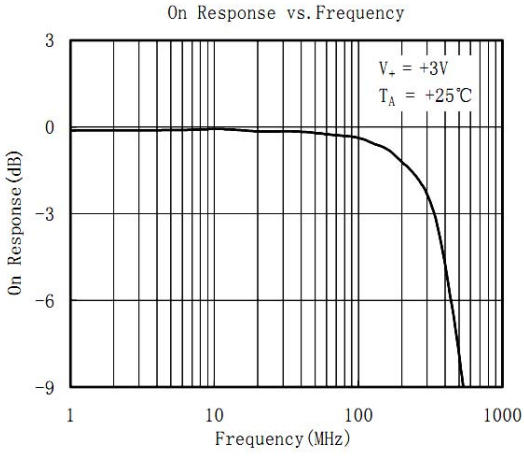
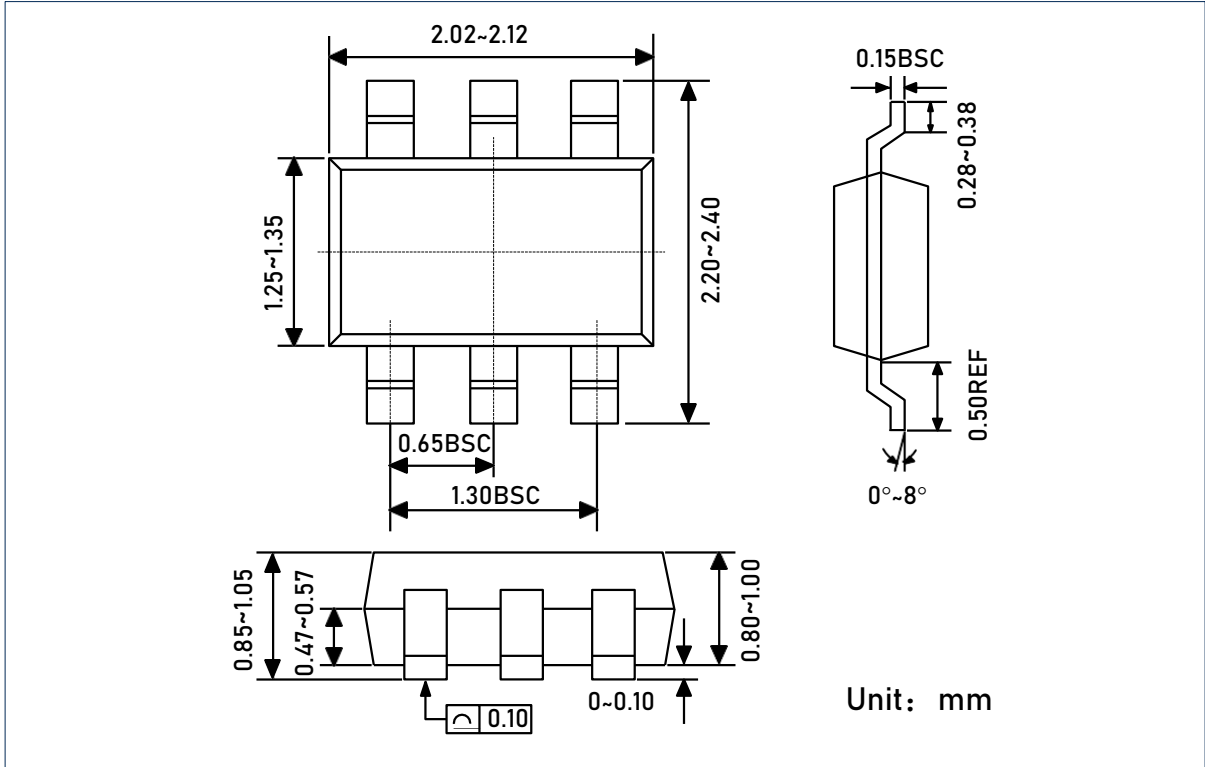


Figure 8. Bandwidth

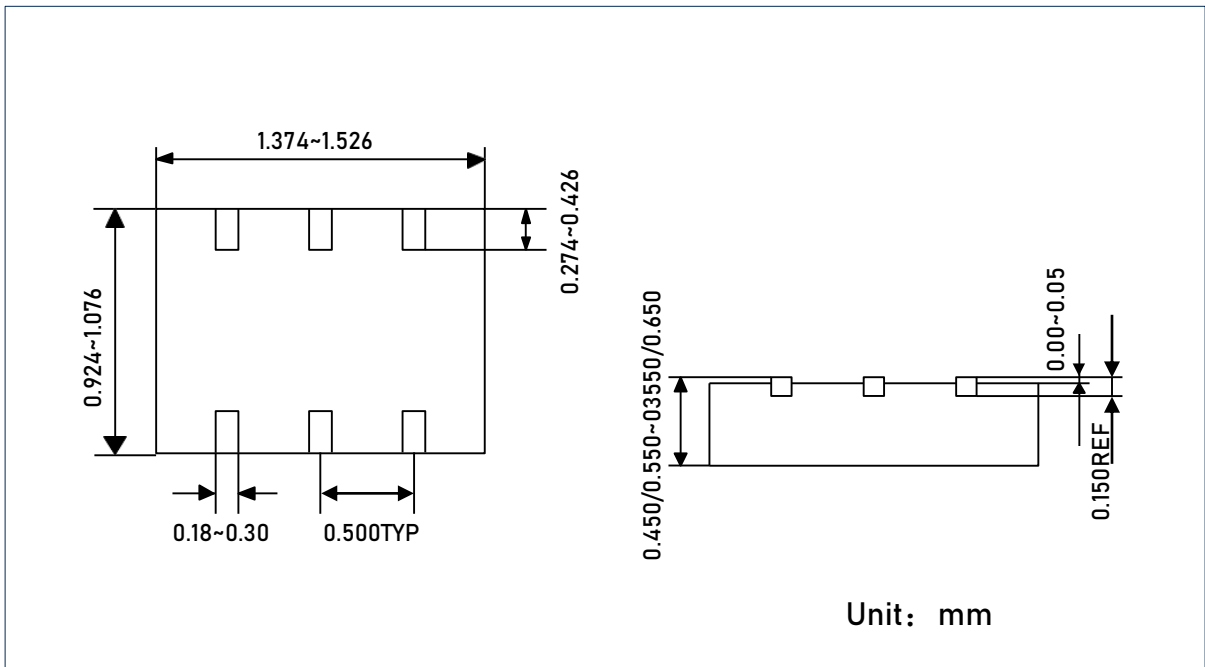


Package Dimension

SC70-6



DFN6



单击下面可查看定价，库存，交付和生命周期等信息

[>>Linearin\(先积\)](#)