

General Description

The LTC7227 is 2 to 1 port analog switches. Their wide bandwidth and low bit-to-bit skew allow them to pass high-speed differential signals with good signal integrity. Each switch is bidirectional and offers little or no attenuation of the high-speed signals at the outputs. Industry-leading advantages include a propagation delay of less than 250 ps, resulting from its low channel resistance and low I/O capacitance. Their high channel-to-channel crosstalk rejection results in minimal noise interference. Their bandwidth is wide enough to pass High-Speed USB 2.0 differential signals (480 Mbps).

Features

- RON is Typically 6Ω at VCC = 3.3 V
- Low Bit-to-Bit Skew: Typically 50 ps
- Low Crosstalk: -45 dB @ 250 MHz
- Low Current Consumption: 1.0 μA
- Near-Zero Propagation Delay: 250 ps
- Channel On-Capacitance: 3.5pF Typically
- VCC Operating Range: 1.65 V to 4.5 V
- >750 MHz Bandwidth (or Data Frequency)
- Available Packages: QFN1.8×1.4-10L and MSOP-10L

Applications

- Differential Signal Data Routing
- USB 2.0 Signal Routing

Order Information

MODEL	PACKAGE	ORDERING NUMBER
LTC7227	QFN1.8×1.4-10L	LTC7227YFS10
	MSOP-10L	LTC7227YV10

Pin Description

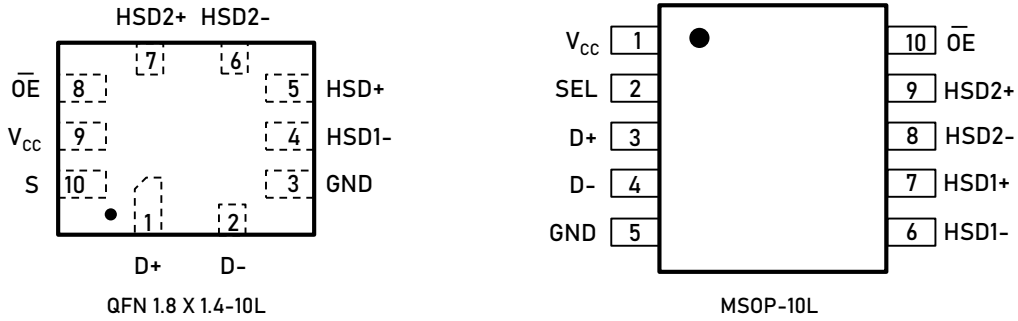


Figure1. Top View

Pin Function

Pin Name	Function
SEL	Select Input
\overline{OE}	Output Enable
HSD1+,HSD1-,HSD2+,HSD2-,D+,D-	Data Ports

Truth Table

\overline{OE}	SEL	HSD1+,HSD1-	HSD2+,HSD2-
1	X	OFF	OFF
0	0	ON	OFF
0	1	OFF	ON

Absolute Maximum Ratings

Symbol	Pin	Parameter	Value	Unit
V_{CC}	V_{CC}	Positive DC Supply Voltage	-0.5 to +6.0	V
V_{IS}	HSD1+,HSD1-,HSD2+,HSD2-	Analog Signal Voltage	-0.5 to V_{CC}	V
	D+,D-		-0.5 to +5.5	
V_{IN}	\overline{OE} ,SEL	Control Input Voltage	-0.5 to V_{CC}	V
I_{CC}	V_{CC}	Positive DC Supply Current	50	mA
T_S		Storage Temperature	-65 to +150	°C
I_{IS_CON}	HSD1+,HSD1-,HSD2+,HSD2-D+,D-	Analog Signal Continuous Current-Closed Switch	± 100	mA
I_{IS_PK}	HSD1+,HSD1-,HSD2+,HSD2-D+,D-	Analog Signal Continuous Current 10% Duty Cycle	± 150	mA
I_{IN}	\overline{OE}	Control Input Current	± 20	mA
	All pin	Human Body Model, JEDEC: JESD22-A114	>8	
ESD	Air Discharge	IEC 61000-4-2 System on	>15	kV
	Contact	USB Connector Pins D+, D-	>8	
	Charged Device Model, JEDEC: JESD22-C101		>2	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Symbol	Pins	Parameter	Min	Max	Unit
V_{CC}		Positive DC Supply Voltage	1.65	4.5	V
V_{IS}	HSD1+,HSD1-,HSD2+,HSD2-	Analog Signal Voltage	GND	V_{CC}	V
	D+,D-		GND	4.5	
V_{IN}	\overline{OE}	Digital Select Input Voltage	GND	V_{CC}	V
T_A		Operating Temperature Range	-40	+85	°C

Minimum and maximum values are guaranteed through test or design across the Recommended Operating Conditions, where applicable. Typical values are listed for guidance only and are based on the particular conditions listed for section, where applicable. These conditions are valid for all values found in the characteristics tables unless otherwise specified in the test conditions.

DC Electrical Characteristics

CONTROL INPUT (Typical: T = 25 °C, V_{CC} = 3.3 V)

Symbol	Pins	Parameter	Test Conditions	V _{CC} (V)	-40°C to +85°C			Unit
					Min	Typ	Max	
V _{IH}	$\overline{\text{OE}}$	Control Input High Voltage		2.7	1.3	-	-	V
				3.3	1.4			
				4.2	1.6			
V _V	$\overline{\text{OE}}$	Control Input Low Voltage		2.7	-		0.4	V
				3.3			0.4	
				4.2			0.5	
I _{IN}	$\overline{\text{OE}}$	Control Input Leakage Current	0 ≤ V _{IS} ≤ V _{CC}	1.65 – 4.5	-	-	±1.0	µA

SUPPLY AND LEAKAGE CURRENT (Typical: T = 25 °C, V_{CC} = 3.3 V)

Symbol	Pins	Parameter	Test Conditions	V _{CC} (V)	-40°C to +85°C		unit
					Min	Max	
I _{CC}	V _{CC}	Quiescent Supply Current	V _{IS} = V _{CC} or GND I _{OUT} = 0A	1.65 – 4.5	-	1.0	µA
I _{CCT}	V _{CC}	Increase in ICC per Control Voltage	V _{IN} = 2.6V	3.6	-	10	µA
I _{OZ}	HSD1+ HSD1- HSD2+ HSD2-	OFF Stage Leakage Current	0 ≤ V _{IS} ≤ V _{CC}	1.65 – 4.5	-	±1.0	µA
I _{OFF}	D+, D-	Power OFF Leakage Current	0 ≤ V _{IS} ≤ 4.5V	0	-	±1.0	µA

HIGH SPEED ON RESISTANCE (Typical: T = 25 °C, V_{CC} = 3.3 V)

Symbol	Pins	Parameter	Test Conditions	V _{CC} (V)	-40°C to +85°C			Unit
					Min	Typ	Max	
R _{ON}		On-Resistance	V _{IS} = 0 V to 0.4 V, I _{ON} = 8 mA	3.3	-	6.0	10	Ω
R _{FLAT}		On-Resistance Flatness	V _{IS} = 0 V to 1.0 V, I _{ON} = 8 mA	3.3	-	0.5	-	Ω
ΔR _{ON}		On-Resistance Matching	V _{IS} = 0 V to 0.4 V, I _{ON} = 8 mA	3.3	-	0.2	-	Ω

CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.

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TIMING/FREQUENCY (Typical: T = 25°C, V_{CC} = 3.3V, R_L = 50Ω, C_L = 5 pF, f = 1MHz)

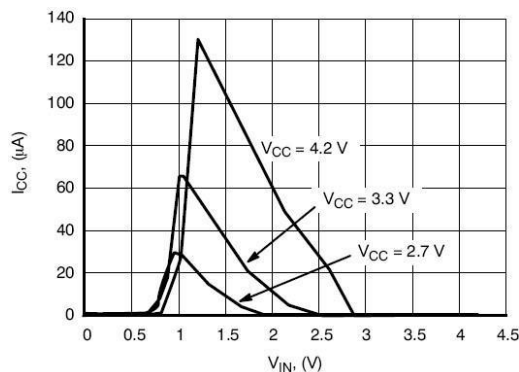
Symbol	Pins	Parameter	Test Conditions	V _{CC} (V)	-40°C to +85°C			unit
					Min	Typ	Max	
t _{ON}	Closed to Open	Turn-ON Time		1.65- 4.5	-	14	30	ns
t _{OFF}	Open to Closed	Turn-OFF Time		1.65- 4.5	-	10	20	ns
t _{BBM}		Break-Before-Ma ke Delay	V _{IS} = 0 V to V _{CC} , I _{ON} = 8 mA	1.65- 4.5	-	2.20 2.45 2.65	-	ns
BW		-3dB Bandwidth	C _L =5pF	3.0- 4.5	-	550	-	MHz
			C _L =0pF		-	900	-	

ISOLATION (Typical: T = 25°C, V_{CC} = 3.3V, R_L = 50Ω, C_L = 5 pF, f = 1 MHz)

Symbol	Pin	Parameter	Test Conditions	V _{CC} (V)	-40°C to +85°C			unit
					Min	Typ	Max	
O _{IRR}	Open	OFF-Isolation	f=250 MHz	1.65- 4.5	-	-30	-	dB
X _{TALK}	HSD1+ to HSD1-	Non-Adjacent Channel Crosstalk	f=250 MHz	1.65- 4.5	-	-45	-	dB

CAPACITANCE (Typical: T = 25°C, V_{CC} = 3.3 V, R_L = 50Ω, C_L = 5 pF, f = 1 MHz)

Symbol	Pins	Parameter	Test Conditions	V _{CC} (V)	-40°C to +85°C			unit
					Min	Typ	Max	
C _{IN}	\overline{OE}	Control Pin Input Capacitance		0		1.8		pF
C _{ON}	D+ to HSD1+ or HSD2+	ON Capacitance	\overline{OE} = 0 V	3.3		4.0		pF
C _{OFF}	HSD2+, HSD2-	OFF Capacitance	V _{IS} = 3.3 V \overline{OE} = 3.3 V	3.3		2.2		pF

Figure 2-a. I_{CC} vs. V_{IN}

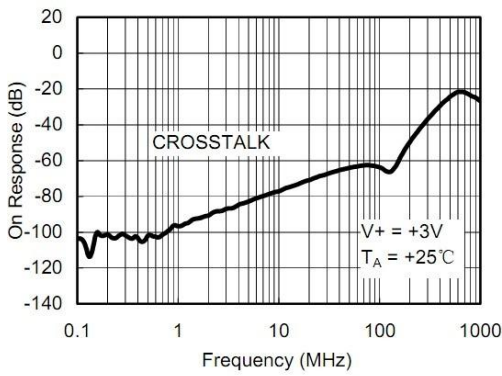


Figure 2-b. Response vs. frequency

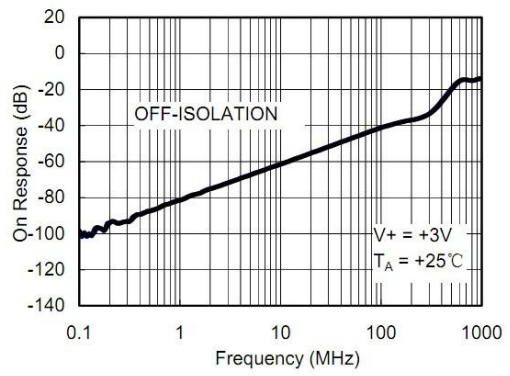


Figure 2-c. Response vs. frequency

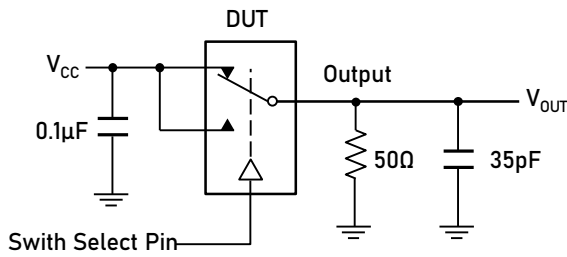


Figure 3. t_{BMM} (Time Break-Before-Make)

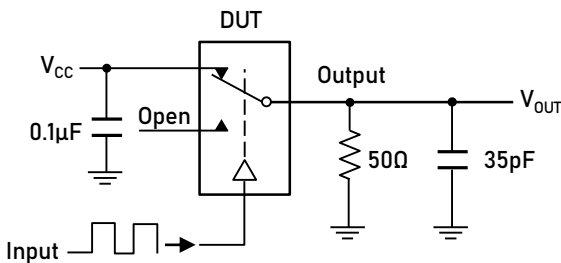
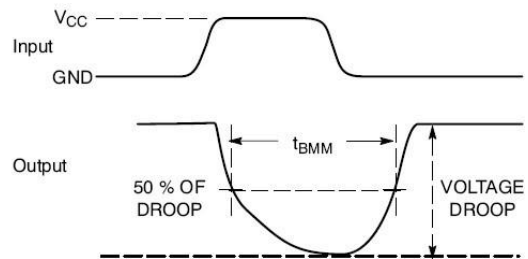


Figure 4. t_{ON}/t_{OFF}

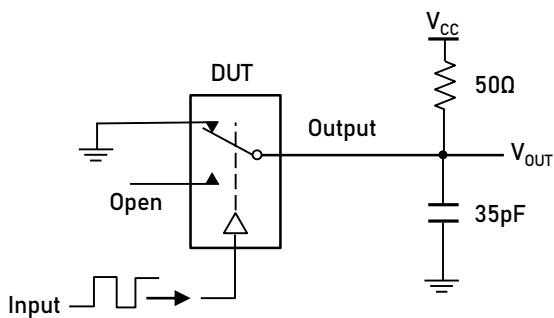
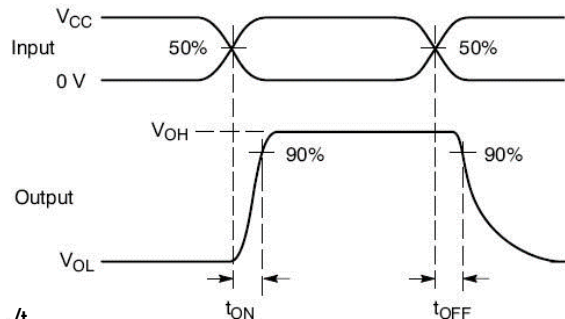
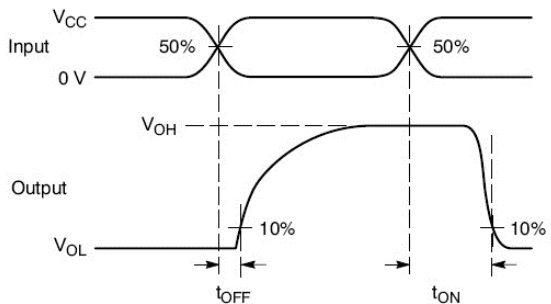


Figure 5. t_{ON}/t_{OFF}



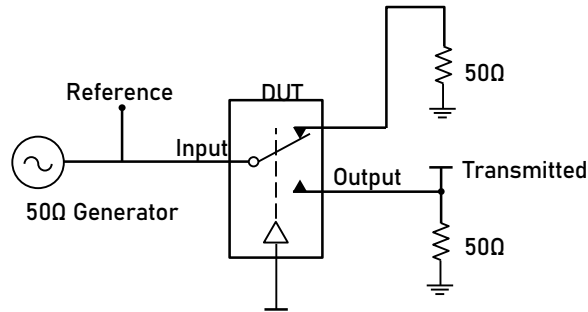


Figure6. Off Channel Isolation/On Channel Loss (BW)/Crosstalk (On Channel to Off Channel)/ V_{ONL}

Channel switch control/s test socket is normalized. Off isolation is measured across an off channel. On loss is the bandwidth of an On switch. V_{ISO} , Bandwidth and V_{ONL} are independent of the input signal direction.

$$V_{ISO} = \text{Off Channel Isolation} = 20 \text{ Log} \left(\frac{V_{OUT}}{V_{IN}} \right) \text{ for } V_{IN} \text{ at } 100 \text{ kHz}$$

$$V_{ONL} = \text{On Channel Loss} = 20 \text{ Log} \left(\frac{V_{OUT}}{V_{IN}} \right) \text{ for } V_{IN} \text{ at } 100 \text{ kHz}$$

Bandwidth (BW) = the frequency 3 dB below V_{ONL}

V_{CT} = Use V_{ISO} setup and test to all other switch analog input/outputs terminated with 50Ω

Typical Performance Curves $T_A = +25^\circ\text{C}$, Unless Otherwise Specified (Continued)

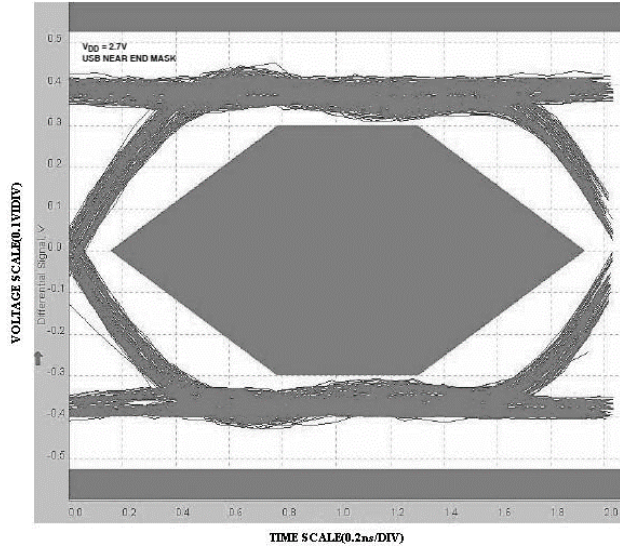


Figure7. EYE PATTERN: 480Mbps WITH USB SWITCHES IN THE SIGNAL PATH

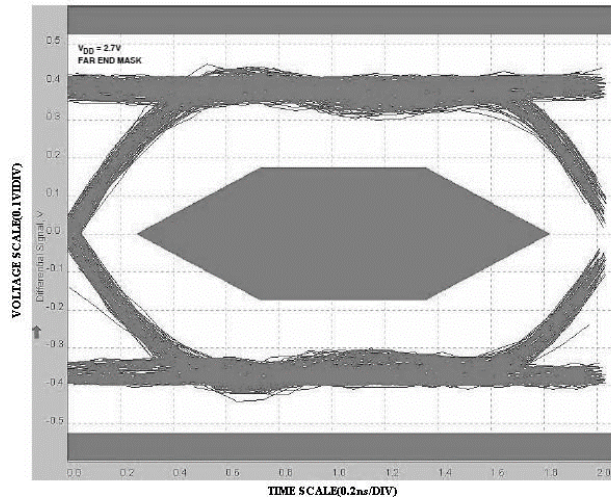


Figure8. EYE PATTERN: 480Mbps WITH USB SWITCHES IN THE SIGNAL PATH

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