General Description

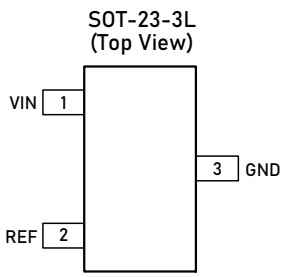
The LTR33 series devices are low temperature drift (20 ppm/℃ maximum), low-power, high-precision CMOS voltage reference, featuring ±0.15% initial accuracy, low operating current with power consumption less than 500μA. This device also offers very low output noise of 12 $\mu V_{PP}/V$, which enables its ability to maintain high signal integrity with high-resolution data converters in noise critical systems.

Packaged in the same SOT-23-3 package, LTR33xx offers enhanced specifications and pin-to-pin replacement for REF33xx and LM4132. Stability and system reliability are further improved by the low output-voltage hysteresis of the device and low long-term output voltage drift. LTR33xx is specified for the wide temperature range of −40 to +85 ℃.

Features and Benefits

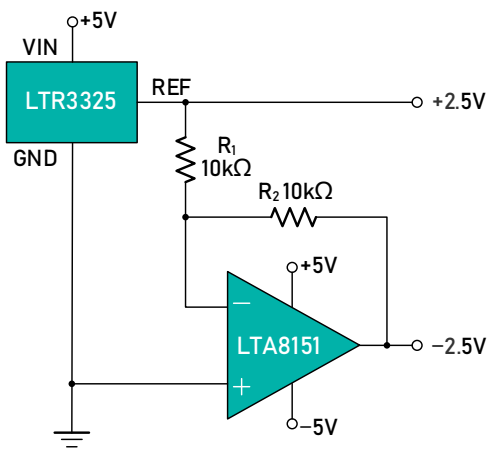
- Voltage options: 1.25V, 2.048V, 2.5V, 3.0V, 3.3V, 4.096V
- Initial accuracy: ±0.15% (maximum)
- Low temperature coefficient: 20 ppm/℃ (maximum)
- Output 1/f noise at 0.1 to 10 Hz: 12 $\mu V_{PP}/V$
- Excellent line regulation: 100 ppm/V
- Supply voltage: 2.7 to 5.5 V
- Power consumption: < 500 μA
- Startup time: < 2ms
- Operating temperature: −40 to 85 ℃

Pin Configuration



Applications

- Data acquisition (DAQ)
- PLC analog I/O modules
- Field transmitters
- Motor drive control module
- Battery test equipment
- LCR meters



Pin Description

Pin. Name	Pin Description
VIN	Power supply voltage
GND	Ground.
REF	Reference voltage outputs , an external capacitor is required.

Ordering Information (1)

Type Number	Output Voltage	Temperature Coefficient	Operating Temperature	Package Name
LTR3312T20YT3	1.25V	20ppm/℃	−40 to 85 ℃	SOT-23-3
LTR3320T20YT3	2.048V	20ppm/℃	−40 to 85 ℃	SOT-23-3
LTR3325T20YT3	2.5V	20ppm/℃	−40 to 85 ℃	SOT-23-3
LTR3330T20YT3	3.0V	20ppm/℃	−40 to 85 ℃	SOT-23-3
LTR3333T20YT3	3.3V	20ppm/℃	−40 to 85 ℃	SOT-23-3

(1) Please contact to your Linearin representative for the latest availability information and product details.

Limiting Value – In accordance with the Absolute Maximum Rating System (IEC 60134).

Operating Ambient Temperature Range	−40 to 85 ℃
Storage Temperature Range	−50 to 125 ℃
Input Voltage Range	−0.3 V to 5.5 V
ESD protection	> 2000 V

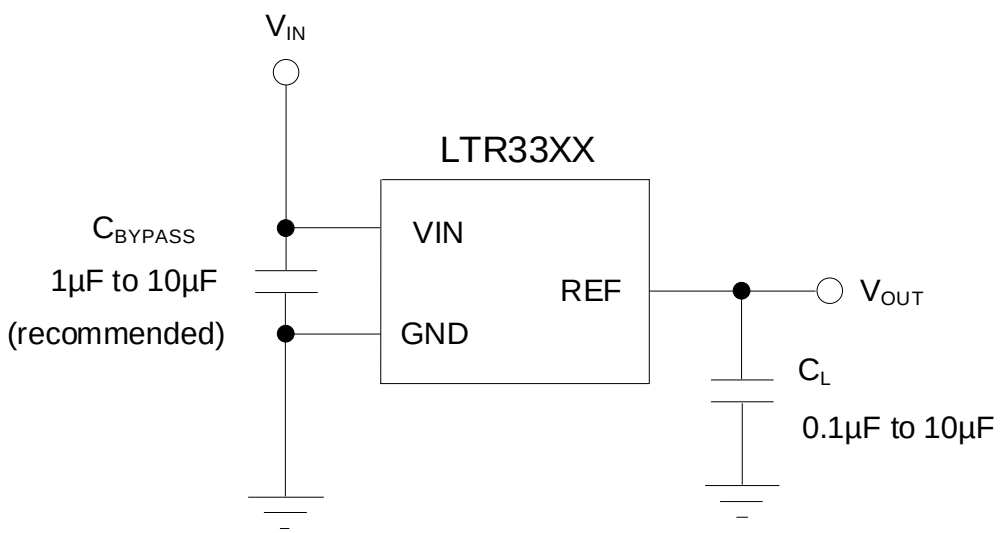
Note: Stresses exceeding those listed in the Maximum Rating stable may damage the device. Operation beyond the maximum Rating conditions or under harsh conditions may affect product reliability and function.

Electrical Characteristics

Symbol	Parameter	Description	Min.	Typ.	Max.	Unit
V_{IN}	Power supply voltage		2.7	5	5.5	V
I_{CC}	Power consumption	V_{CC} = 5.0V, no load.		300	500	µA
V_{OUT}	Output voltage	LTR3312		1.25		V
		LTR3320		2.048		V
		LTR3325		2.5		V
		LTR3330		3.0		V
		LTR3333		3.3		V
		LTR3340		4.096		V
ΔV_{OUT}	Output voltage accuracy		−0.15		0.15	%
T_C	Temperature coefficient				20	ppm/°C
$V_{IN}-V_{OUT}$	Dropout Voltage			200		mV
$\Delta V_{OUT}/\Delta V_{IN}$	Line Regulation				100	ppm/V
$\Delta V_{OUT}/\Delta I_L$	Load Regulation				50	ppm/mA

Note: Low current coefficient version is available by Q2/2022.

Typical Application



Layout

Layout Guidelines

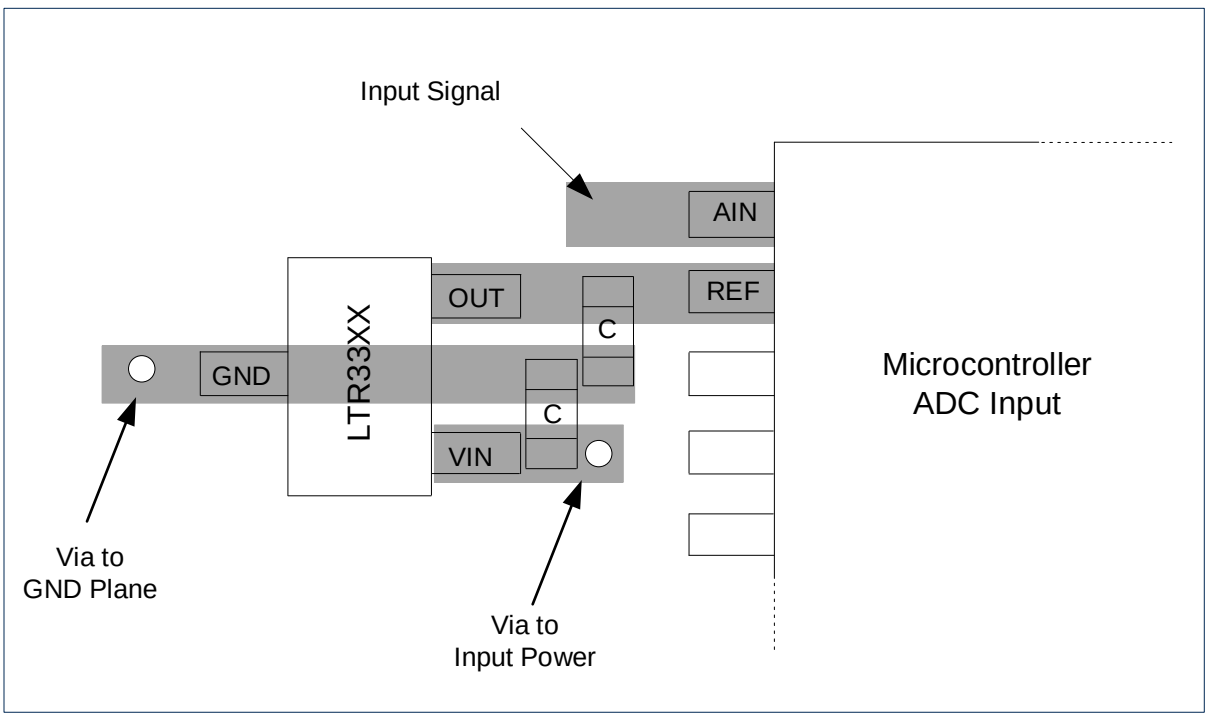
For optimal performance of this design，please follow standard printed circuit board (PCB) layout guidelines, including proper decoupling close to all integrated circuits and adequate power and ground connections with large copper pours.

As shown below an example of a PCB layout for a data acquisition system using the LTR33xx.

Some key considerations are:

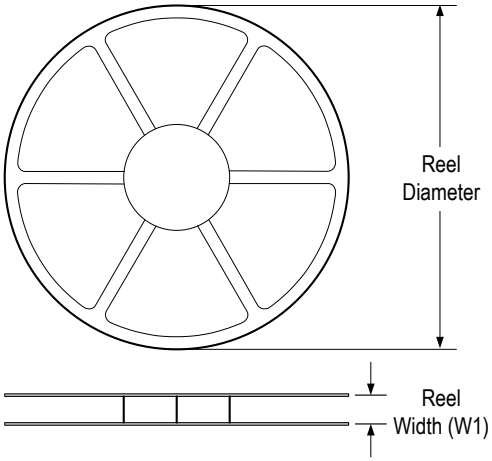
- Connect a low-ESR, 1µF ceramic capacitor at the IN pin for bypass, and a 0.1uF to 10uF ceramic capacitor at the OUT pin for stability of the LTR33xx.
- Decouple other active devices in the system per the device specifications.
- Use a solid ground plane helps distribute heat and reduces EMI noise pickup.
- Place the external components as close to the device as possible. This configuration prevents parasitic errors (such as the Seebeck effect) from occurring.
- Minimize trace length between the reference and bias connections to the ADC to reduce noise pickup·
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when absolutely necessary.

Layout Example

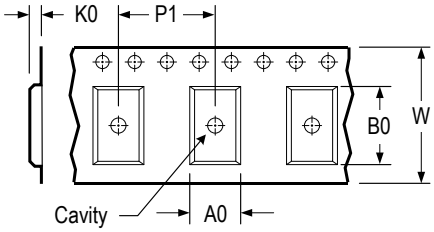


Tape and Reel Information

REEL DIMENSIONS

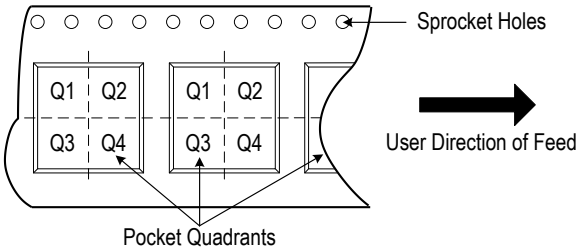


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIETATION IN TAPE

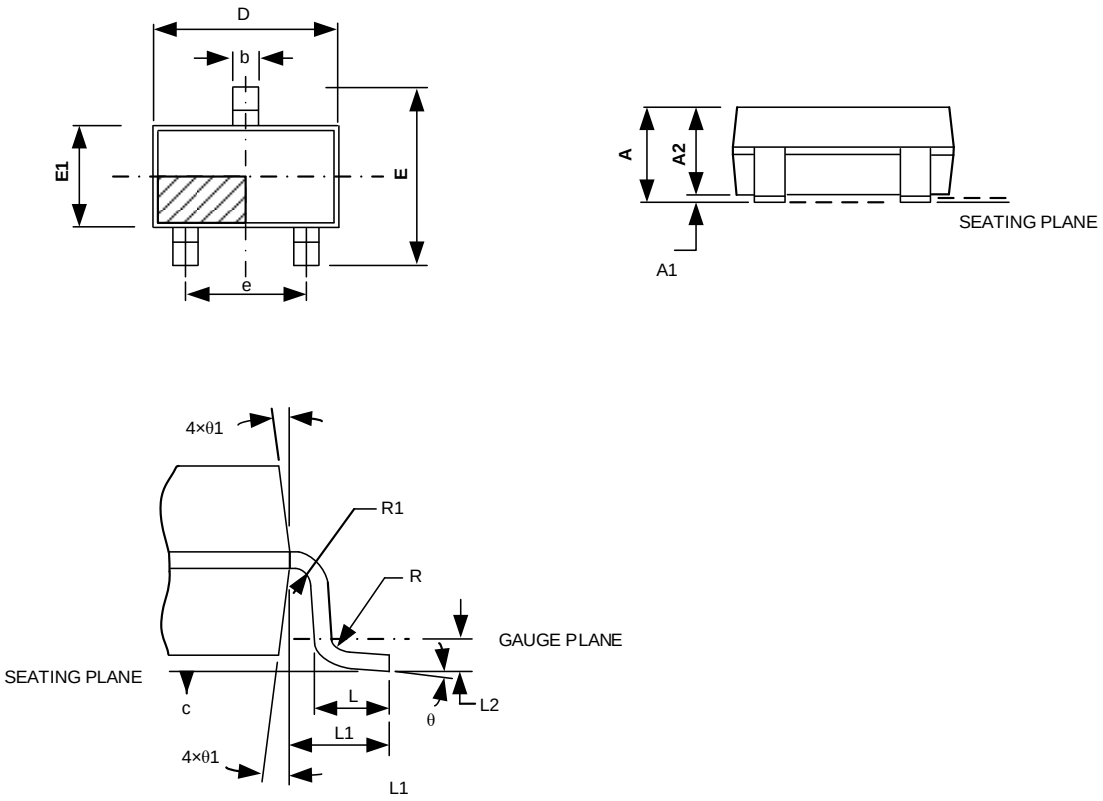


* All dimensions are nominal

Device	Package Type	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin 1 Quadrant
LTR3312T20YT3	SOT23	3	3 000	178	9.0	3.3	3.2	1.5	4.0	8.0	Q3

Package Outlines

DIMENSIONS, SOT-23-3



Symbol	Min.	Typ.	Max.
A	–	–	1.35
A1	0	–	0.15
A2	1.0	1.1	1.2
b	0.35	–	0.45
b1	0.32	–	0.38
C	0.14	–	0.20
C1	0.14	0.15	0.16
D	2.82	2.92	3.02
E	2.60	2.80	3.00
E1	1.526	1.626	1.726
e	1.8	1.9	2.0
L	0.35	0.45	0.6
L1	0.6REF		
L2	0.25REF		
R	0.1	–	–
R1	0.1	–	0.25
θ	0°	4°	8°
θ1	5°	10°	15°

(Unit: mm)

单击下面可查看定价，库存，交付和生命周期等信息

>>Linearin(先积)