LTC8741, LTC8742, LTC8743 , LTC8744

33ns, Micro-Power, 1.8V, RRI, Push-Pull Output Comparators

General Description

The LTC8741/8742/8743/8744 are single-, dual-, and quad- channel comparators with push-pull output that offer the ultimate combination of high speed (33 ns propagation delay) and micro power consumption (135 µA), available in small packages with features such as rail-to-rail inputs, low offset voltage (0.8 mV), large output drive current, and a wide range of supply voltages from 1.8 V to 5.5 V. The devices are very easy to implement in a wide variety of applications where require critical response time, power-sensitive, low-voltage, and/or tight board space. The output of the LTC8741/8742/8743/8744 pulls to within 0.1 V of either supply rail without external pull-up circuitry, making these devices ideal for interface with both CMOS and TTL logics. All input and output pins can tolerate a continuous short-circuit fault condition to either rail. Internal hysteresis ensures clean output switching, even with slow-moving input signals.

The LTC8741/LTC8743 (single) is available in both SOT23-5L and SC70-5L packages. The LTC8742 (dual) is offered in DFN-8L, SOIC-8L and MSOP-8L packages. The LTC8744 (quad) is offered in SOIC-14L and TSSOP-14L packages. All devices are rated over –40 ℃ to +125 ℃ industrial temperature range.

Features and Benefits

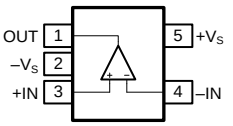
- Fast 33 ns Propagation Delay (100-mV Overdrive)
- Micro-power Operating Current (135 µA) Preserves Battery Power
- Single 1.8 V to 5.5 V Supply Voltage Range
  - Can be Powered From the Same 1.8V/2.5V/3.3V/5V System Rails
- Rail-to-Rail Input
- Push-Pull Output Current Drive: 30 mA Typically at 5V Supply
- Internal Hysteresis for Clean Switching
- Internal RF/EMI Filter
- Operating Temperature Range: –40 ℃ to +125 ℃

Applications

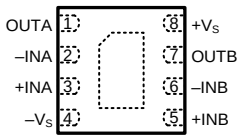
- Consumer Accessories
- Handsets, Tablets and Notebooks
- Portable and Battery-Powered Devices
- Alarms and Monitoring Circuits
- Zero-Crossing Detectors
- Threshold Detectors and Discriminators
- Window Comparators
- IR Receivers
- Level Translators
- Line Receivers

Pin Configurations (Top View)

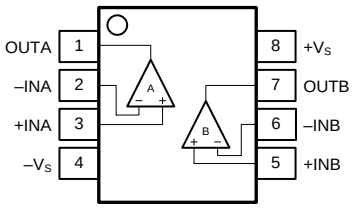
LTC8741
SOT23-5L / SC70-5L



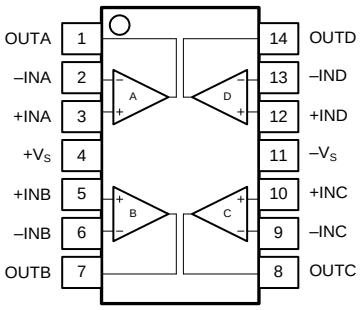
LTC8742
DFN-8L



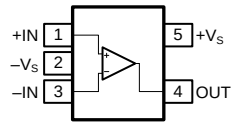
LTC8742
SOIC-8L / MSOP-8L



LTC8744
SOIC-14L / TSSOP-14L



LTC8743
SOT23-5L / SC70-5L



Pin Description

Symbol	Description
–IN	Negative input. The voltage range is from (V_{S-} – 0.1V) to (V_{S+} + 0.1V).
+IN	Positive input. This pin has the same voltage range as –IN.
$+V_S$	Positive power supply. The voltage is from 1.8 V to 5.5 V. Split supplies are possible as long as the voltage between V_{S+} and V_{S-} is from 1.8 V to 5.5 V.
$-V_S$	Negative power supply. It is normally tied to ground. It can also be tied to a voltage other than ground as long as the voltage between V_{S+} and V_{S-} is from 1.8 V to 5.5 V.
OUT	Comparator output.

Ordering Information

Orderable Type Number	Package Name	Package Quantity	Eco Class(1)	Operating Temperature	Marking Code
LTC8741YT5/R6	SOT23-5L	3 000	Green	–40℃ to +125℃	CM1
LTC8741YC5/R6	SC70-5L	3 000	Green	–40℃ to +125℃	CM1
LTC8742YS8/R8	SOIC-8L	4 000	Green	–40℃ to +125℃	CM2 Y
LTC8742YV8/R6	MSOP-8	3 000	Green	–40℃ to +125℃	CM2Y
LTC8742YF8/R6	DFN2x2-8L	3 000	Green	–40℃ to +125℃	CM2
LTC8743YT5/R6	SOT23-5L	3 000	Green	–40℃ to +125℃	CM3
LTC8743YC5/R6	SC70-5L	3 000	Green	–40℃ to +125℃	CM3
LTC8744YS14/R5	SOIC-14L	2 500	Green	–40℃ to +125℃	CM4 Y
LTC8744YT14/R6	TSSOP-14L	3 000	Green	–40℃ to +125℃	CM4 Y

(1) Eco Class - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & Halogen Free).
(2) Please contact to your Linearin representative for the latest availability information and product content details.

Limiting Value

In accordance with the Absolute Maximum Rating System (IEC 60134).

Parameter	Absolute Maximum Rating
Supply Voltage, V_{S+} to V_{S-}	10.0 V
Signal Input Terminals: Voltage, Current	V_{S-} – 0.3 V to V_{S+} + 0.3 V, ±10 mA
Output Short-Circuit	Continuous
Storage Temperature Range, T_{stg}	–65 ℃ to +150 ℃
Junction Temperature, T_J	150 ℃
Lead Temperature Range (Soldering 10 sec)	260 ℃

ESD Rating

Parameter	Item	Value	Unit
Electrostatic Discharge Voltage	Human body model (HBM), per MIL-STD-883J / Method 3015.9	±5 000	V
	Charged device model (CDM), per ESDA/JEDEC JS-002-2014	±2 000	
	Machine model (MM), per JESD22-A115C	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Electrical Characteristics

V_S = 5.0V, T_A = +25°C, unless otherwise noted.

Boldface limits apply over the specified temperature range, T_A = −40 to +125 °C.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
OFFSET VOLTAGE						
V_{OS}	Input offset voltage	V_{CM} = 0		±0.8	±3.5	mV
		T_A = −40 to +125 °C			**±4.0**	
V_{OS} TC	Offset voltage drift	T_A = −40 to +125 °C		**±1**		µV/°C
PSRR	Power supply rejection ratio	V_S = 1.8 to 5.5 V, V_{S-} < V_{CM} < V_{S+}	65	80		dB
		(V_{S-}+0.1V) < V_{CM} < (V_{S+}−0.2V), T_A = −40 to +125 °C	**60**			
Hyst	Input hysteresis	V_{CM} = 0		3		mV
INPUT BIAS CURRENT						
I_B	Input bias current	V_{CM} = V_{S+} /2		5		pA
		T_A = +85 °C		200		
		T_A = +125 °C		1,000		
I_{OS}	Input offset current	V_{CM} = V_{S+} /2		10		pA
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage range	T_A = −40 to +85 °C	V_{S-}−0.1		V_{S+}+0.1	V
		T_A = −40 to +125 °C	V_{S-}+0.1		V_{S+}−0.2	
CMRR	Common-mode rejection ratio	V_{CM} = −0.1 to 5.0 V	60	82		dB
		V_{CM} = 0.1 to 4.8 V, T_A = −40 to +125°C	**55**			
		V_S = 2.0 V, V_{CM} = −0.1 to 2.0 V	56	78		
		V_{CM} = 0.1 to 1.8 V, T_A = −40 to +125 °C	**52**			
INPUT IMPEDANCE						
R_{IN}	Input resistance		100			GΩ
C_{IN}	Input capacitance	Differential		2.0		pF
		Common mode		3.5		
OUTPUT						
V_{OH}	High output voltage swing	I_{SOURCE} = 1 mA		63	80	mV
		T_A = −40 to +125 °C			120	
V_{OL}	Low output voltage swing	I_{SINK} = 1 mA		44	58	mV
		T_A = −40 to +125 °C			90	
I_{SC}	Output short-circuit current			±30		mA
POWER SUPPLY						
V_S	Operating supply voltage	T_A = −40 to +125 °C	1.8		5.5	V
I_Q	Quiescent current (per comparator)	V_S = 5.0 V, V_{CM} = 0.5V, I_O = 0		135	190	µA
		T_A = −40 to +125 °C			**230**	
		V_S = 1.8 V, V_{CM} = 0.5V, I_O = 0		170	220	
		T_A = −40 to +125 °C			**280**	

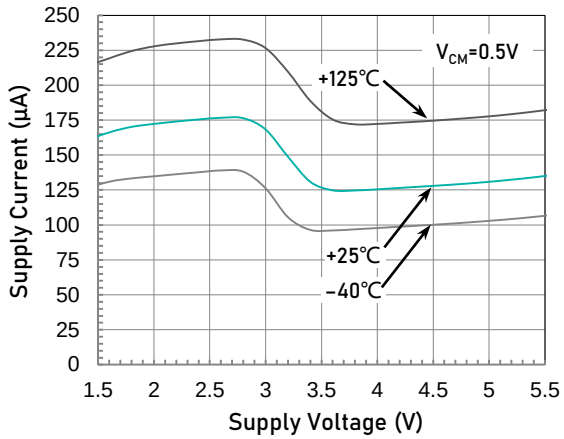
Electrical Characteristics (continued)

V_S = 5.0V, T_A = +25°C, unless otherwise noted.
Boldface limits apply over the specified temperature range, T_A = –40 to +125 °C.

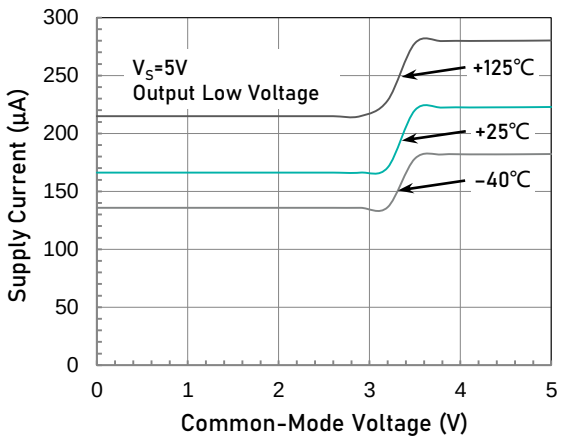
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
SWITCHING CHARACTERISTICS						
t_{PD-}	Propagation delay time, High to low	Input overdrive = 100 mV, C_L = 15 pF		33		ns
		Input overdrive = 20 mV, C_L = 15 pF		57		
t_{PD+}	Propagation delay time, Low to high	Input overdrive = 100 mV, C_L = 15 pF		39		ns
		Input overdrive = 20 mV, C_L = 15 pF		60		
t_F	Fall time	Input overdrive = 100 mV, C_L = 15 pF		5		ns
		Input overdrive = 20 mV, C_L = 15 pF		7		
t_R	Rise time	Input overdrive = 100 mV, C_L = 15 pF		8		ns
		Input overdrive = 20 mV, C_L = 15 pF		9		
THERMAL CHARACTERISTICS						
T_A	Operating temperature range		-40		+125	°C
θ_{JA}	Package Thermal Resistance	SC70-5L		333		°C/W
		SOT23-5L		190		
		DFN2x2-8L		80		
		MSOP-8L		216		
		SOIC-8L		125		
		TSSOP-14L		112		
		SOIC-14L		115		

Typical Performance Characteristics

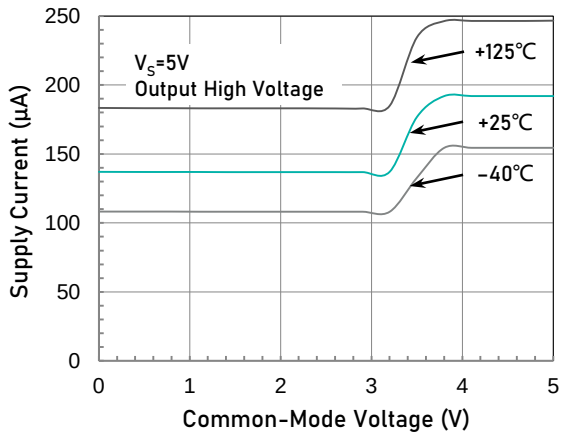
At T_A=+25°C, V_S=±2.5V, V_{CM}=V_S/2, R_L=10kΩ connected to V_S/2, and C_L=15pF, unless otherwise noted.



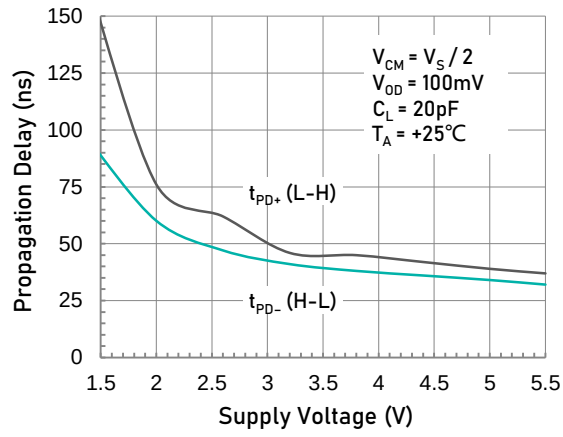
Supply Current vs. Supply Voltage



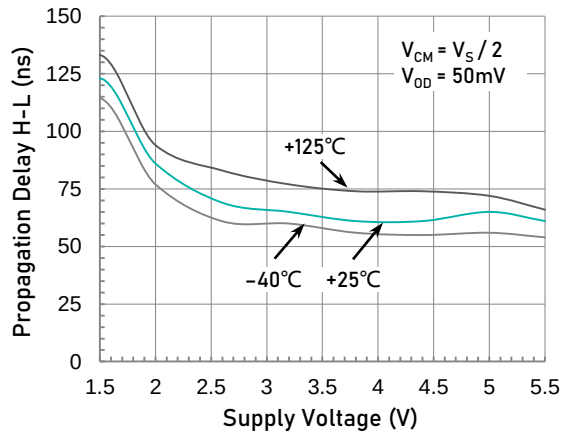
Supply Current vs. Common-Mode Input



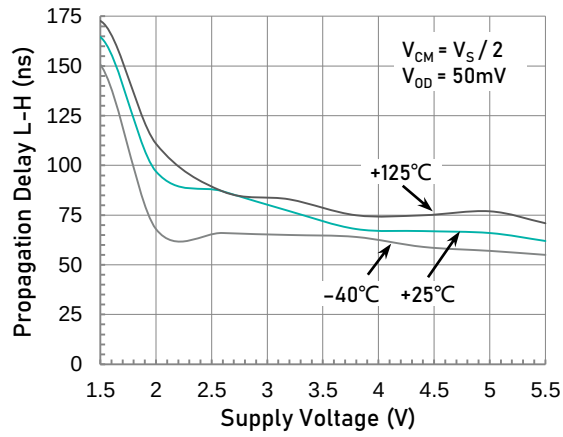
Supply Current vs. Common-Mode Input



Propagation Delay vs. Supply Voltage



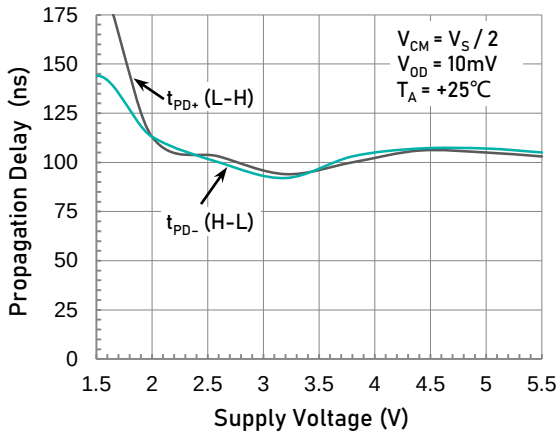
Propagation Delay H-L (t_{PD-}) vs. Supply Voltage



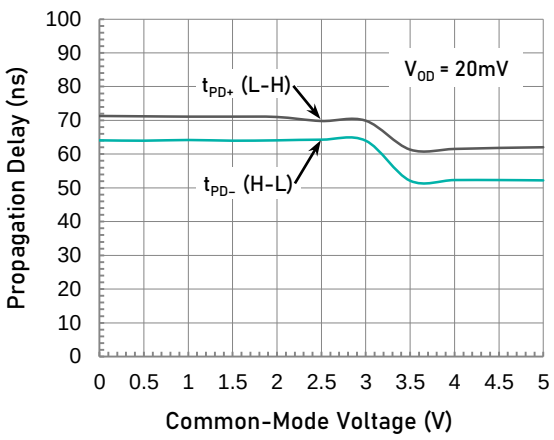
Propagation Delay L-H (t_{PD+}) vs. Supply Voltage

Typical Performance Characteristics

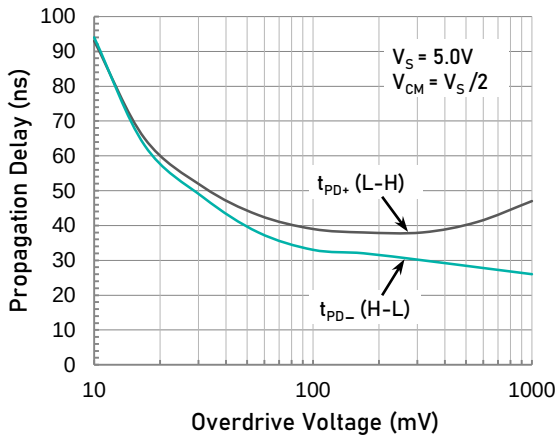
At T_A=+25°C, V_S=±2.5V, V_{CM}=V_S/2, R_L=10kΩ connected to V_S/2, and C_L=15pF, unless otherwise noted.



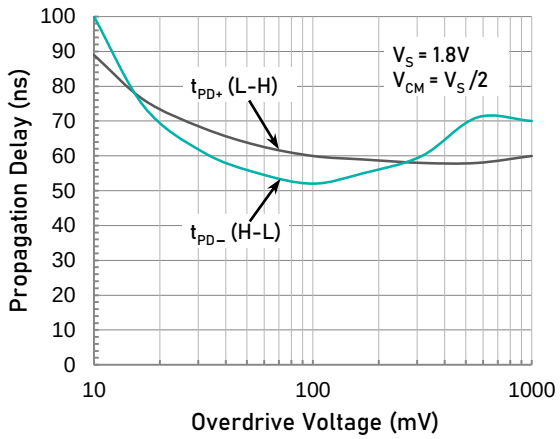
Propagation Delay vs. Supply Voltage



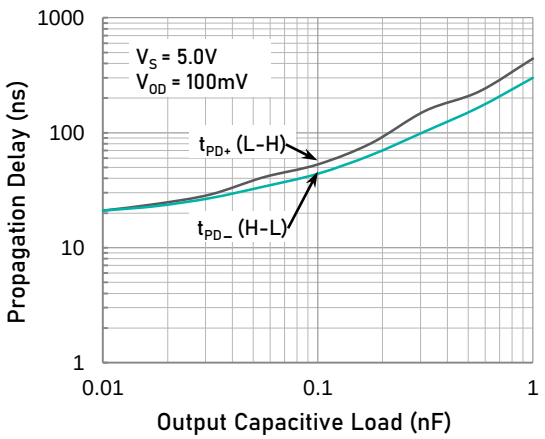
Propagation Delay vs. Input Common-Mode



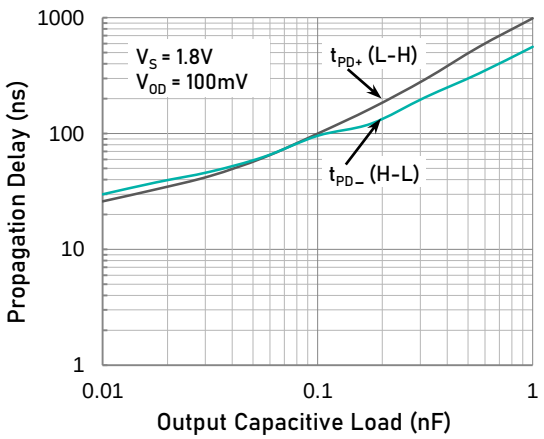
Propagation Delay vs. Input Overdrive



Propagation Delay vs. Input Overdrive



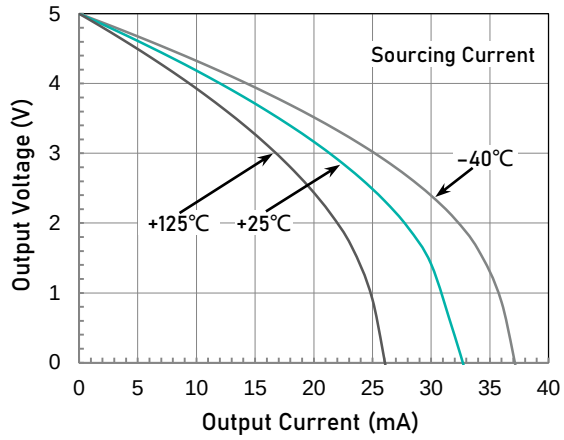
Propagation Delay vs. Capacitive Load



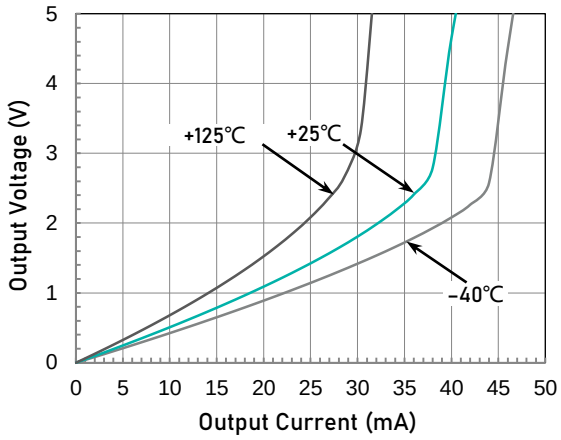
Propagation Delay vs. Capacitive Load

Typical Performance Characteristics

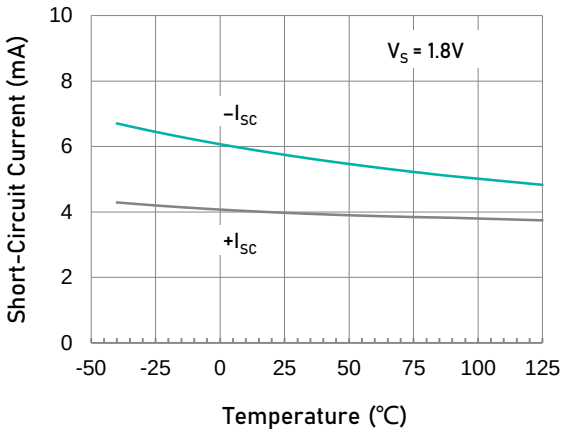
At T_A=+25℃, V_S=±2.5V, V_{CM}=V_S/2, R_L=10kΩ connected to V_S/2, and C_L=15pF, unless otherwise noted.



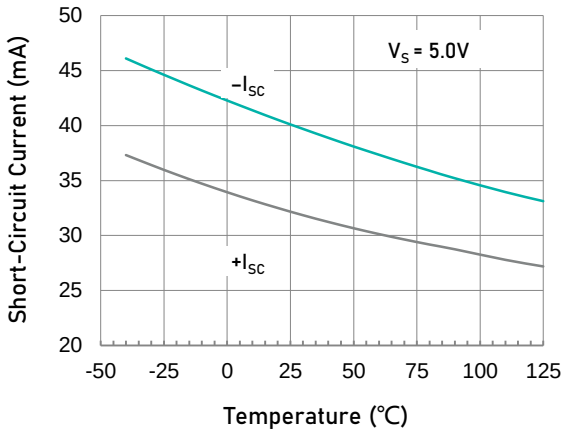
Output Voltage vs. Output Sourcing Current



Output Voltage vs. Output Sinking Current



Short Circuit Current vs. Temperature



Short Circuit Current vs. Temperature

Application Notes

OPERATING VOLTAGE

The LTC874x family of micro-power push-pull output comparators is fully specified and ensured for operation from 1.8 V to 5.5 V and offers an excellent speed-to-power combination with a propagation delay of 33 ns and a quiescent supply current of 135 µA. This combination of fast response time at micro-power enables power conscious systems to monitor and respond quickly to fault conditions.

In addition, and many specifications apply over the industrial temperature range of –40°C to +125°C. Parameters that vary significantly with operating voltages or temperature are illustrated in the Typical Characteristics graphs.

INPUT VOLTAGE

The input common-mode voltage range of the LTC874x comparators extends 100mV beyond the supply rails. This performance is achieved with a complementary input stage: an N-channel input differential pair in parallel with a P-channel differential pair. The N-channel pair is active for input voltages close to the positive rail, typically V_{S+}–1.4V to the positive supply, whereas the P-channel pair is active for inputs from 100mV below the negative supply to approximately V_{S+}–1.4V. There is a small transition region, typically V_{S+}–1.2V to V_{S+}–1V, in which both pairs are on. This 200mV transition region can vary up to 200mV with process variation. Thus, the transition region (both stages on) can range from V_{S+}–1.4V to V_{S+}–1.2V on the low end, up to V_{S+}–1V to V_{S+}–0.8V on the high end. Within this transition region, PSRR, CMRR, offset voltage, offset drift, and THD can be degraded compared to device operation outside this region.

INPUT VOLTAGE

The LTC8741/8742/8743/8744 comparator family uses CMOS transistors at the inputs which prevent phase inversion when the input pins exceed the supply voltages.

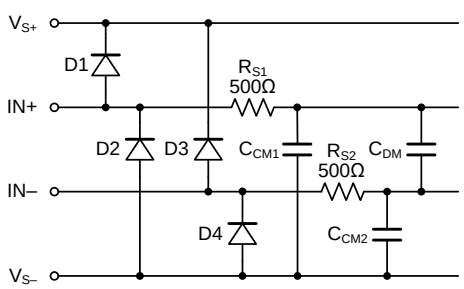


Figure 1. Input EMI Filter and Clamp Circuit

Figure 1 shows the input EMI filter and clamp circuit. The LTC8741/8742/8743/8744 comparators have internal ESD protection diodes (D1, D2, D3, and D4) that are connected between the inputs and each supply rail. These diodes protect the input transistors in the event of electrostatic discharge and are reverse biased during normal operation. This protection scheme allows voltages as high as approximately 300mV beyond the rails to be applied at the input of either terminal without causing permanent damage. See the table of Absolute Maximum Ratings for more information.

EMI REJECTION RATIO

Circuit performance is often adversely affected by high frequency EMI. When the signal strength is low and transmission lines are long, an amplifier must accurately amplify the input signals. However, all comparator pins — the non-inverting input, inverting input, positive supply, negative supply, and output pins — are susceptible to EMI signals. These high frequency signals are coupled into an comparator by various means, such as conduction, near field radiation, or far field radiation. For example, wires and printed circuit board (PCB) traces can act as antennas and pick up high frequency EMI signals.

Amplifiers do not amplify EMI or RF signals due to their relatively low bandwidth. However, due to the nonlinearities of the input devices, comparators can rectify these out of band signals. When these high frequency signals are rectified, they appear as a dc offset at the output.

The LTC8741/8742/8743/8744 comparators have integrated EMI filters at their input stage. A mathematical method of measuring EMIRR is defined as follows:

$$EMIRR = 20 \log (V_{IN\_PEAK} / \Delta V_{OS})$$

INTERNAL HYSTERESIS

Most high-speed comparators oscillate in the linear region because of noise or undesired parasitic feedback. This tends to occur when the voltage on one input is at or equal to the voltage on the other input. To counter the parasitic effects and noise, the devices have an internal hysteresis of 3 mV.

The hysteresis in a comparator creates two trip points: one for the rising input voltage and one for the falling input voltage. The difference between the trip points is the hysteresis. The average of the trip points is the offset voltage. When the comparator's input voltages are equal, the hysteresis effectively causes one comparator input voltage to move quickly past the other, thus taking the input out of the region where oscillation occurs. Standard comparators require hysteresis to be added with external resistors. To increase hysteresis and noise margin even more, add

Application Notes

positive feedback with two resistors as a voltage divider from the output to the non-inverting input. Figure 2 illustrates the case where IN– is fixed and IN+ is varied. If the inputs were reversed, the figure would look the same, except the output would be inverted.

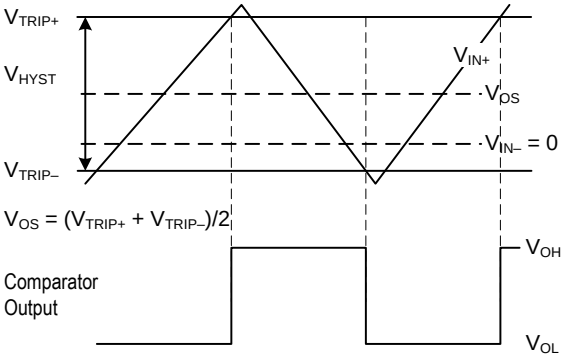


Figure 2. Input and Output Waveform, Non-inverting Input Varied

MAXIMIZING PERFORMANCE THROUGH PROPER LAYOUT

To achieve the maximum performance of the extremely high input impedance and low offset voltage of the LTC8741/8742/8743/8744 devices, care is needed in laying out the circuit board. The PCB surface must remain clean and free of moisture to avoid leakage currents between adjacent traces. Surface coating of the circuit board reduces surface moisture and provides a humidity barrier, reducing parasitic resistance on the board. The use of guard rings around the comparator inputs further reduces leakage currents. Figure 3 shows proper guard ring configuration and the top view of a surface-mount layout. The guard ring does not need to be a specific width, but it should form a continuous loop around both inputs. By setting the guard ring voltage equal to the voltage at the non-inverting input, parasitic capacitance is minimized as well. For further reduction of leakage currents, components can be mounted to the PCB using Teflon standoff insulators.

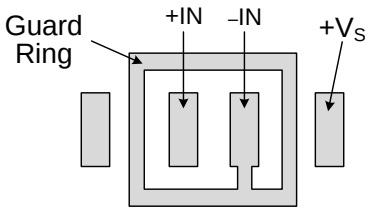


Figure 3. Use a guard ring around sensitive pins

Other potential sources of offset error are thermoelectric voltages on the circuit board. This voltage, also called Seebeck voltage, occurs at the junction of two dissimilar metals and is proportional to the temperature of the junction. The most common metallic junctions on a circuit board are solder-to-board trace and solder-to-component lead. If the temperature of the PCB at one end of the component is different from the temperature at the other end, the resulting Seebeck voltages are not equal, resulting in a thermal voltage error.

This thermocouple error can be reduced by using dummy components to match the thermoelectric error source. Placing the dummy component as close as possible to its partner ensures both Seebeck voltages are equal, thus canceling the thermocouple error. Maintaining a constant ambient temperature on the circuit board further reduces this error. The use of a ground plane helps distribute heat throughout the board and reduces EMI noise pickup.

INPUT-TO-OUTPUT COUPLING

To minimize capacitive coupling, the input and output signal traces should not be parallel. This helps reduce unwanted positive feedback.

Typical Application Circuits

IR RECEIVER AFE AND WAKE- UP CIRCUIT

Infrared (IR) communication is inherently immune to RF interference as long as there is a line-of-sight path between the transmitter and the receiver. It is also one of the lowest cost communication schemes. This makes it a good choice for implementing wireless communications in applications such as utility metering. A common system topology to extend battery life is to use a power efficient IR receiver analog front end (AFE) that is always on and wakes up the host only when there is a valid IR signal detected as shown in Figure 1.

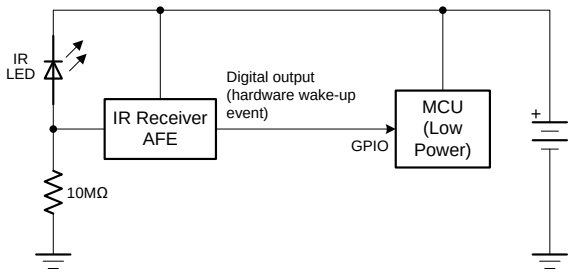


Figure 4. Coin Cell Battery Powered IR Receiver

Power efficient comparators such as the LTC874x can be used in the IR receiver AFE to increase battery life. The LTC874x device is responsible for two major tasks:

1. IR signal conditioning,
2. Host system wake-up.

The LTC874x device is constantly powered to always be ready to receive IR signals and wake up the host microcontroller (MCU) when data is received. The short working distance (approx 5 cm) is suitable for a virtual-contact operation where the IR transmitter and receiver are closely placed with an optional mechanical alignment guide.

Figure 1 shows the IR receiver system block diagram. The host MCU is normally in the shutdown mode (during which the quiescent current is less than 1 µA) except when data is being transferred.

Figure 2 shows the detailed circuit design. The circuit establishes a threshold through R_2 and C_1 which automatically adapts to the ambient light level. To further reduce BOM cost, this example uses an IR LED as the IR receiver. The IR LED is reverse-biased to function as a photodiode (but at a reduced sensitivity).

The low input bias current allows a greater load resistor value (R_1) without sacrificing linearity, which in turn helps reduce the always-on supply current.

The load resistor R_1 converts the IR light induced current into a voltage fed into the inverting input of the comparator. R_2 and C_1 establish a reference voltage V_{REF} which tracks the mean amplitude of the IR signal. The non-inverting input is connected to V_{REF} through R_3. And finally R_3 and R_4 are used to introduce additional hysteresis to keep the output free of spurious toggles.

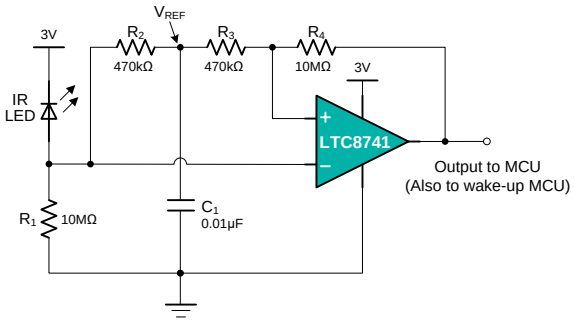


Figure 5. IR Receiver AFE Using LTC8741

USE WINDOW COMPARATOR TO DETECT UNDER-VOLTAGE AND OVER-VOLTAGE

Window comparators are commonly used to detect undervoltage (UV) and overvoltage (OV) conditions. Figure 6 shows a simple window comparator circuit.

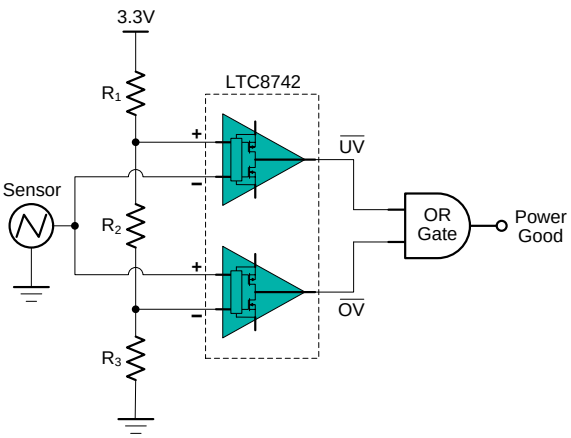


Figure 6. Window Comparator

For this design, follow these design requirements:

- Alert (logic low output) when an input signal is less than 1.1 V
- Alert (logic low output) when an input signal is greater than 2.2 V
- Alert signal is active low
- Operate from a 3.3-V power supply

Configure the circuit as shown in Figure 6. Connect V_{S+} to a 3.3-V power supply and V_{S-} to ground. Make R_1, R_2 and R_3 each 10-MΩ resistors. These three resistors are used to create the positive and negative thresholds for the window comparator (V_{TH+} and V_{TH-}). With each resistor being equal, V_{TH+} is 2.2 V and V_{TH-}

Typical Application Circuits

is 1.1 V. Large resistor values such as 10-MΩ are used to minimize power consumption. The sensor output voltage is applied to the inverting and non-inverting inputs of the 2-channel LTC8742's. The respective comparator outputs will be low when the sensor is less than 1.1 V or greater than 2.2 V. V_{OUT} will be high when the sensor is in the range of 1.1 V to 2.2 V. See the application curve in Figure 7.

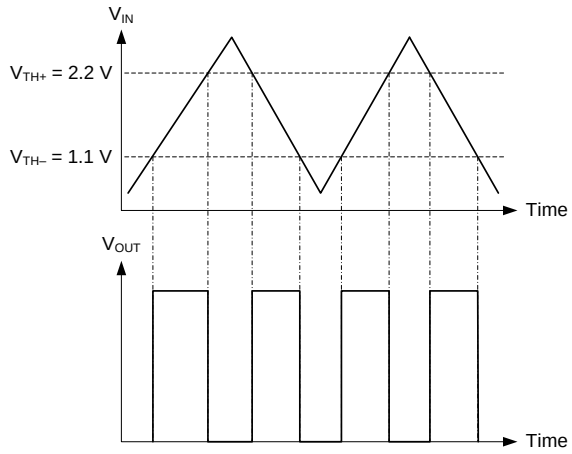
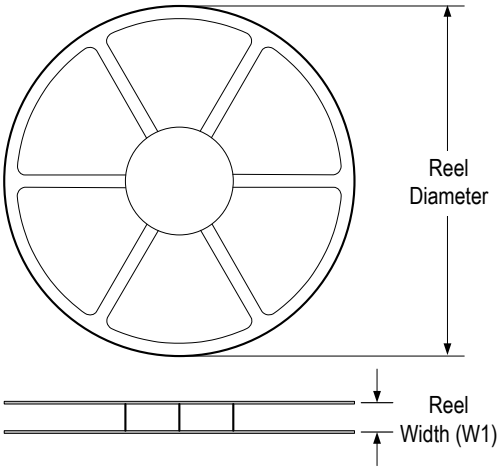


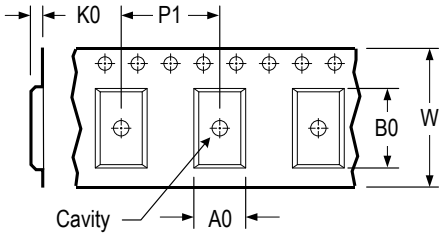
Figure 5. Window Comparator Results

Tape and Reel Information

REEL DIMENSIONS

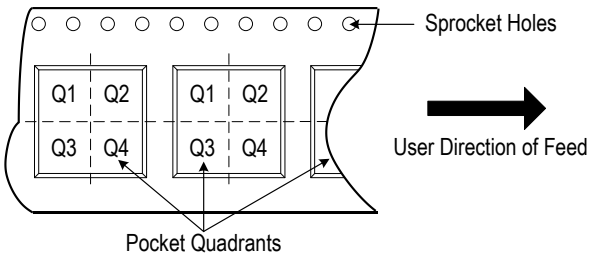


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIETATION IN TAPE

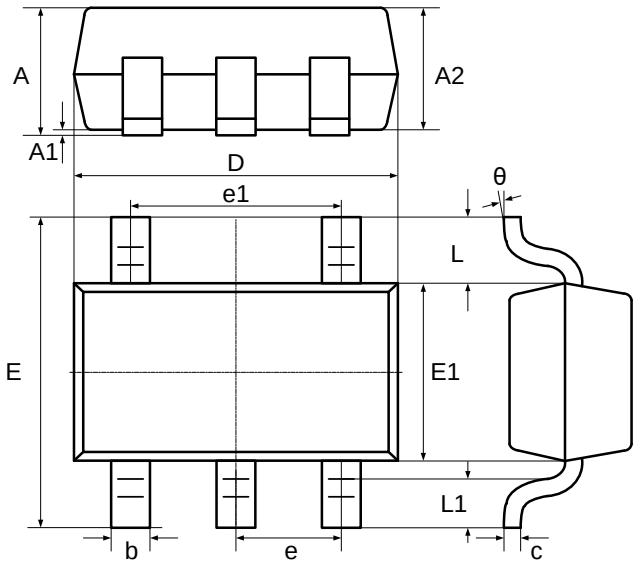


* All dimensions are nominal

Device	Package Type	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin 1 Quadrant
LTC8741YT5/R6	SOT23	5	3 000	178	9.0	3.3	3.2	1.5	4.0	8.0	Q3

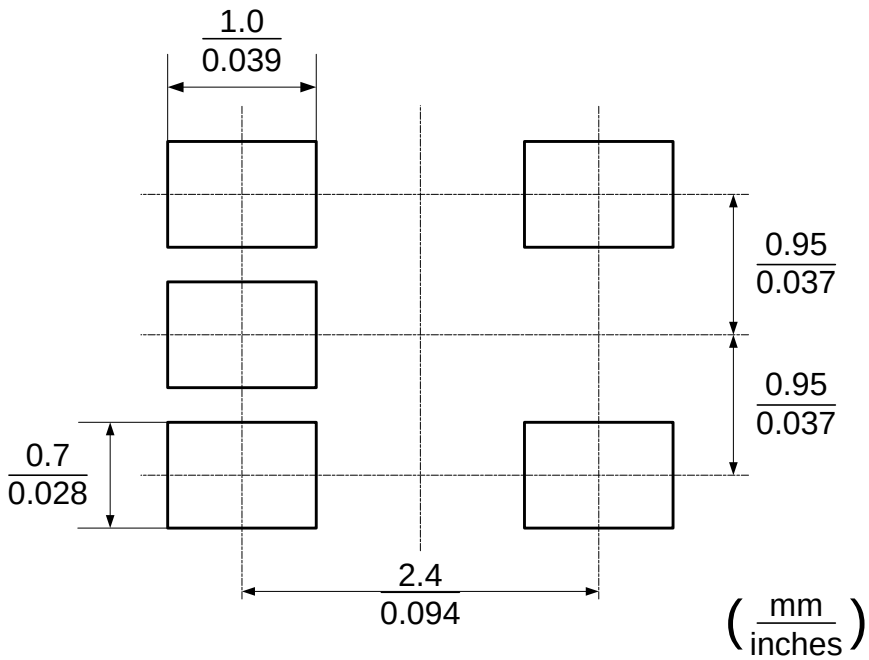
Package Outlines

DIMENSIONS, SOT23-5L



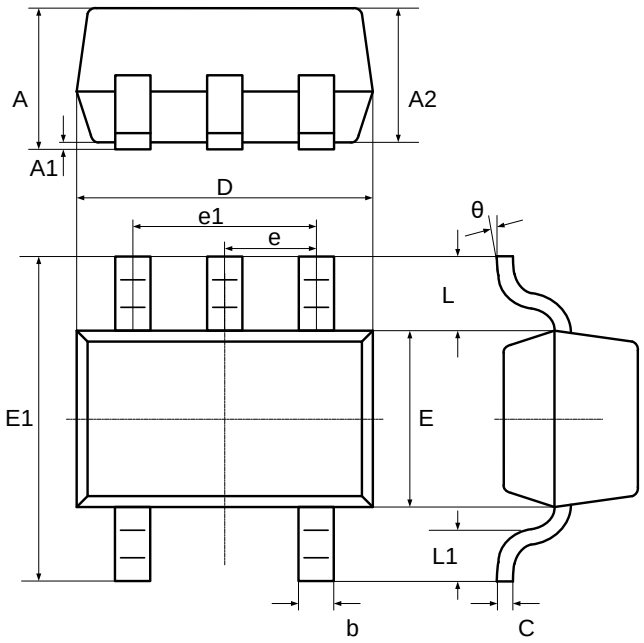
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	-	1.25	-	0.049
A1	0.04	0.10	0.002	0.004
A2	1.00	1.20	0.039	0.047
b	0.33	0.41	0.013	0.016
c	0.15	0.19	0.006	0.007
D	2.820	3.02	0.111	0.119
E1	1.50	1.70	0.059	0.067
E	2.60	3.00	0.102	0.118
e	0.95 BSC		0.037 BSC	
e1	1.90 BSC		0.075 BSC	
L	0.60 REF		0.024 REF	
L1	0.30	0.60	0.012	0.024
θ	0°	8°	0°	8°

RECOMMENDED SOLDERING FOOTPRINT, SOT23-5L



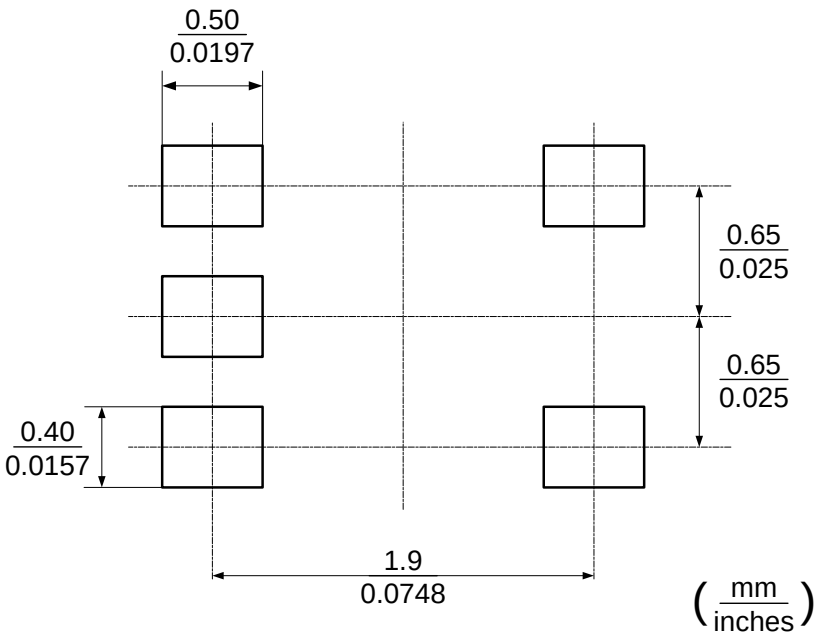
Package Outlines (continued)

DIMENSIONS, SC70-5L (SOT353)



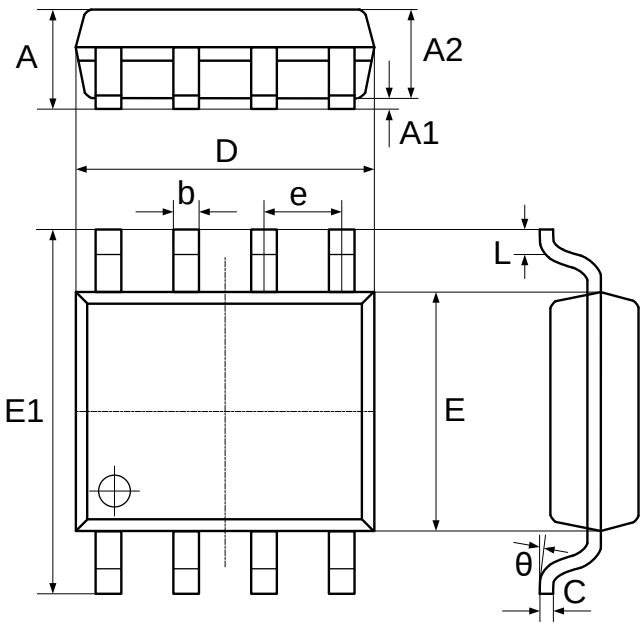
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.90	1.10	0.035	0.043
A1	0.00	0.10	0.000	0.004
A2	0.90	1.00	0.035	0.039
b	0.15	0.35	0.006	0.014
C	0.08	0.15	0.003	0.006
D	2.00	2.20	0.079	0.087
E	1.15	1.35	0.045	0.053
E1	2.15	2.45	0.085	0.096
e	0.65 typ.		0.026 typ.	
e1	1.20	1.40	0.047	0.055
L	0.525 ref.		0.021 ref.	
L1	0.26	0.46	0.010	0.018
θ	0°	8°	0°	8°

RECOMMENDED SOLDERING FOOTPRINT, SC70-5L (SOT353)



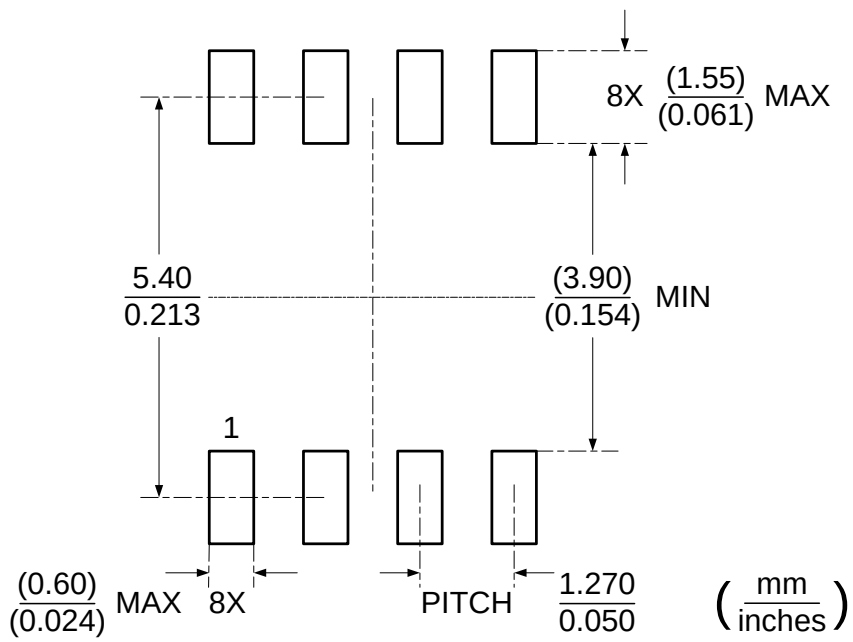
Package Outlines (continued)

DIMENSIONS, SOIC-8L



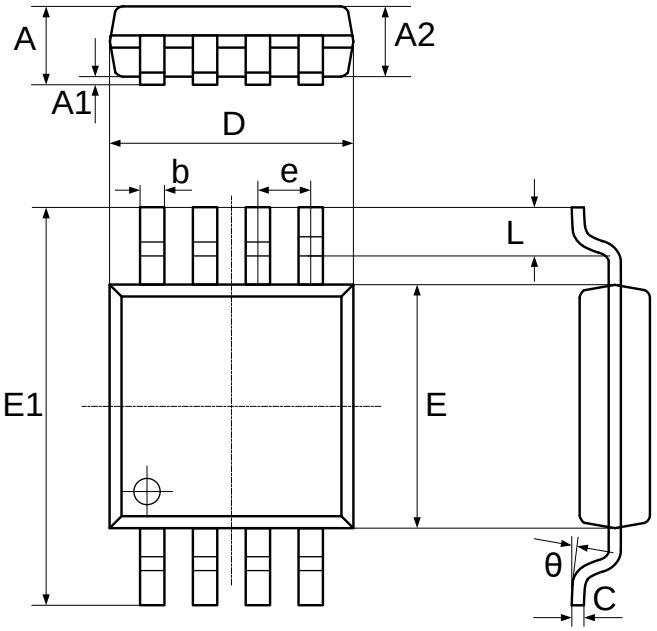
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.370	1.670	0.054	0.066
A1	0.070	0.170	0.003	0.007
A2	1.300	1.500	0.051	0.059
b	0.306	0.506	0.012	0.020
C	0.203 TYP.		0.008 TYP.	
D	4.700	5.100	0.185	0.201
E	3.820	4.020	0.150	0.158
E1	5.800	6.200	0.228	0.244
e	1.270 TYP.		0.050 TYP.	
L	0.450	0.750	0.018	0.030
θ	0°	8°	0°	8°

RECOMMENDED SOLDERING FOOTPRINT, SOIC-8L



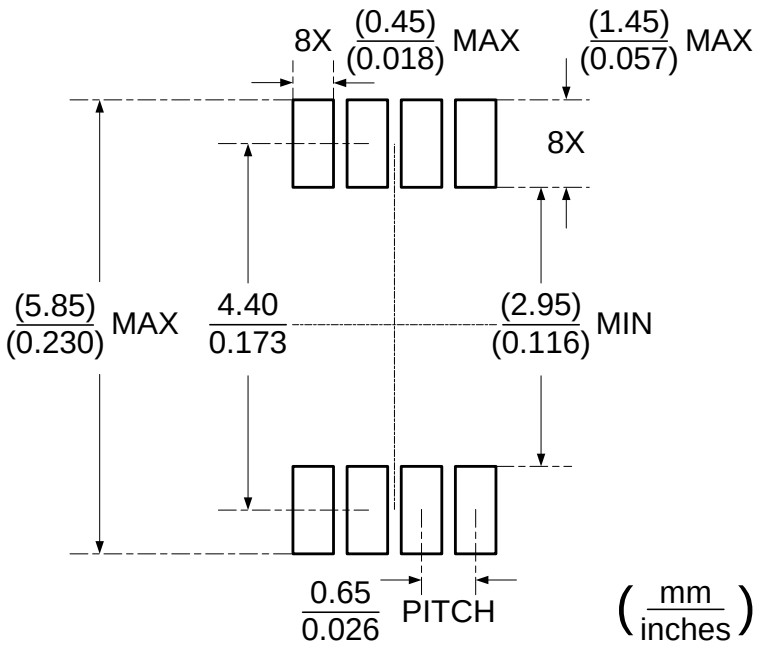
Package Outlines (continued)

DIMENSIONS, MSOP-8L



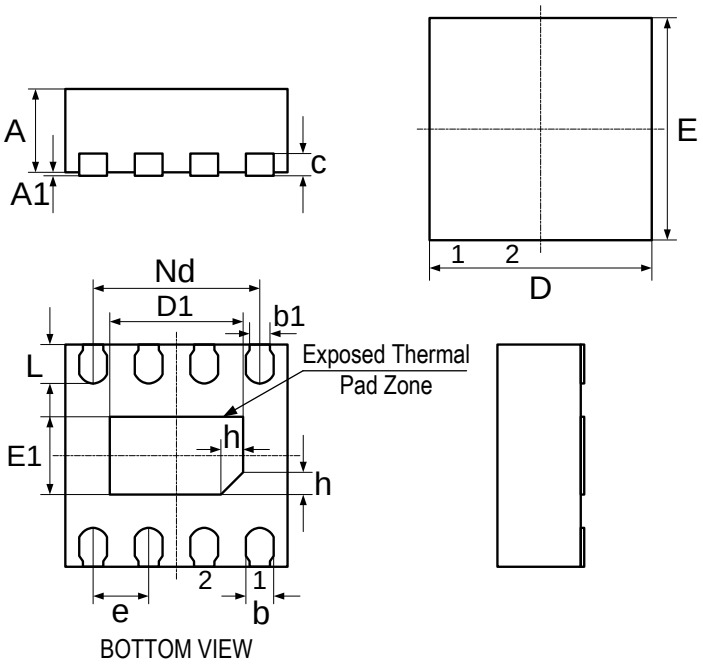
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.800	1.100	0.031	0.043
A1	0.050	0.150	0.002	0.006
A2	0.750	0.950	0.030	0.037
b	0.290	0.380	0.011	0.015
C	0.150	0.200	0.006	0.008
D	2.900	3.100	0.114	0.122
E	2.900	3.100	0.114	0.122
E1	4.700	5.100	0.185	0.201
e	0.650 TYP.		0.026 TYP.	
L	0.400	0.700	0.016	0.028
θ	0°	8°	0°	8°

RECOMMENDED SOLDERING FOOTPRINT, MSOP-8L



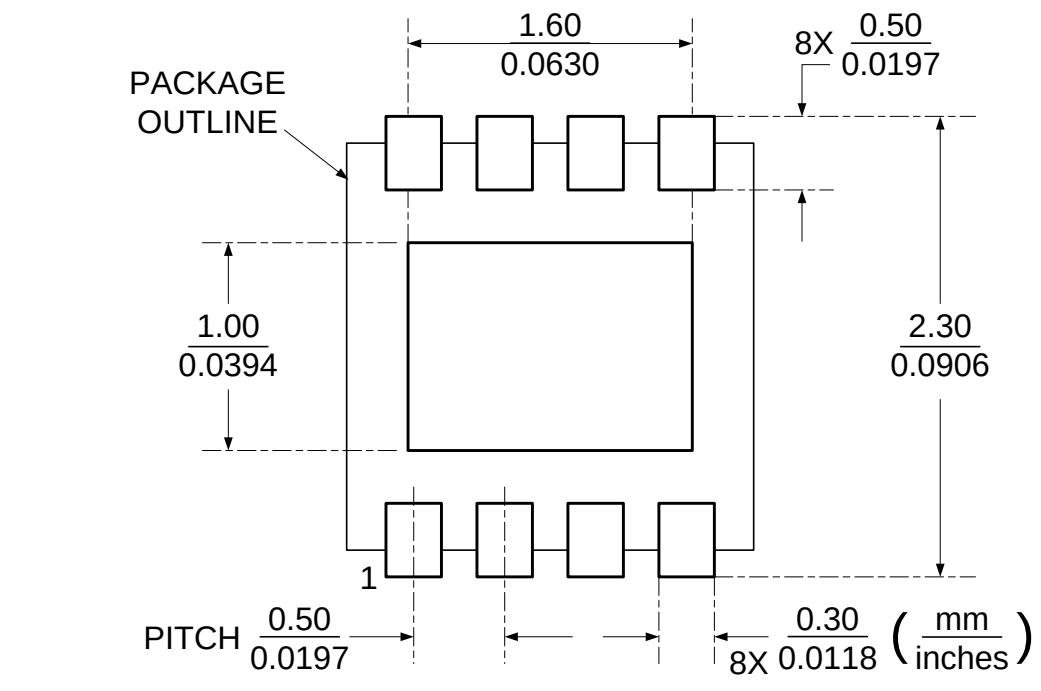
Package Outlines (continued)

DIMENSIONS, DFN2x2-8L



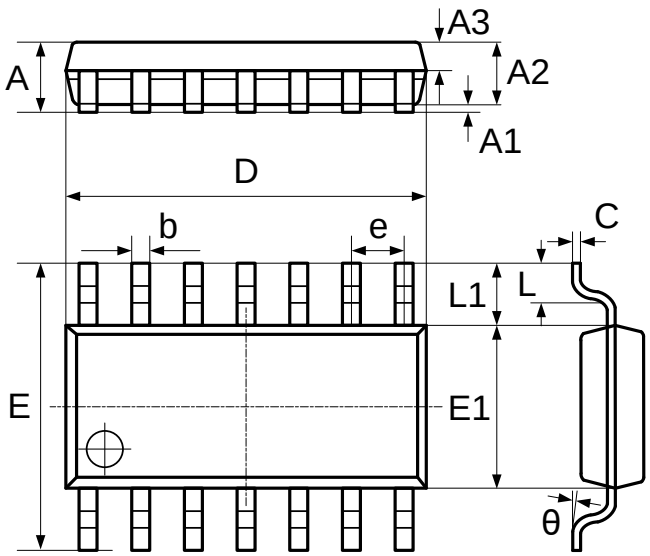
Symbol	Millimeters		
	Min.	Nom.	Max.
A	0.70	0.75	0.80
A1	-	0.02	0.05
b	0.20	0.25	0.30
b1		0.18 REF	
c	0.18	0.20	0.25
D	1.90	2.00	2.10
D1	1.10	1.20	1.30
Nd		1.50BSC	
E	1.90	2.00	2.10
E1	0.60	0.70	0.80
e		0.50BSC	
L	0.30	0.35	0.40
h	0.15	0.20	0.25

RECOMMENDED SOLDERING FOOTPRINT, DFN2x2-8L



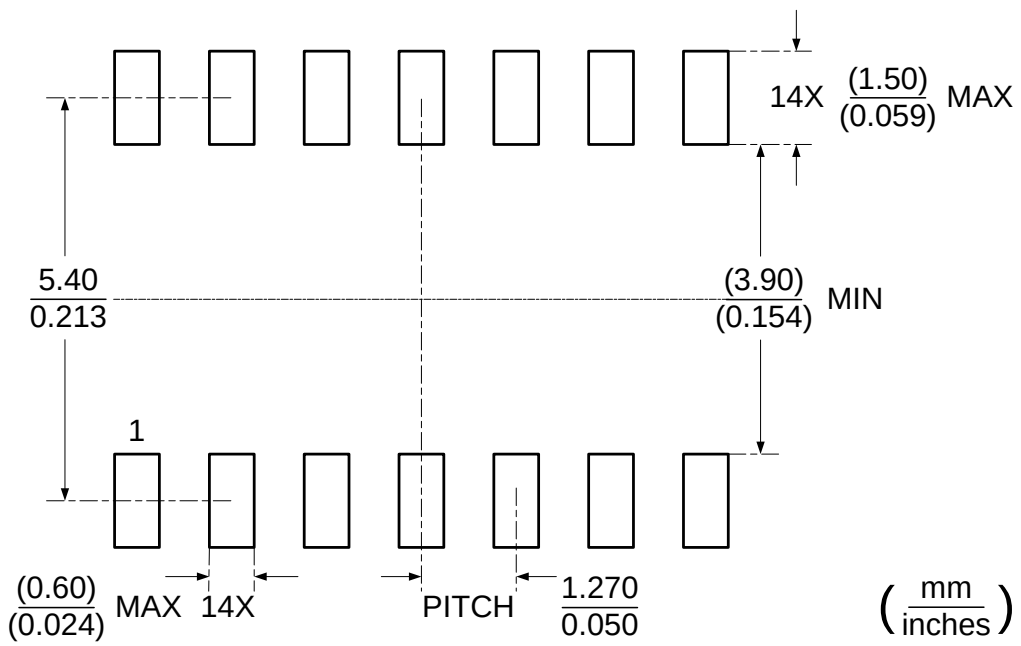
Package Outlines (continued)

DIMENSIONS, SOIC-14L



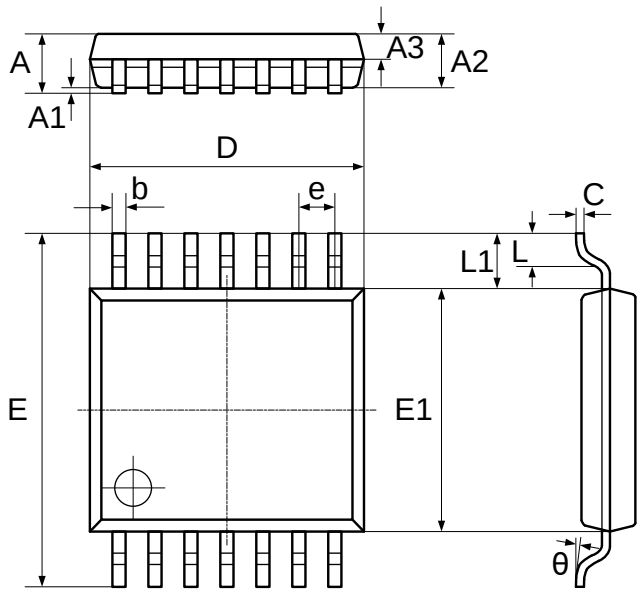
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.450	1.850	0.057	0.073
A1	0.100	0.300	0.004	0.012
A2	1.350	1.550	0.053	0.061
A3	0.550	0.750	0.022	0.030
b	0.406 TYP.		0.016 TYP.	
C	0.203 TYP.		0.008 TYP.	
D	8.630	8.830	0.340	0.348
E	5.840	6.240	0.230	0.246
E1	3.850	4.050	0.152	0.159
e	1.270 TYP.		0.050 TYP.	
L1	1.040 REF.		0.041 REF.	
L	0.350	0.750	0.014	0.030
θ	2°	8°	2°	8°

RECOMMENDED SOLDERING FOOTPRINT, SOIC-14L



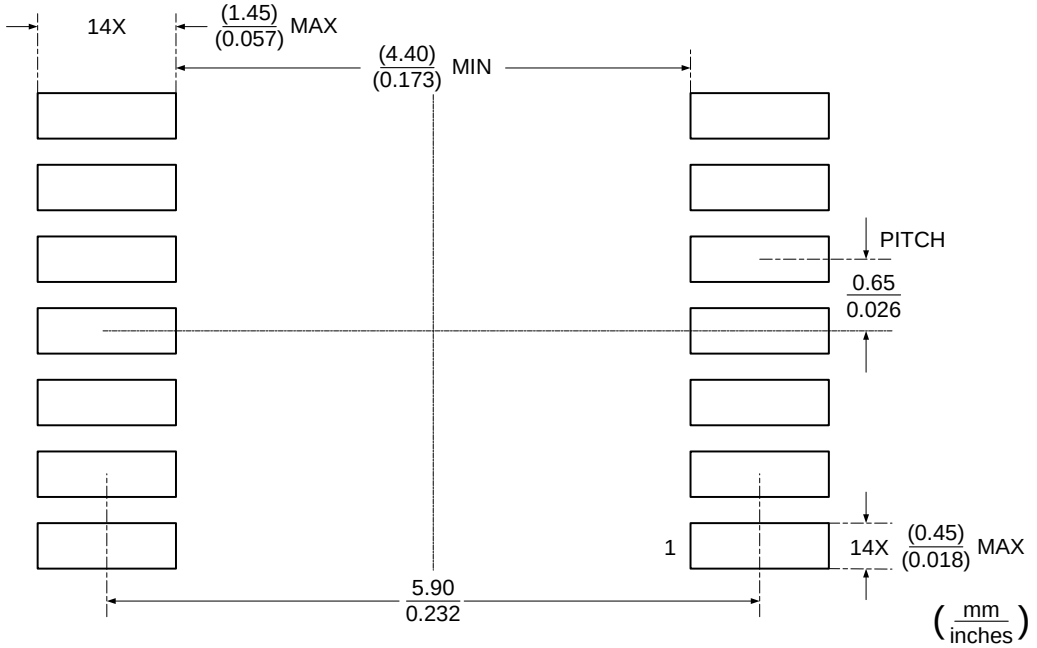
Package Outlines (continued)

DIMENSIONS, TSSOP-14L



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	-	1.200	-	0.047
A1	0.050	0.150	0.002	0.006
A2	0.900	1.050	0.035	0.041
A3	0.390	0.490	0.015	0.019
b	0.200	0.290	0.008	0.011
C	0.130	0.180	0.005	0.007
D	4.860	5.060	0.191	0.199
E	6.200	6.600	0.244	0.260
E1	4.300	4.500	0.169	0.177
e	0.650 TYP.		0.026 TYP.	
L1	1.000 REF.		0.039 REF.	
L	0.450	0.750	0.018	0.030
θ	0°	8°	0°	8°

RECOMMENDED SOLDERING FOOTPRINT, TSSOP-14L



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