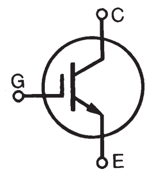
IXYS

Advance Technical Information

High Voltage IGBT

IXGR6N170A

(Electrically Isolated Tab)

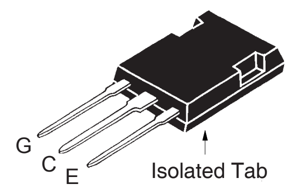


V_{CES} = 1700V
I_{C25} = 5.5A
$V_{CE(sat)}$ ≤ 7.0V
$t_{fi(typ)}$ = 32ns

Symbol	Test Conditions	Maximum Ratings	
V_{CES}	T_C = 25°C to 150°C	1700	V
V_{CGR}	T_J = 25°C to 150°C, R_{GE} = 1MΩ	1700	V
V_{GES}	Continuous	± 20	V
V_{GEM}	Transient	± 30	V
I_{C25}	T_C = 25°C	5.5	A
I_{C110}	T_C = 110°C	2.5	A
I_{CM}	T_C = 25°C, 1ms	18	A
SSOA (RBSOA)	V_{GE} = 15V, T_{VJ} = 125°C, R_G = 33Ω Clamped Inductive Load	I_{CM} = 12 @ 0.8 • V_{CES}	A
t_{SC}	T_J = 125°C, V_{CE} = 1200 V, V_{GE} = 15 V, R_G = 33Ω	10	µs
P_C	T_C = 25°C	50	W
T_J		- 55 ... +150	°C
T_{JM}		150	°C
T_{stg}		- 55 ... +150	°C
V_{ISOL}	50/60 Hz, RMS, t = 1minute I_{ISOL} < 1mA t = 20 seconds	2500 3000	V~ V~
F_C	Mounting Force	20..120/4.5..27	N/lb
T_L	Maximum Lead Temperature for Soldering	300	°C
T_{SOLD}	1.6mm (0.062 in.) from Case for 10s	260	°C
Weight		5	g

Symbol	Test Conditions (T_J = 25°C Unless Otherwise Specified)	Characteristic Values Min.	Typ.	Max.	
BV_{CES}	I_C = 250µA, V_{GE} = 0V	1700			V
$V_{GE(th)}$	I_C = 250µA, V_{CE} = V_{GE}	3.0		5.0	V
I_{CES}	V_{CE} = 0.8 • V_{CES}, V_{GE} = 0V Note 2, T_J = 125°C			10 500	µA µA
I_{GES}	V_{CE} = 0V, V_{GE} = ± 20V			±100	nA
$V_{CE(sat)}$	I_C = 3A, V_{GE} = 15V, Note 1 T_J = 125°C		 5.4	7.0	V V

ISOPLUS247™



G = Gate C = Collector
E = Emitter

Features

- Silicon Chip on Direct-Copper Bond (DCB) Substrate
- Isolated Mounting Surface
- 2500V~ Electrical Isolation

Advantages

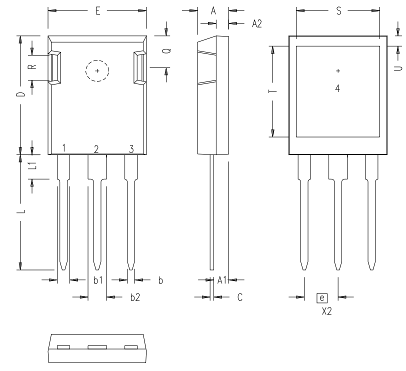
- High Power Density
- Low Gate Drive Requirement

Applications

- Power Inverters
- UPS
- Motor Drives
- SMPS
- PFC Circuits
- Welding Machines

Symbol	Test Conditions (T_J = 25°C, Unless Otherwise Specified)	Characteristic Values Min.	Typ.	Max.	
g_{fs}	I_C = 6A, V_{CE} = 20V, Note 1	2.0	3.5		S
C_{ies}	V_{CE} = 25V, V_{GE} = 0V, f = 1MHz		390		pF
C_{oes}			20		pF
C_{res}			7		pF
Q_g	I_C = 6A, V_{GE} = 15V, V_{CE} = 0.5 • V_{CES}		18.5		nC
Q_{ge}			2.8		nC
Q_{gc}			8.2		nC
$t_{d(on)}$	**Inductive load, T_J = 25°C**		46		ns
t_{ri}	I_C = 6A, V_{GE} = 15V		40		ns
E_{on}	V_{CE} = 0.5 • V_{CES}, R_G = 33Ω		0.59		mJ
$t_{d(off)}$	Note 3		220	400	ns
t_{fi}			32	65	ns
E_{off}			0.18	0.36	mJ
$t_{d(on)}$	**Inductive load, T_J = 125°C**		48		ns
t_{ri}	I_C = 6A, V_{GE} = 15V		43		ns
E_{on}	V_{CE} = 0.5 • V_{CES}, R_G = 33Ω		0.62		mJ
$t_{d(off)}$	Note 3		230		ns
t_{fi}			41		ns
E_{off}			0.25		mJ
R_{thJC}				2.5	°C/W
R_{thCK}			0.15		°C/W

ISOPLUS247 (IXGR) Outline



SYM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.190	.205	4.83	5.21
A1	.090	.100	2.29	2.54
A2	.075	.085	1.91	2.16
b	.045	.055	1.14	1.40
b1	.075	.084	1.91	2.13
b2	.115	.123	2.92	3.12
C	.024	.031	0.61	0.80
D	.819	.840	20.80	21.34
E	.620	.635	15.75	16.13
e	.215 BSC		5.45 BSC	
L	.780	.800	19.81	20.32
L1	.150	.170	3.81	4.32
Q	.220	.244	5.59	6.20
R	.170	.190	4.32	4.83
S	.520	.540	13.21	13.72
T	.620	.640	15.75	16.26
U	.065	.080	1.65	2.03

1 – GATE
2 – DRAIN (COLLECTOR)
3 – SOURCE (EMITTER)
4 – NO CONNECTION

NOTE: This drawing will meet all dimensions requirement of JEDEC outline TO-247AD except screw hole.

Notes:

1. Pulse test, t ≤ 300μs, duty cycle, d ≤ 2%.
2. Part must be heatsunk for high-temp Ices measurement.
3. Switching times & energy losses may increase for higher V_{CE}(Clamp), T_J or R_G.

ADVANCE TECHNICAL INFORMATION

The product presented herein is under development. The Technical Specifications offered are derived from a subjective evaluation of the design, based upon prior knowledge and experience, and constitute a "considered reflection" of the anticipated result. IXYS reserves the right to change limits, test conditions, and dimensions without notice.

Fig. 1. Output Characteristics @ T_J = 25ºC

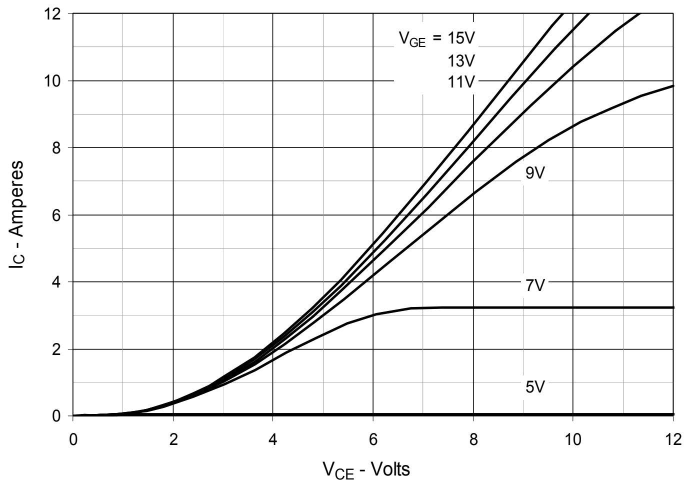


Fig. 2. Extended Output Characteristics @ T_J = 25ºC

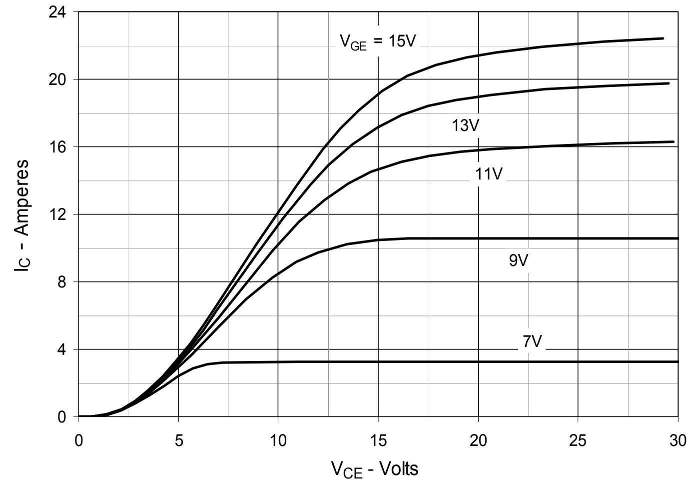


Fig. 3. Output Characteristics @ T_J = 125ºC

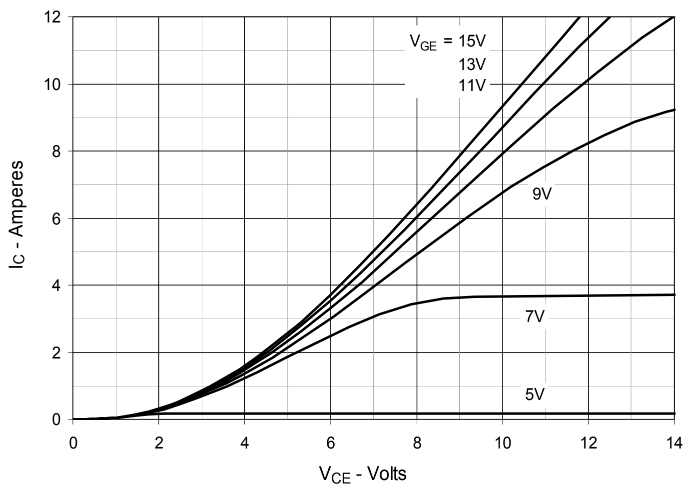


Fig. 4. Dependence of $V_{CE(sat)}$ on Junction Temperature

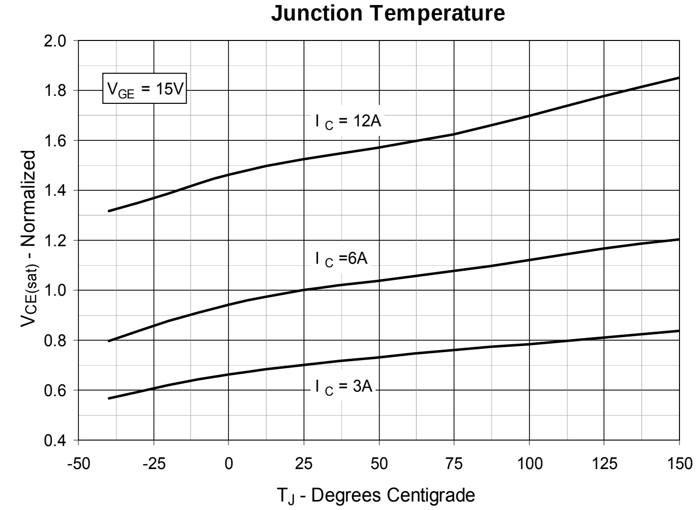


Fig. 5. Collector-to-Emitter Voltage vs. Gate-to-Emitter Voltage

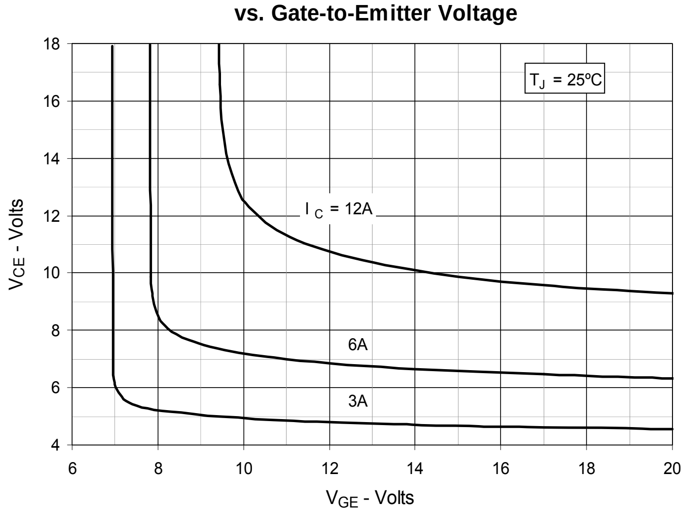


Fig. 6. Input Admittance

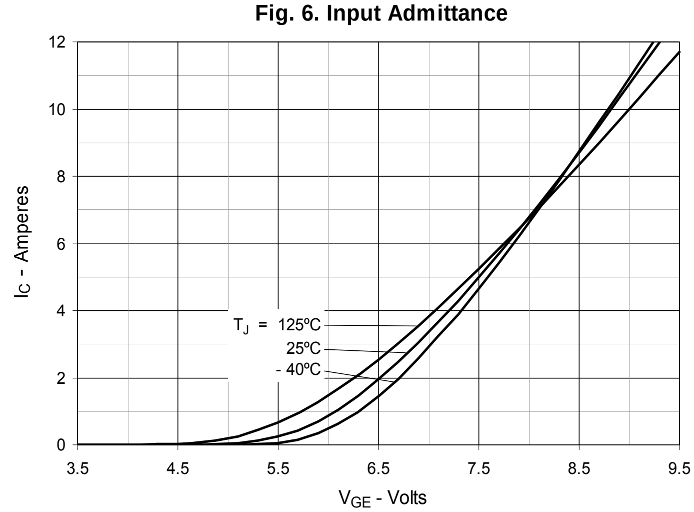


Fig. 7. Transconductance

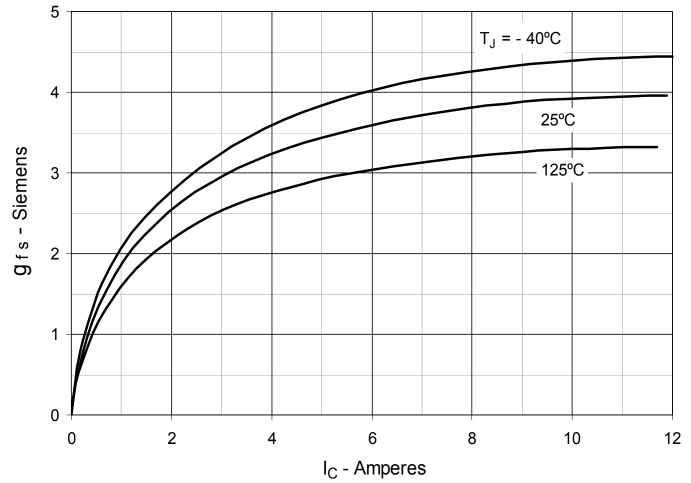


Fig. 8. Gate Charge

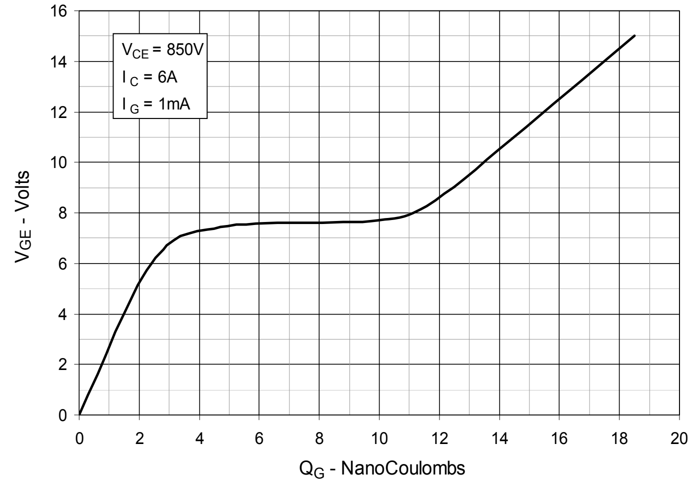


Fig. 9. Reverse-Bias Safe Operating Area

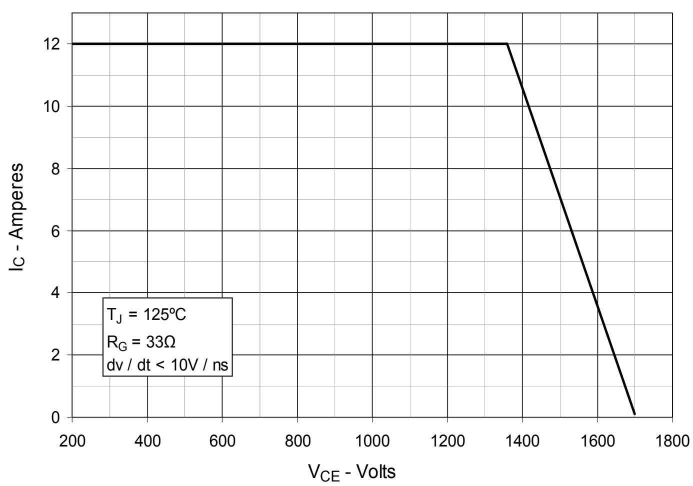


Fig. 10. Capacitance

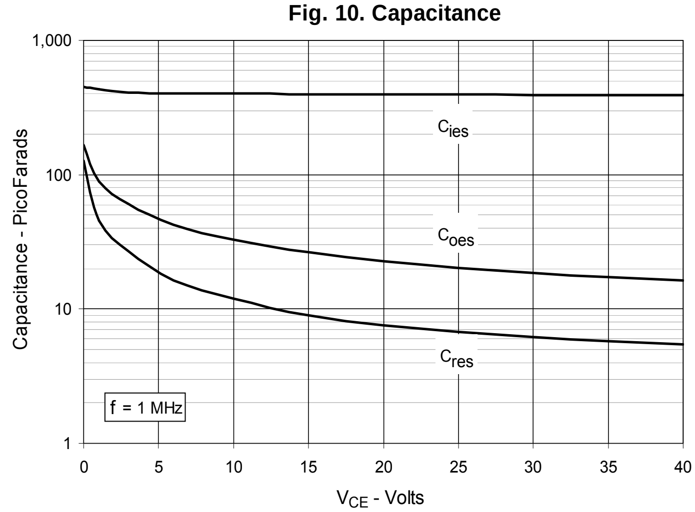
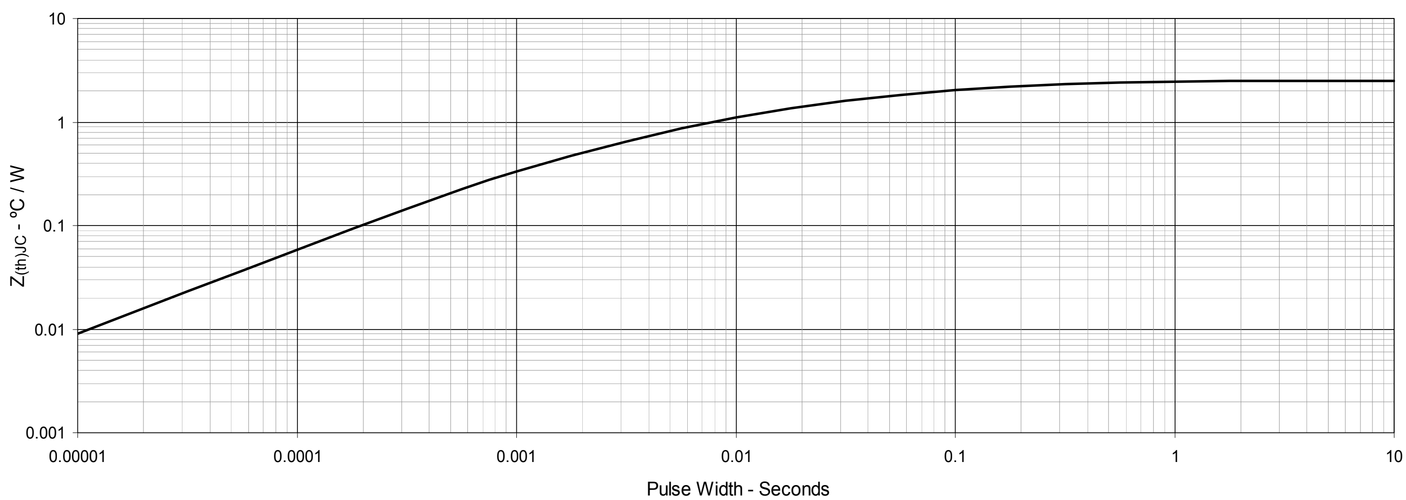


Fig. 11. Maximum Transient Thermal Impedance



IXYS Reserves the Right to Change Limits, Test Conditions, and Dimensions.

Fig. 12. Inductive Switching Energy Loss vs. Gate Resistance

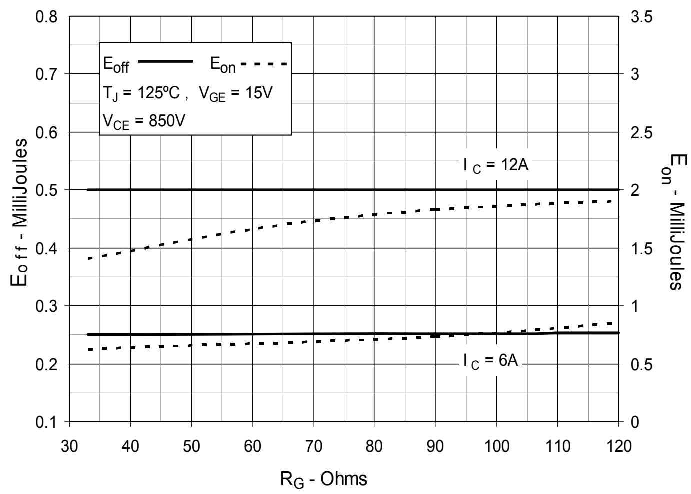


Fig. 13. Inductive Switching Energy Loss vs. Collector Current

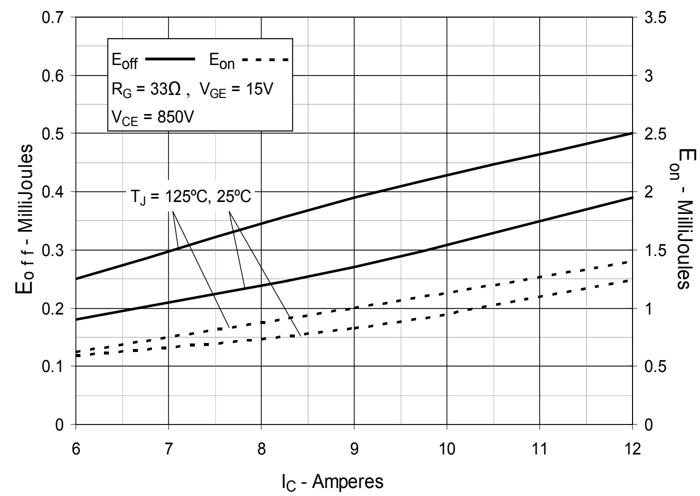
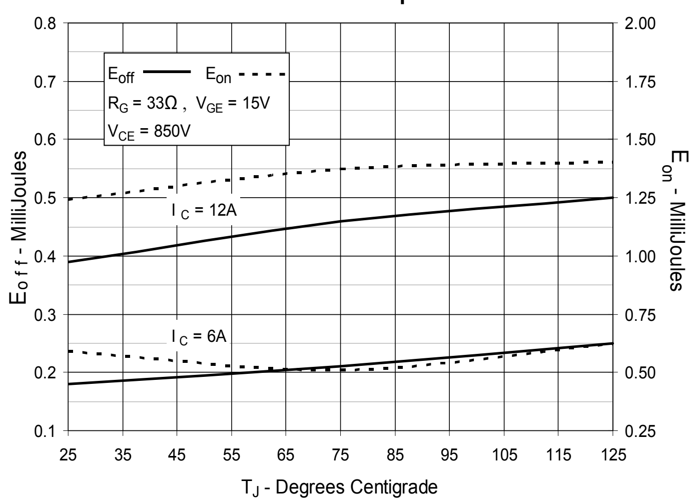


Fig. 14. Inductive Switching Energy Loss vs. Junction Temperature



IXYS
A Littelfuse Technology

单击下面可查看定价，库存，交付和生命周期等信息

>>Littelfuse(美国力特)