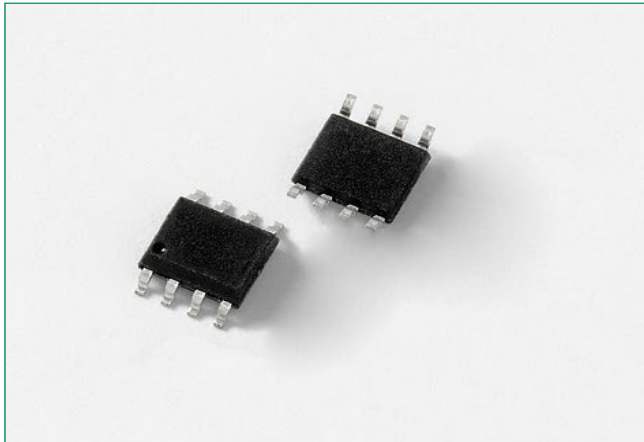
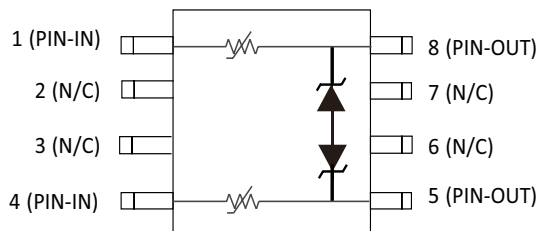


SP4031 Series



Functional Block Diagram



Features

- ESD, IEC 61000-4-2, ±30kV contact, ±30kV air
- EFT, IEC 61000-4-4, 40A (5/50ns)
- Lightning, 35A (8/20 as defined in IEC 61000-4-5 2nd edition)
- Low capacitance of 2.5pF (@V_R=0V)
- Moisture Sensitivity Level (MSL -1)
- Lead free and RoHS compliant
- This SP4031 hybrid component provides a tested and proved protection solution for high-speed interfaces such as 10/100/1000BaseT applications
- Low parasitic capacitance
- Low operating voltage (<3.3 V)
- Low breakdown voltage (>3.5V)

Description

The SP4031 hybrid protector offers both overcurrent and differential only overvoltage protection for applications such as 10/100/1000BaseT ports. Compliant with the newest standards of overvoltage per industry standard ITU-T K.21. Tested to basic tests levels 2.5kV overvoltage. Flow-through package layout allows PCB trace routing directly through the SP4031 without changing pitch dimensions, thus having less impact on normal signal high frequency components.

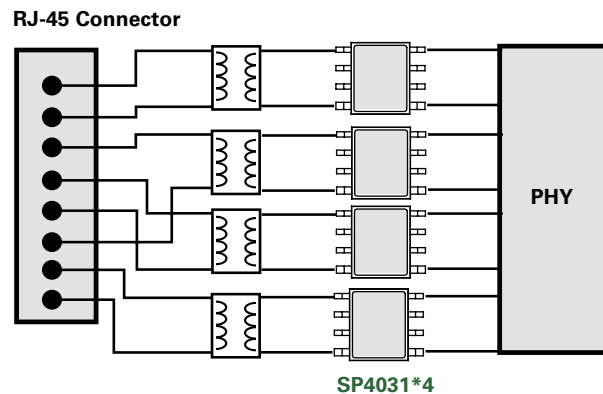
During a prolonged overvoltage event such as a power fault, this component will present a high impedance. The high impedance state will reset once the power fault event has ended. During a fast transient event, the component will clamp, thus protecting any downstream chipsets.

These components can safely absorb up to 35A per IEC 61000-4-5 2nd edition (t_p=8/20µs) without performance degradation and a minimum ±30kV ESD per IEC 61000-4-2 International Standard. The low loading capacitance and high surge capability makes the SP4031 ideal for protecting telecommunication ports such as Ethernet and other high speed data interfaces.

Applications

- 10/100/1000BaseT Ethernet
- ITU K.21 Basic level compliance
- ADSL/VDSL/G.fast modem
- Industrial Ethernet

Application Example



Life Support Note:

Not Intended for Use in Life Support or Life Saving Applications

The products shown herein are not designed for use in life sustaining or life saving applications unless otherwise expressly indicated.

Absolute Maximum Ratings

Symbol	Parameter	Value	Units
T _{OP}	Operating Temperature	-40 to 85	°C
I _{PP}	Peak Current (t _p =8/20μs)	35	A
T _{STOR}	Storage Temperature	-55 to 85	°C

Notes:

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the component. This is a stress only rating and operation of the component at these or any other conditions above those indicated in the operational sections of this specification is not implied.

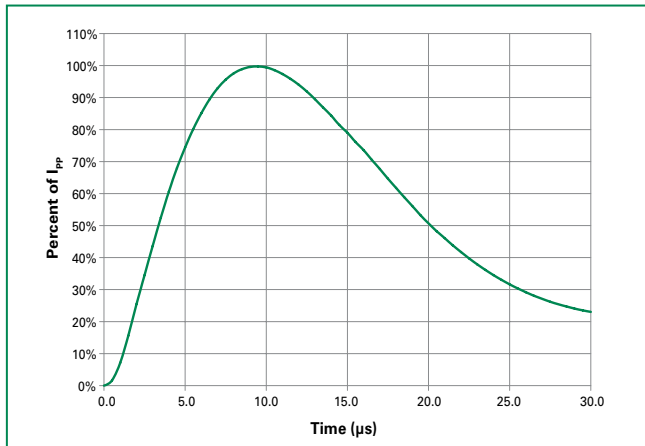
Electrical Characteristics, Pin1 to Pin5 (T_{OP} = 25°C)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Reverse Standoff Voltage	V _{RWM}	I _R = 1μA			3.3	V
Breakdown Voltage	V _{BR}	I _R = 1mA	3.5	4.5		V
Reverse Leakage Current	I _{LEAK}	V _R = 3.3V			0.5	μA
Clamp Voltage ¹	V _C	I _{PP} = 1A, t _p = 8/20μs, Pin5 to Pin8		6	7.5	V
		I _{PP} = 35A, t _p = 8/20μs, Pin5 to Pin8		29.5	35	V
Dynamic Resistance ²	R _{DYN}	TLP, t _p = 100ns, Pin5 to Pin8		0.45		Ω
ESD Withstand Voltage ¹	V _{ESD}	IEC 61000-4-2 (Contact Discharge)	±30			kV
		IEC 61000-4-2 (Air Discharge)	±30			kV
Diode Capacitance ¹	C _{V(O-I/O)}	Reverse Bias=0V, f=1MHz		2	2.5	pF

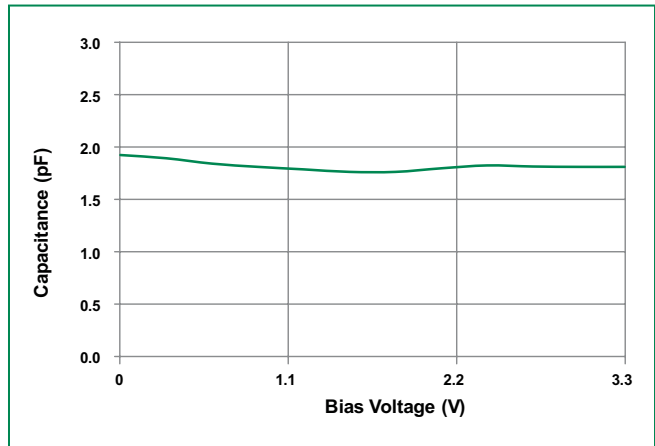
Notes: 1 Parameter is guaranteed by design and/or component characterization.

2. Transmission Line Pulse (TLP) with 100ns width, 2ns rise time, and average window t1=70ns to t2= 90ns

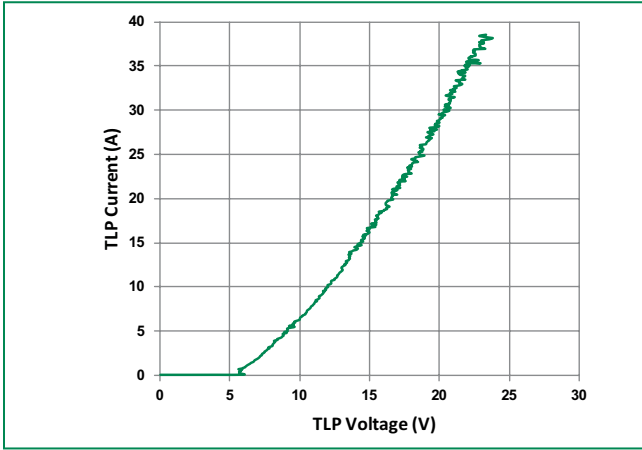
8/20 Pulse Waveform



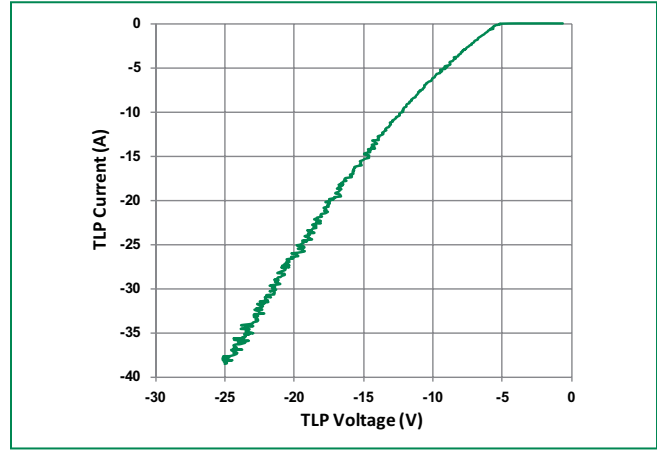
Capacitance vs. Reverse Bias



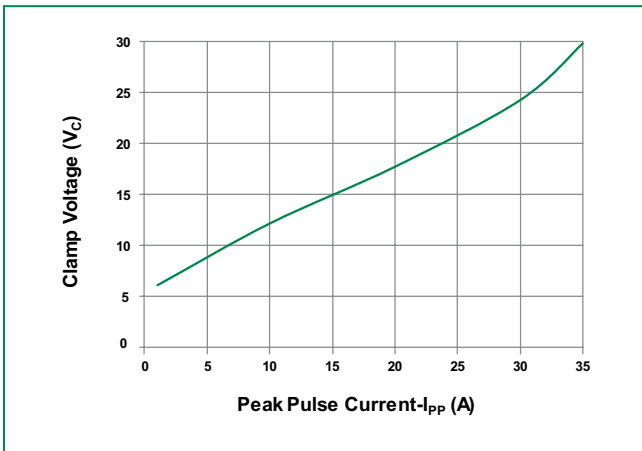
Positive Transmission Line Pulsing (TLP) Plot



Negative Transmission Line Pulsing (TLP) Plot

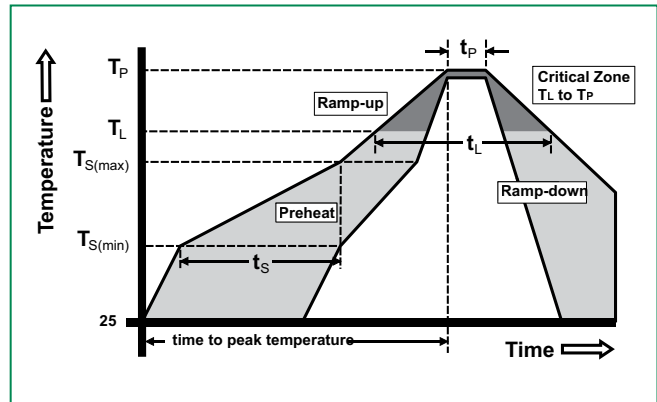


Clamping voltage vs. I_{pp} for 8/20 μ S waveshape



Soldering Parameters

Reflow Condition		Pb – Free assembly
Pre Heat	- Temperature Min ($T_{s(min)}$)	150°C
	- Temperature Max ($T_{s(max)}$)	200°C
	- Time (min to max) (t_s)	60 – 180 secs
Average ramp up rate (Liquidus) Temp (T_L) to peak		3°C/second max
$T_{s(max)}$ to T_L - Ramp-up Rate		3°C/second max
Reflow	- Temperature (T_L) (Liquidus)	217°C
	- Temperature (t_L)	60 – 150 seconds
Peak Temperature (T_p)		260 ^{+0/-5} °C
Time within 5°C of actual peak Temperature (t_p)		20 – 40 seconds
Ramp-down Rate		6°C/second max
Time 25°C to peak Temperature (T_p)		8 minutes Max.
Do not exceed		260°C



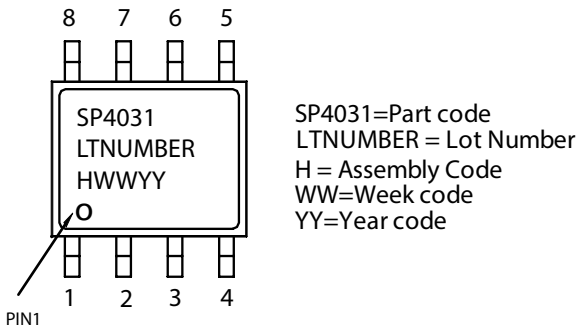
Product Characteristics

Lead Plating	Pre-Plated Frame
Lead Material	Copper Alloy
Lead Coplanarity	0.004 inches(0.102mm)
Substrate Material	Silicon
Body Material	Molded Compound
Flammability	UL Recognized compound meeting flammability rating V-0

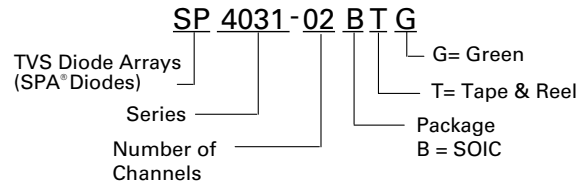
Ordering Information

Part Number	Package	Min. Order Qty.
SP4031-02BTG	SOIC Tape & Reel	2500

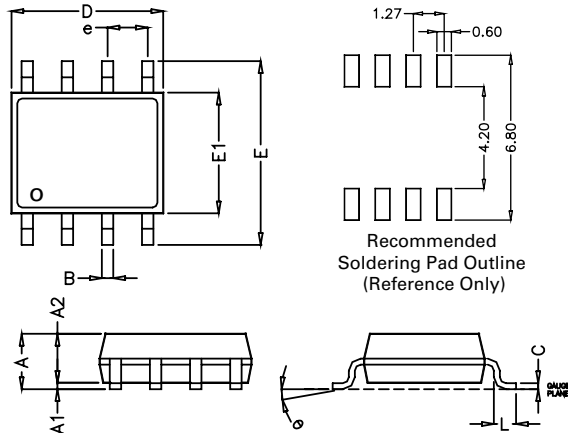
Part Marking System



Part Numbering System

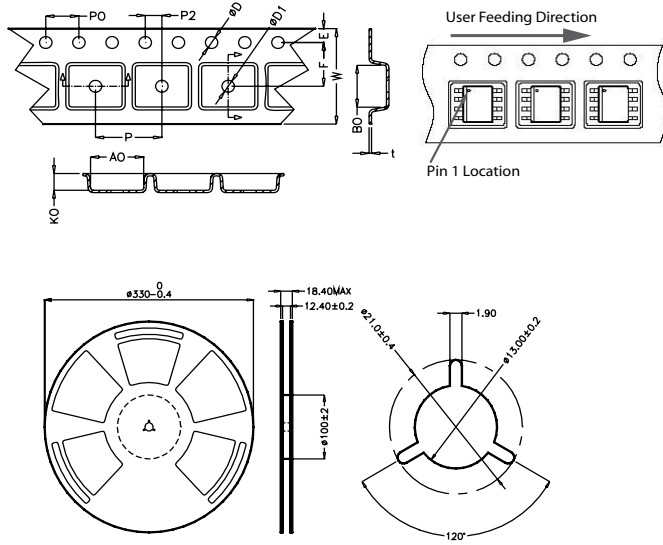


Package Dimensions of SOIC-8



Package	SOIC			
Pins	8			
JEDEC	MS-012			
	Millimeters		Inches	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
A2	1.25	1.65	0.050	0.065
B	0.31	0.51	0.012	0.020
c	0.17	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
L	0.40	1.27	0.016	0.050

Embossed Carrier Tape & Reel Specification – SOIC Package



	Millimeters		Inches	
	Min	Max	Min	Max
E	1.65	1.85	0.065	0.073
F	5.4	5.6	0.213	0.22
P2	1.95	2.05	0.077	0.081
D	1.5	1.6	0.059	0.063
D1	1.50 Min		0.059 Min	
P0	3.9	4.1	0.154	0.161
10P0	40.0 +/- 0.20		1.574 +/- 0.008	
W	11.9	12.1	0.468	0.476
P	7.9	8.1	0.311	0.319
A0	6.3	6.5	0.248	0.256
B0	5.1	5.3	0.2	0.209
K0	2	2.2	0.079	0.087
t	0.30 +/- 0.05		0.012 +/- 0.002	

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Revision: 02/28/19

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