

# Standard Power MOSFET

## IXTH 16P20

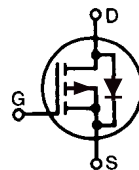
P-Channel Enhancement Mode  
Avalanche Rated

$$V_{DSS} = -200 \text{ V}$$

$$I_{D25} = -16 \text{ A}$$

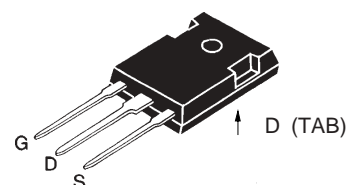
$$R_{DS(on)} = 0.16 \text{ } \Omega$$

### Preliminary Data Sheet



Symbol	Test Conditions	Maximum Ratings	
$V_{DSS}$	$T_J = 25^\circ\text{C}$ to $150^\circ\text{C}$	-200	V
$V_{DGR}$	$T_J = 25^\circ\text{C}$ to $150^\circ\text{C}$ ; $R_{GS} = 1 \text{ M}\Omega$	-200	V
$V_{GS}$	Continuous	$\pm 20$	V
$V_{GSM}$	Transient	$\pm 30$	V
$I_{D25}$	$T_C = 25^\circ\text{C}$	-16	A
$I_{DM}$	$T_C = 25^\circ\text{C}$ , pulse width limited by $T_J$	-64	A
$I_{AR}$	$T_C = 25^\circ\text{C}$	-16	A
$E_{AR}$	$T_C = 25^\circ\text{C}$	30	mJ
$P_D$	$T_C = 25^\circ\text{C}$	300	W
$T_J$		-55 ... +150	$^\circ\text{C}$
$T_{JM}$		150	$^\circ\text{C}$
$T_{stg}$		-55 ... +150	$^\circ\text{C}$
$T_L$	Maximum lead temperature for soldering 1.6 mm (0.062 in.) from case for 10 s	300	$^\circ\text{C}$
$M_d$	Mounting torque	1.13/10	Nm/lb.in.
<b>Weight</b>		6	g

TO-247 AD



G = Gate, D = Drain,  
S = Source, TAB = Drain

### Features

- International standard package JEDEC TO-247 AD
- Low  $R_{DS(on)}$  HDMOS™ process
- Rugged polysilicon gate cell structure
- Unclamped Inductive Switching (UIS) rated
- Low package inductance (<5 nH)  
- easy to drive and to protect

### Applications

- High side switching
- Push-pull amplifiers
- DC choppers
- Automatic test equipment

### Advantages

- Easy to mount with 1 screw (isolated mounting screw hole)
- Space savings
- High power density

Symbol	Test Conditions	Characteristic Values ( $T_J = 25^\circ\text{C}$ , unless otherwise specified)		
		min.	typ.	max.
$V_{DSS}$	$V_{GS} = 0 \text{ V}$ , $I_D = -250 \text{ } \mu\text{A}$	-200		V
$V_{GS(th)}$	$V_{DS} = V_{GS}$ , $I_D = -250 \text{ } \mu\text{A}$	-3.0		V
$I_{GSS}$	$V_{GS} = \pm 20 \text{ V}_{DC}$ , $V_{DS} = 0$			$\pm 100 \text{ nA}$
$I_{DSS}$	$V_{DS} = 0.8 \cdot V_{DSS}$ $V_{GS} = 0 \text{ V}$			$-25 \text{ } \mu\text{A}$ $-1 \text{ mA}$
$R_{DS(on)}$	$V_{GS} = -10 \text{ V}$ , $I_D = 0.5 \cdot I_{D25}$			0.16 $\Omega$

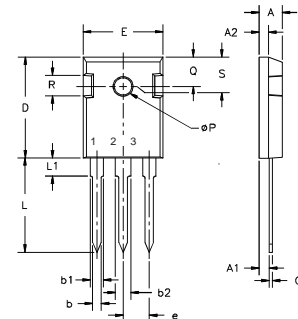
Symbol	Test Conditions	Characteristic Values ( $T_J = 25^\circ\text{C}$ , unless otherwise specified)		
		min.	typ.	max.
$g_{fs}$	$V_{DS} = -10\text{ V}$ ; $I_D = I_{D25}$ , pulse test	6	10	S
$C_{iss}$	$V_{GS} = 0\text{ V}$ , $V_{DS} = -25\text{ V}$ , $f = 1\text{ MHz}$		2800	pF
$C_{oss}$			550	pF
$C_{rss}$			240	pF
$t_{d(on)}$	$V_{GS} = -10\text{ V}$ , $V_{DS} = 0.5 V_{DSS}$ , $I_D = 0.5 I_{D25}$ $R_G = 4.7\ \Omega$ (External)		33	ns
$t_r$			26	ns
$t_{d(off)}$			65	ns
$t_f$			25	ns
$Q_{g(on)}$	$V_{GS} = -10\text{ V}$ , $V_{DS} = 0.5 V_{DSS}$ , $I_D = 0.5 I_{D25}$		95	nC
$Q_{gs}$			27	nC
$Q_{gd}$			40	nC
$R_{thJC}$			0.42	K/W
$R_{thCS}$		0.25		K/W

### Source-Drain Diode

Characteristic Values  
( $T_J = 25^\circ\text{C}$ , unless otherwise specified)

Symbol	Test Conditions	min.	typ.	max.
$I_S$	$V_{GS} = 0$			-16 A
$I_{SM}$	Repetitive; pulse width limited by $T_{JM}$			-64 A
$V_{SD}$	$I_F = I_S$ , $V_{GS} = 0\text{ V}$ , Pulse test, $t \leq 300\ \mu\text{s}$ , duty cycle $d \leq 2\%$			-3 V
$t_{rr}$	$I_F = I_S$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_R = -50\text{ V}$		250	ns

### TO-247 AD Outline



Terminals: 1 - Gate 2 - Drain  
3 - Source Tab - Drain

Dim.	Millimeter		Inches	
	Min.	Max.	Min.	Max.
A	4.7	5.3	.185	.209
A <sub>1</sub>	2.2	2.54	.087	.102
A <sub>2</sub>	2.2	2.6	.059	.098
b	1.0	1.4	.040	.055
b <sub>1</sub>	1.65	2.13	.065	.084
b <sub>2</sub>	2.87	3.12	.113	.123
C	.4	.8	.016	.031
D	20.80	21.46	.819	.845
E	15.75	16.26	.610	.640
e	5.20	5.72	0.205	0.225
L	19.81	20.32	.780	.800
L1		4.50		.177
ØP	3.55	3.65	.140	.144
Q	5.89	6.40	0.232	0.252
R	4.32	5.49	.170	.216
S	6.15	BSC	.242	BSC

IXYS reserves the right to change limits, test conditions, and dimensions.

IXYS MOSFETs and IGBTs are covered by one or more of the following U.S. patents: 4,835,592 4,881,106 5,017,508 5,049,961 5,187,117 5,486,715 6,306,728B1 6,259,123B1 6,306,728B1 4,850,072 4,931,844 5,034,796 5,063,307 5,237,481 5,381,025 6,404,065B1 6,162,665 6,534,343 6,583,505



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