1.5MHZ,1500mA,Duty 100%,High Efficiency Synchronous PWM Step-down DC/DC Convert With Soft-start

General Description

The LP3208 is a constant frequency, current mode, PWM step-down converter. The device integrates a main switch and a synchronous rectifier for high efficiency. The 2.5V to 5.5V input voltage range makes the LP3208 is ideally suited for portable electronic devices that are powered from 1-cell Li-ion battery or from other power sources within the range such as cellular phones, PDAs and handy-terminals. Internal synchronous rectifier with low RDS(ON) dramatically reduces conduction loss at PWM mode.

The internal synchronous switch increases efficiency while eliminate the need for an external Schottky diode. The switching ripple is easily smoothed-out by small package filtering elements due to a fixed operation frequency of 1.5MHz. This along with small SOT-23-5 package provides small PCB area application. Other features include soft start, lower internal reference voltage with 2% accuracy, over temperature protection, and over current protection.

Features

- High Efficiency: 96%
- 1.5MHz Fixed-Frequency PWM Operation
- Adjustable Output From 0.6V to VIN
- 1.2V, 1.8V, 2.5V, 2.8V and 3.3V Fixed
- 1.0A Output Curre nt, 1.5A Peak Current
- No Schottky Diode Required
- 100% Duty Cycle Low Dropout Operation
- Available in SOT23-5/TSOT23-5 Package
- Short Circuit and Thermal Protection
- Over Voltage Protection
- Low than 1μA Shutdown Current

Applications

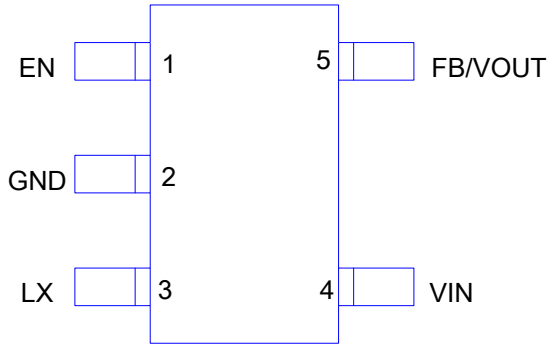
- Portable Media Players/MP3 players
- Cellular and Smart mobile phone
- PDA
- DSC
- Wireless Card

Ordering Information

LP3208 □□ □ □

- F: Pb-Free
- Package:
  - B5: SOT23-5
  - J5: TSOT23-5
- Output Voltage Type
  - A: Adjustable type
  - 12: 1.2V
  - 18: 1.8V
  - 25: 2.5V
  - 30: 3.0V

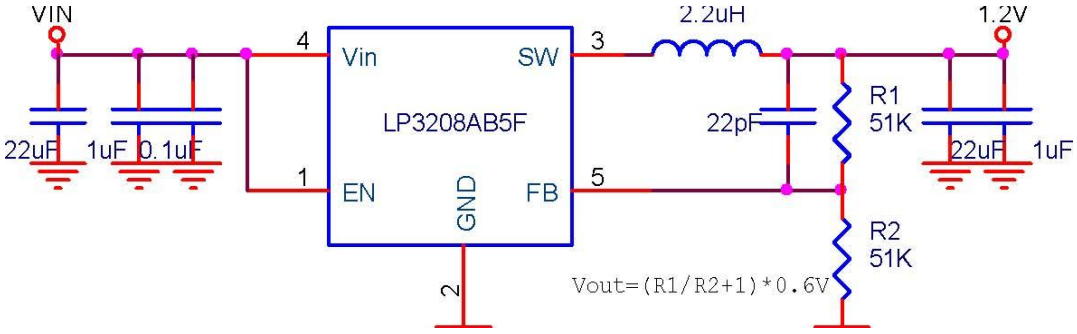
Pin Configurations



Marking information

Device	Marking	Package	Shipping
LP3208		SOT23-5 TSOT23-5	3K/REEL

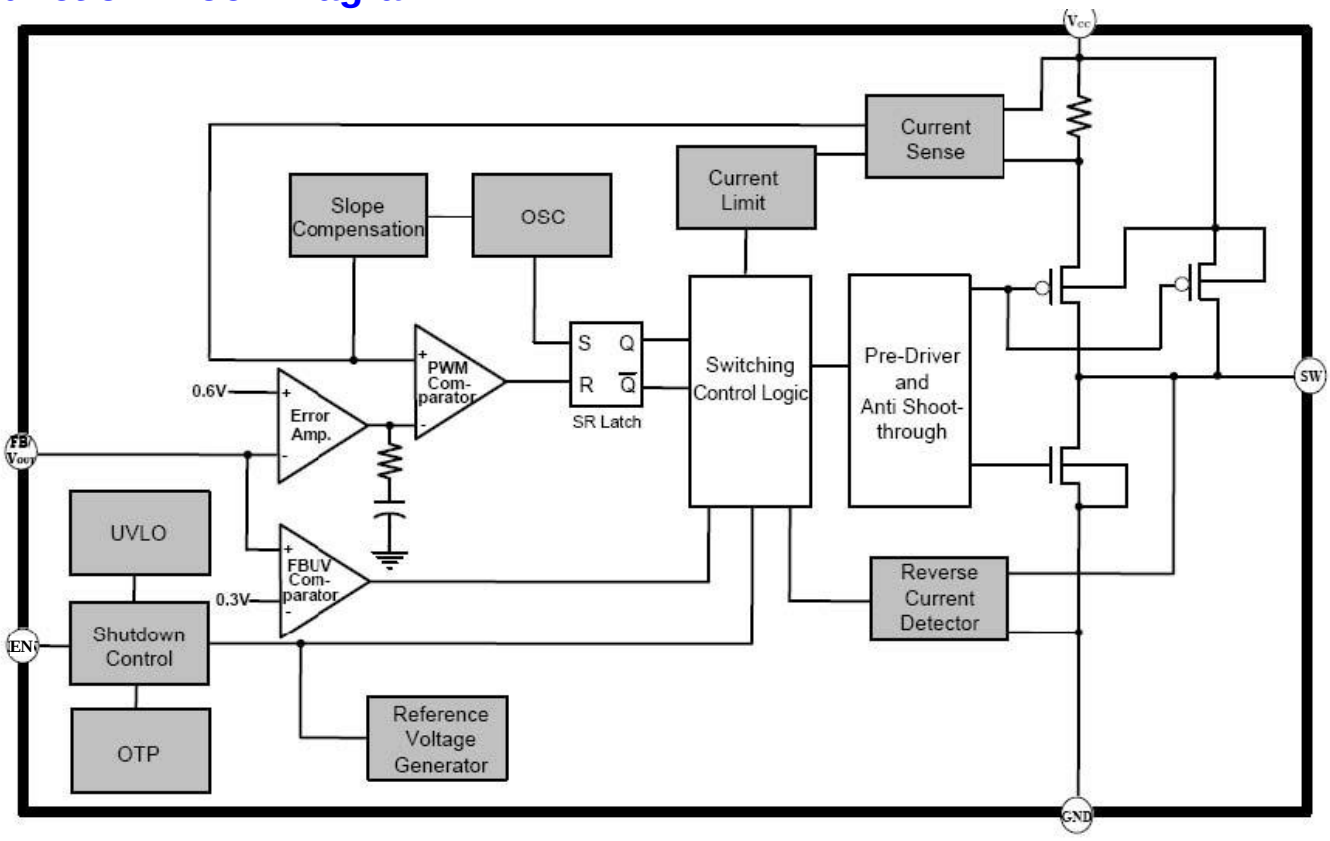
Typical Application Circuit



Functional pin description

Pin Number	Pin Name	Pin Function
1	EN	Chip Enable (Active High)
2	GND	Ground
3	LX	Pin for switching
4	VIN	Power Input
5	FB/VOUT	Feedback Input Pin, Reference voltage is 0.6 V

Function Block Diagram



Absolute Maximum Ratings

Supply Input Voltage----------−0.3V to 6.0V

Peak SW Sink and Source Current----------1.5A

Junction Temperature ----------125℃

ESD Rating (HBM) ----------2KV

Lead Temperature (Soldering, 10 sec.) ---------- 260°C

Operation Temperature Range ----------−40°C to 85°C

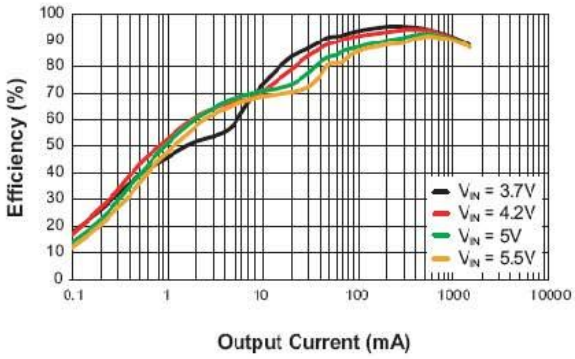
Storage Temperature Range ----------−65°C to 150°C

Electrical Characteristics

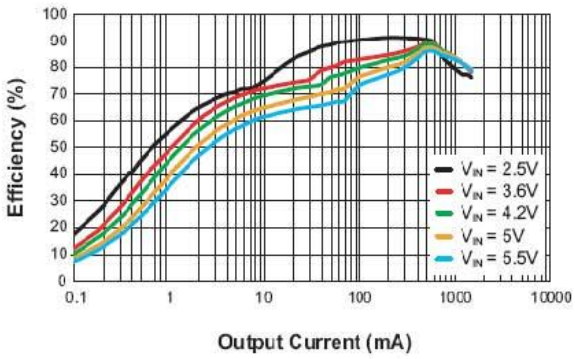
Parameter		Symbol	Test Conditions	Min	Typ	Max	Units
Input Voltage Range		VIN		2.5		5.5	V
Quiescent Current		IQ	IOUT = 0mA, VFB =0.5V IOUT = 0mA, VFB =0.7V		170 25	350 35	uA
Shutdown Current		ISHDN	EN = GND		0.1	1	uA
Reference Voltage		VREF	For adjustable output voltage	0.588	0.6	0.612	V
Adjustable Output Range		VOUT		VREF		VIN − 0.2	V
Output Voltage Accuracy	Fixed	ΔVOUT	VIN = 2.5 to 5.5V, VOUT = 1.2V 0A < IOUT < 600mA	−3		+3	%
		ΔVOUT	VIN = 2.5 to 5.5V, VOUT = 1.5V 0A < IOUT < 600mA	−3		+3	%
		ΔVOUT	VIN = 2.5 to 5.5V, VOUT = 1.8V 0A < IOUT < 600mA	−3		+3	%
		ΔVOUT	VIN = 2.8 to 5.5V, VOUT = 2.5V 0A < IOUT < 600mA	−3		+3	%
		ΔVOUT	VIN = 3.5 to 5.5V, VOUT = 3.3V 0A < IOUT < 600mA	−3		+3	%
	Adjustable	ΔVOUT ΔVOUT	VIN = VOUT + 0.2V to 5.5V, VIN ≧3.5V, 0A < IOUT < 600mA	−3		+3	%
			VIN = VOUT + 0.4V to 5.5V, VIN ≧2.2V, 0A < IOUT < 600mA	−3		+3	%
FB Input Current	IFB	VFB = VIN		-30		30	nA
PMOSFET RON	PRDS(ON)	IOUT = 200mA	VIN = 3.6V		0.15		Ω
NMOSFET RON	NRDS(ON)	IOUT = 200mA	VIN = 3.6V		0.2		Ω
P-Channel Current Limit IP(LM)		VIN =2.5 to 5.5V		1.5			A
EN Threshold	VEN			0.3	1.0	1.5	V
EN Leakage Current	VENL			--	2		uA

Typical Operating Characteristics

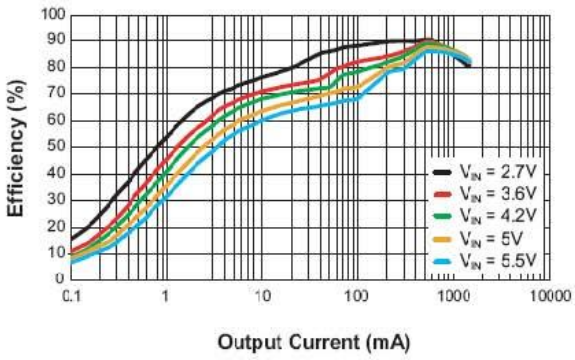
Efficiency vs. Output Current
(V_{OUT} = 3.3V; T_A = 25°C; L = 2.2μH)



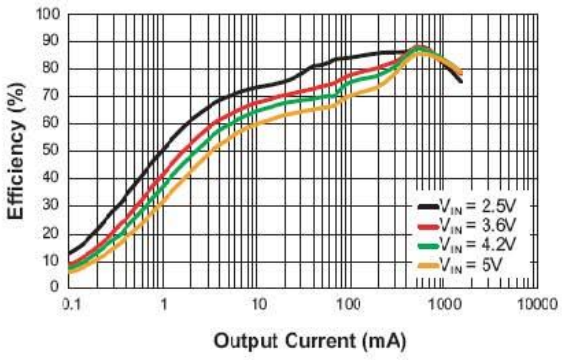
Efficiency vs. Output Current
(V_{OUT} = 1.8V; T_A = 25°C; L = 2.2μH)



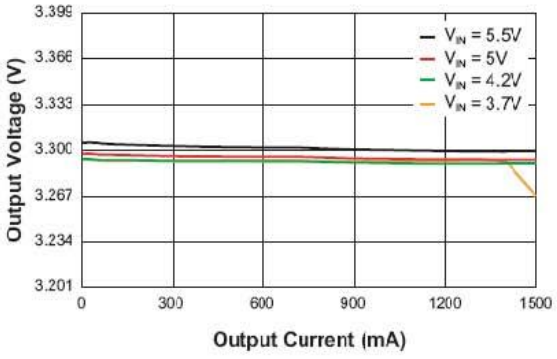
Efficiency vs. Output Current
(V_{OUT} = 1.5V; T_A = 25°C; L = 2.2μH)



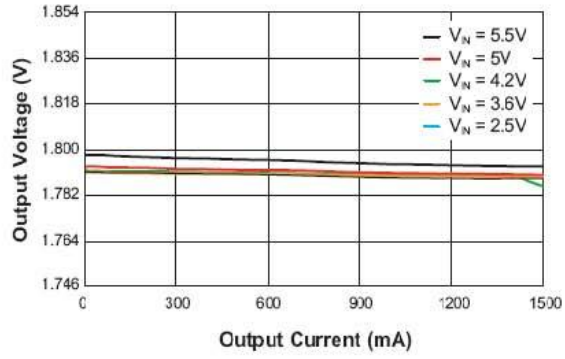
Efficiency vs. Output Current
(V_{OUT} = 1.2V; T_A = 25°C; L = 2.2μH)



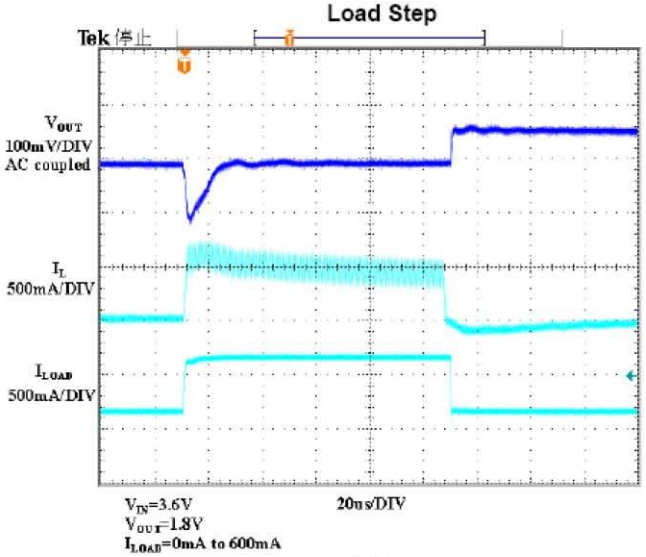
DC Regulation
(V_{OUT} = 3.3V; T_A = 25°C; L = 2.2μH; C_{OUT} = 22μF)



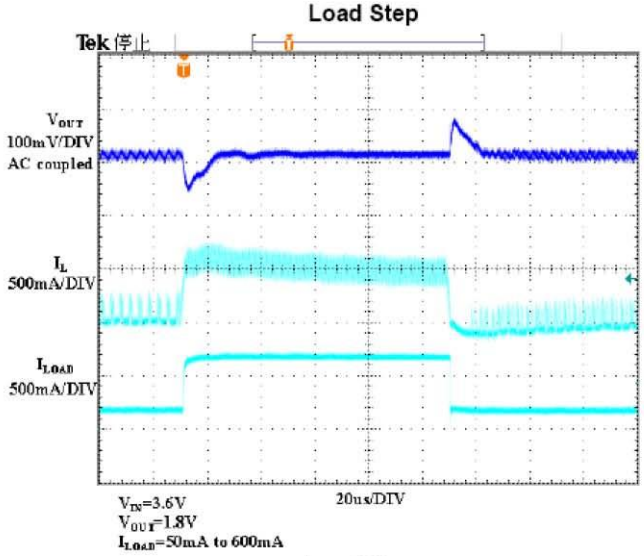
DC Regulation
(V_{OUT} = 1.8V; T_A = 25°C; L = 2.2μH; C_{OUT} = 22μF)



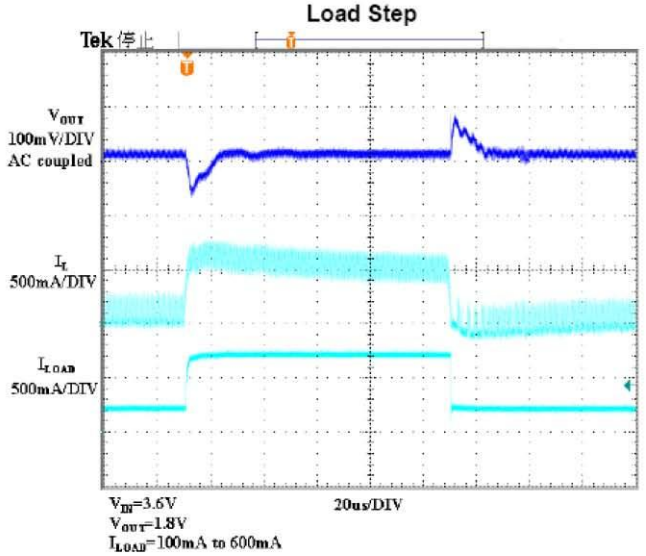
Load Step



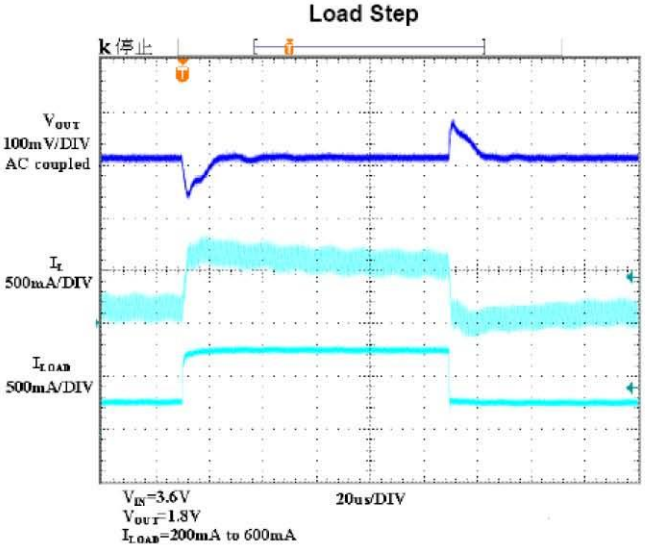
Load Step



Load Step



Load Step



Applications Information

Control Loop

The LP3208 is a high efficiency current mode synchronous buck regulator. Both the main (P-channel MOSFET) and synchronous (N-channel MOSFET) switches are built internally. With current mode operation, the PWM duty is controlled both by the error amplifier output and the peak inductor current. At the beginning of each cycle, the oscillator turn on the P-MOSFET switch to source current from VIN to SW output. Then, the chip starts to compare the inductor current with the error amplifier output. Once the inductor current is larger than the error amplifier output, the P-MOSFET switch is turned off. When load current increases, the feedback voltage will slightly drop. This causes the error amplifier to output a higher current level until the prior mentioned peak inductor current reach the same level. The output voltage then can be sustained at the same. When the top P-MOSFET switch is off, the bottom synchronous N-MOSFET switch is turned on. Once the inductor current reverses, both top and bottom MOSFET will be turn off to leave the SW pin into high impedance state. The LP3208's current mode control loop also includes slope compensation to suppress sub-harmonic oscillations at high duty cycles. This slope compensation is achieved by adding a compensation ramp to the inductor current signal.

LDO Mode

The LP3208's maximum duty cycle can reach 100%. That means the driver's main switch is turn on through-out whole clock cycle. Once the duty reaches 100%, the feedback path no longer controls the output voltage.

The output voltage will be the input voltage minus the main switch voltage drop. Over Current Protection LP3208 limits the peak main switch current cycle by cycle. When over current occurs, chip will turn off the main switch and turn the synchronous switch on until next cycle.

Short Circuit Protection

When the FB pin drops below 300mV, the chip will tri-state the output pin SW automatically. After 300us restart avoid over heat, chip will re-initiate PWM operation with soft start.

Thermal Protection

LP3208 will shutdown automatically when the internal junction temperature reaches 150℃ to protect both the part and the system.

Inductor selection

The output inductor is selected to limit the ripple current to some predetermined value, typically 20%~40% of the full load current at the maximum input voltage. Large value inductors lower ripple currents. Higher Vin or V_{OUT} also increases the ripple current as shown in equation. A reasonable starting point for setting ripple current is $\triangle I_L$=240mA(40% of 600mA).

The DC current rating of the inductor should be at least equal to the maximum load current plus half the ripple current to prevent core saturation. Thus, a 720Ma rated Inductor should be enough for most applications (600mA+120mA). For better efficiency, choose a low DC-resistance inductor.

CIN and COUT Selection

The input capacitance, CIN, is needed to filter the trapezoidal current at the source of the top MOSFET. To prevent large ripple voltage, a low ESR input capacitor Sized for the maximum RMS current should be used. RMS current is given by:

$$\Delta I_L = \frac{1}{(f)(L)} V_{OUT}\left(1-\frac{V_{OUT}}{V_{IN}}\right)$$

This formula has a maximum at VIN=2VOUT, where IRMS=IOUT/2.this simple worst-case condition is commonly. Used for design because even significant deviations do not offer much relief. Note that ripple current ratings from capacitor manufacturers are often based on only 2000 hours of life which makes it advisable to further derate the Capacitor, or choose a capacitor rated at a higher temperature Than required. Several capacitors may also be paralleled to meet size or height requirements in the design.

The selection of COUT is determined by the effective

$$I_{RMS} \quad I_{OUT(MAX)} \frac{V_{OUT}}{V_{IN}} \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

series resistance(ESR) that is required to minimize voltage ripple and load step transients, an well as the amount or bulk capacitance that is necessary to ensure that the control loop is stable. Loop stability can be checked by viewing the load transient response as described in later section. the output ripple, △ VOUT, is determined by:

Using ceramic input and output capacitors Higher

$$\Delta V_{OUT} \leq \Delta I_L \left[ESR + \frac{1}{8fC_{OUT}} \right]$$

values, lower cost ceramic capacitors are now becoming .Available in smaller case sizes ,their high ripple current ,high voltage rating and low ESR make them ideal for switching regulator applications. However care must be taken when these capacitors are used at the input and output. When a ceramic capacitor is use at input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the input ,VIN, At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at VIN large enough to damage the part.

Output voltage programming

The output voltage is set by a resistive divider according to the Following formula:

$$V_{OUT} = 0.6V\left(1 + \frac{R2}{R1}\right)$$

The external resistive divider is connected to the output, allowing Remote voltage sensing as shown in figure3.

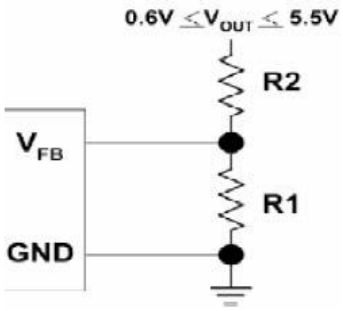


Figure3.

Efficiency considerations

The efficiency of a switching regulator is equal to the output Power divided by the input power times 100%.it is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement efficiency can be expressed as :

Efficiency= 100%- (L1+L2+L3...)

Where L1、 L2, etc. are the individual losses as a percentage of Input power .although all dissipative elements in the for most of losses: VIN quiescent current and I^2R loss dominates the efficiency loss at medium to high load currents. In a typical efficiency plot, the efficiency curve at very low load currents can be misleading since the actual power lost is of no consequence.

1. The VIN quiescent current is due to two components: the DC Bias current as given in the electrical characteristics and the internal main switch and synchronous switch gate charge currents. The gate charge current results from switching the gate capacitance of the internal power MOSFET switches. Each time the gate charge current results from switching the gate capacitance of the internal power MOSFET switches. Each time the gate is switches from high to low to high again, a packet of charge △ Q moves from VIN to ground.

The resulting △ Q/△ t is the current out of VIN that is typically larger than the DC bias current. In continuous mode.

LGATCHG=f(QT+QB)

Where QT and QB are the gate charges of the internal top and bottom switches. Both the DC bias and gate charge losses are proportional to VIN and thus their effects will be more pronounced at higher supply voltages

2. I^2R losses tae calculated from the resistances of the internal switches, RSW and external inductor RL. In continuous mode the average output current flowing through inductor L is “chopped” between the main switch and the synchronous switch. Thus, the series resistance looking into the LX pin is a function of both top and bottom MOSFER RDS(ON) and the duty cycle (DC) as follows:

RSW=RDS(ON)TOP×DC+RDS(ON)BOT×(1-DC)

The RDS(ON) for both the top and bottom MOSFETS can be obtained from the typical performance characteristics curves. Thus, to obtain I^2R losses, simply add RSW to RL and multiply the square of the average output current.

Other losses including CIN and COUT ESR dissipative losses and inductor core losses generally account for less than 2% of the total loss.

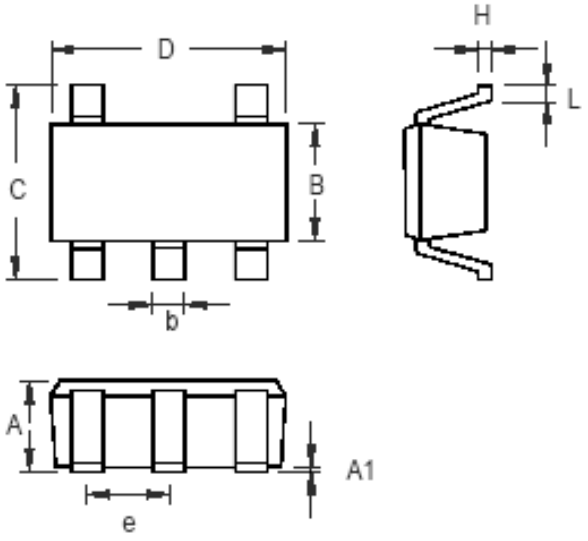
Checking Transient Response

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in load current. When a load step occurs, VOUT immediately shifts by an amount equal to ΔILOAD (ESR), where ESR is the effective series resistance of COUT. ΔILOAD also begins to charge or discharge COUT generating a feedback error signal used by the regulator to return VOUT to its steady-state value. During this recovery time, VOUT can be monitored for overshoot or ringing that would indicate a stability problem.

Layout Considerations

- Follow the PCB layout guidelines for optimal performance of LP3208.
- For the main current paths as indicated in bold lines, keep their traces short and wide.
- Put the input capacitor as close as possible to the device pins (VIN and GND).
- LX node is with high frequency voltage swing and should be kept small area. Keep analog components away from LX node to prevent stray capacitive noise pick-up.
- Connect feedback network behind the output capacitors. Keep the loop area small. Place the feedback components near the LP3208.
- Connect all analog grounds to a command node and then connect the command node to the power ground behind the output capacitors.

Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.889	1.295	0.035	0.051
A1	0.000	0.152	0.000	0.006
B	1.397	1.803	0.055	0.071
b	0.356	0.559	0.014	0.022
C	2.591	2.997	0.102	0.118
D	2.692	3.099	0.106	0.122
e	0.838	1.041	0.033	0.041
H	0.080	0.254	0.003	0.010
L	0.300	0.610	0.012	0.024

SOT-23-5 Surface Mount Package

单击下面可查看定价，库存，交付和生命周期等信息

>>LOW POWER(微源半导体)