Build in EQ Function 12W Class-D Audio Amplifier With AGC function

General Description

The LPA2101 is a mono efficient, digital amplifier power stage for driving speakers up to 12W/4Ω. The LPA2101 integrates AGC(automatic gain control)circuit for a NCN(Non-Crack Noise) technical in application without damaging speaker when a high power signal occurs. when function failed happened to input capacitor, the chip will cut off the output circuit through detecting the input signal to protect speaker. The LPA2101 device is fully protected against faults with short-circuit protection and thermal protection as well as over-voltage and DC protection. Faults are reported back to the processor to prevent devices form being damaged during overload conditions.

Features

- 12W Output at 10% THD with a 4Ω Load and10V PVCC for amplifier
- Wide voltage range: 4.5V~12V
- Integrated 2 degree AGC circuit
- Integrated Self-Protection Circuits Including Over-Voltage, Under-Voltage, Over-Temperature, DC-Detect, and Short Circuit
- Multiple Switching Frequencies
  - AM Avoidance
  - Master/Slave Synchronization
  - Up to 350KHz Switching Frequency
- High Efficient Class-D Operation: >90%
- Indication for NCN(Non-Crack Noise)
- Pb-Free Package

Order Information

LPA2101 □ □ □

- F: Pb-Free
- Package Type
  SO : SOP16

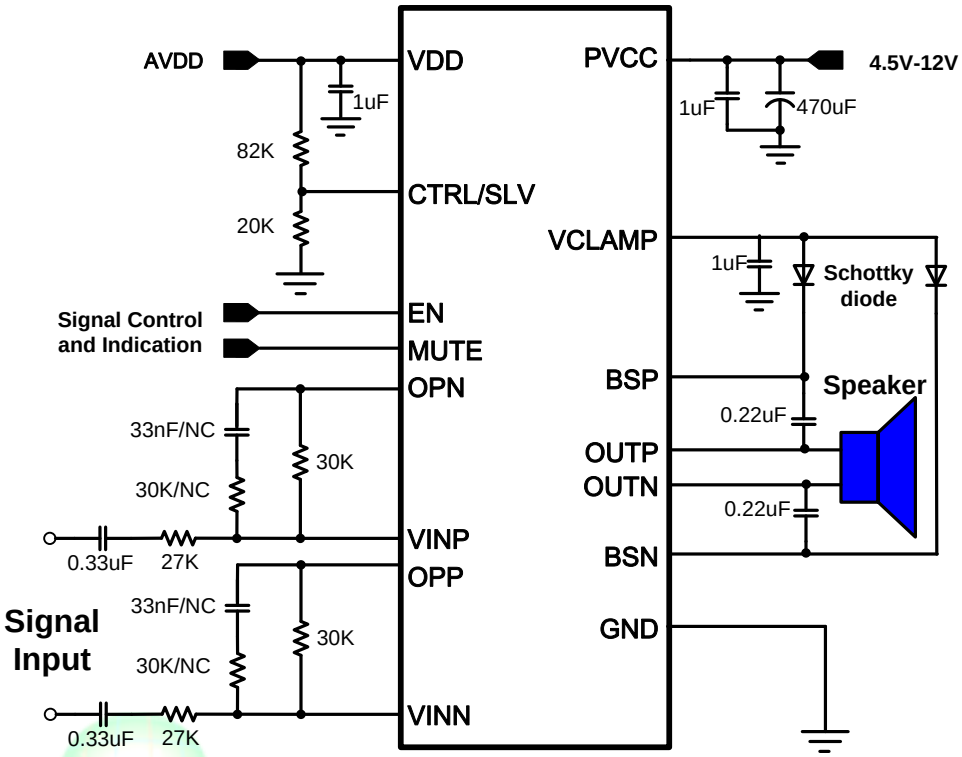
Applications

- Mini-Micro Component, Speaker Bar, Docks
- After-Market Automotive
- Consumer Audio Applications, CRT TV
- Portable Bluetooth Speaker
- Cellular and Smart mobile phone
- Square Speaker

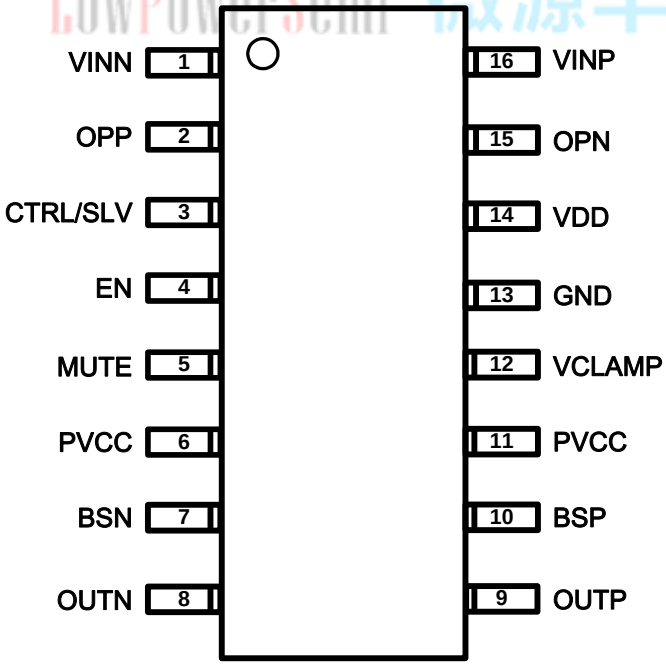
Marking Information

Device	Marking	Package	Shipping
LPA2101	LPS LPA2101 YWX	SOP-16	xxxK/REEL
Y: Y is year code. W: W is week code. X: X is series number.			

Typical Application Circuit



Pin Configuration(TOP View)

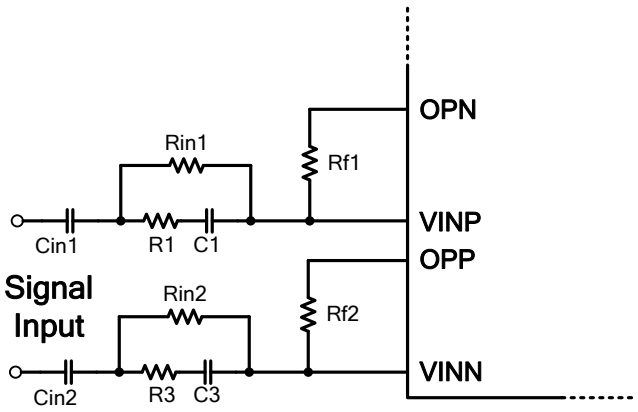


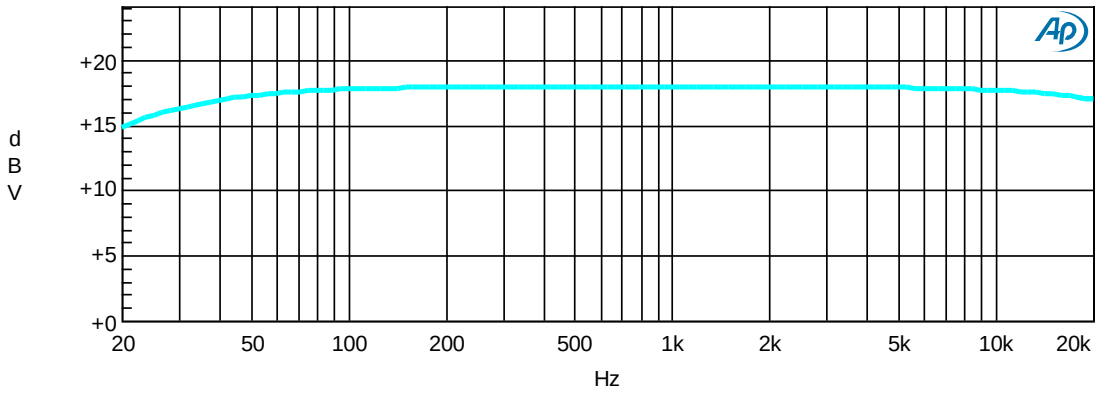
SOP16

Functional Pin Description

SOP16 Pin Num	Pin Name	Description
1	VINN	Negative signal input.
2	OPP	Plus signal output.
3	CTRL/SLV	AGC control and selects between Master and Slave mode depending on pin voltage divider. Show detail in sheet 1.
4	EN	Chip enable pin. Active high.
5	MUTE	Mute control. Active low.
6	PVCC	Power supply for chip.
7	BSN	Negative self boost output pin. There is a 220nF capacitor between this pin and OUTN.
8	OUTN	Minus signal output.
9	OUTP	Positive channel output.
10	BSP	Positive self boost output pin. There is a 220nF capacitor between this pin and OUTN.
11	PVCC	Power supply for chip.
12	VCLAMP	Supply for internal Power MOS. There should be a 1uF capacitor between this pin and GND.
13	GND	Ground.
14	VDD	Internal power supply. There should be a 1uF capacitor between this pin and GND.
15	OPN	Negative signal output.
16	VINP	Positive signal input.

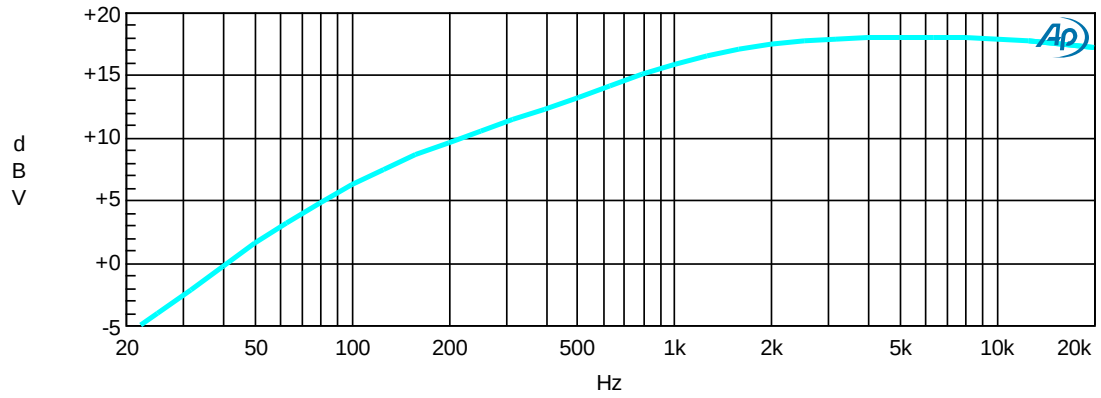
Classical Application 1: Low Restraint





Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Cyan	Solid	3	Analyzer.Level A	Left	

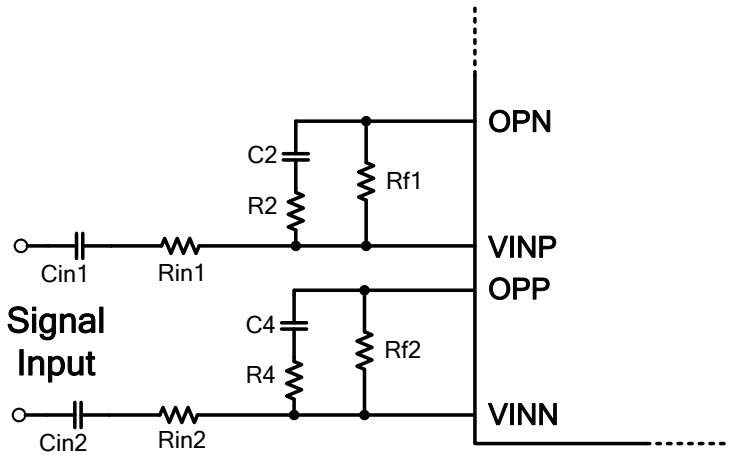
Cin1/2=1uF; Rin1/2=20K; R1/3=NC; C1/3=NC; Rf1/2=47K

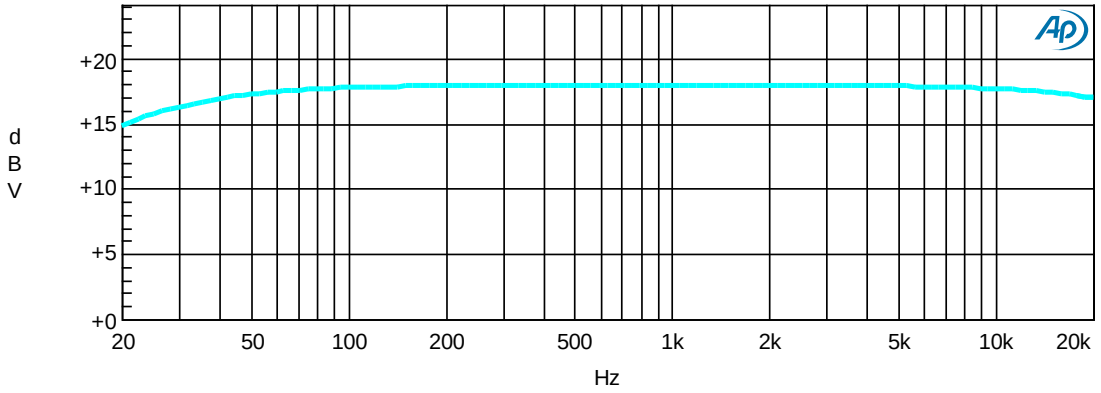


Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Cyan	Solid	3	Analyzer.Level A	Left	

Cin1/2=47nF; Rin1/2=20K; R1/3=20K;C1/3=10nF; Rf1/2=47K

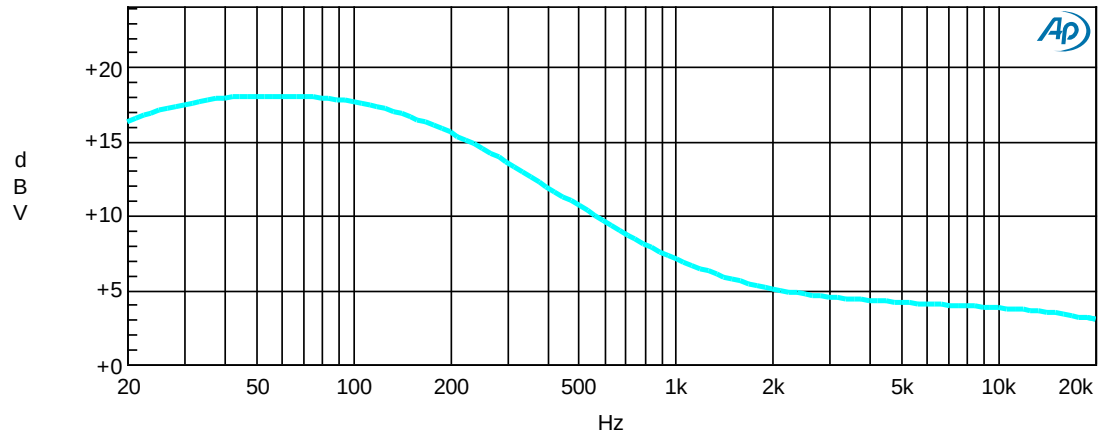
Classical Application 2: High Restraint





Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Cyan	Solid	3	Analyzer.Level A	Left	

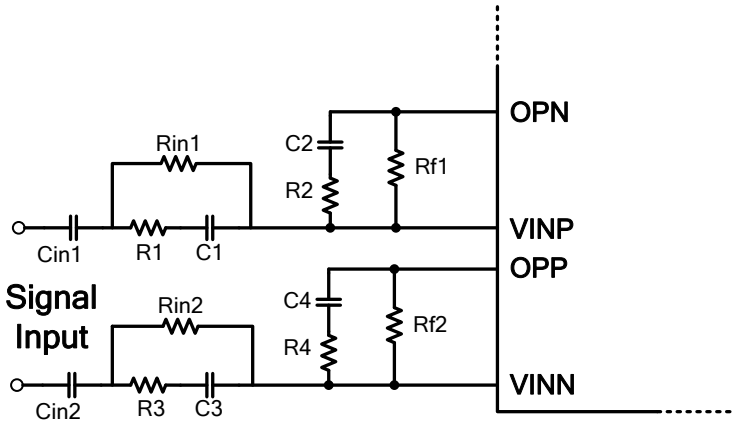
Cin1/2=1uF; Rin1/2=20K; C2/4=NC; R2/4=NC; Rf1/2=47K

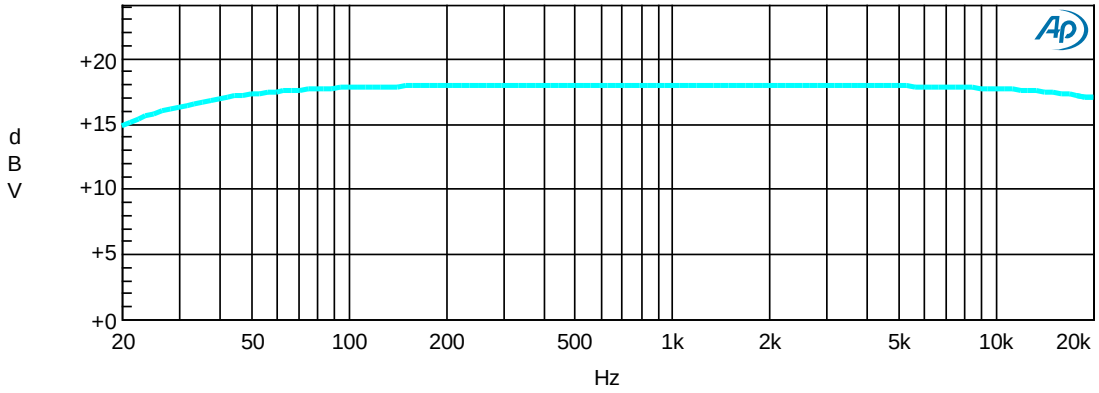


Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Cyan	Solid	3	Analyzer.Level A	Left	

Cin1/2=0.47uF; Rin1/2=20K; C2/4=15nF; R2/4=10K; Rf1/2=47K

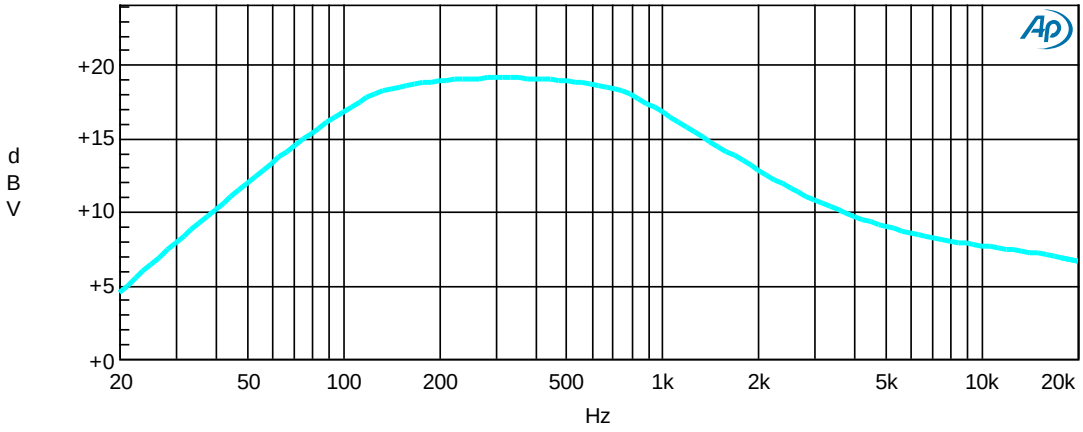
Classical Application 3: High and Low Restraint (Band Pass)





Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Cyan	Solid	3	Analyzer.Level A	Left	

Cin1/2=1uF; Rin1/2=20K;R1/3=NC; C1/3=NC; C2/4=NC; R2/4=NC; Rf1/2=47K



Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Cyan	Solid	3	Analyzer.Level A	Left	

Cin1/2=0.47uF; Rin1/2=20K; R1/3=20K; C2/4=10nF; R2/4=10K; Rf1/2=47K

Absolute Maximum Ratings Note 1

- ✧ Supply Voltage to GND ---------- -0.3V to 15V
- ✧ Other Pin to GND ---------- -0.3V to 6V
- ✧ Maximum Junction Temperature ---------- 150°C
- ✧ Operating Ambient Temperature Range (Ta) ---------- -40℃ to 85°C
- ✧ Maximum Soldering Temperature (at leads, 10 sec) ---------- 260°C

Note 1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Information

- ✧ Maximum Power Dissipation (ESOP-16, PD,TA=25°C) ---------- 1.9W
- ✧ Thermal Resistance (ESOP-16, JA) ---------- 65℃/W

ESD Susceptibility

- ✧ HBM(Human Body Mode) Note 2 ---------- 2KV
- ✧ MM(Machine Mode) Note 3 ---------- 200V

Note 2. The Human body model (HBM) is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. The testing is done according JEDEC.

Note 3. Machine Model (MM) is a 200pF capacitor discharged through a 500nH inductor with no series resistor into each pin. The testing is done according JEDEC.

Electrical Characteristics

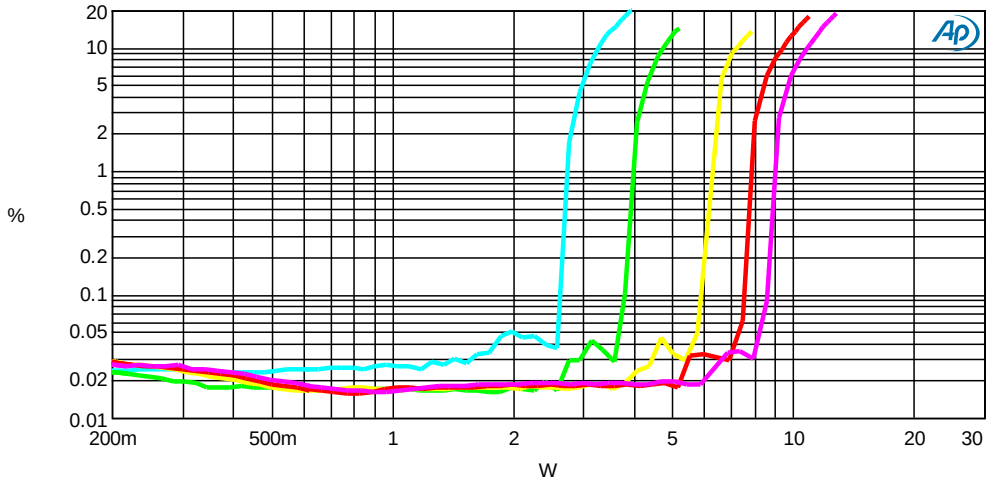
(T_A = 25°C, PVCC = 12V, R_L = 4 Ω, unless otherwise noted)

Parameter	Symbol	Test Conditions		Min	Typ	Max	Units
Supply power	PVCC			4.5		12	V
Output power	P_O	THD+N=10%, f=1KHz,RL=4Ω	PVCC=12V		12		W
			PVCC=10V		10		
		THD+N=10%, f=1KHz,RL=8Ω	PVCC=12V		8		
			PVCC=10V		6		
		THD+N=1%, f=1KHz,RL=4Ω	PVCC=12V		12		
			PVCC=10V		9		
		THD+N=1%, f=1KHz,RL=8Ω	PVCC=12V		7		
			PVCC=10V		4.8		
Power supply ripple rejection	PSRR	INPUT ac-grounded with CIN=0.47uF, PVCC=12V	f=100HZ		70		dB
			f=1KHz		73		
Signal-to-noise ratio	SNR	PVCC=12V,P_{OUT}=12W,R_L=4Ω	f=1KHz		92		dB
Eifficency	η	R_L=4Ω,P_O=12W	f=1KHz		90		%
Quiescent current	I_Q	PVCC=12V	No load		15		mA
Shutdown current	I_{SD}	PVCC=12V			2		uA
Internal power supply	VDD	PVCC=12V			5.1		V
Shutdown supply voltage(min)		PVCC=12V			>2.0		V
Shutdown supply current (min)		PVCC=12V			70		uA
MUTE supply voltage(min)		PVCC=12V			>1.9		V
MUTE supply Current		PVCC=12V			70		uA
Offset output voltage	V_{OS}	PVCC=12V, V_{SD} =0V			5		mV
fOSC Oscillator frequency	fsw				350		KHz

Typical Operating Characteristic For Amplifier

PO VS THD

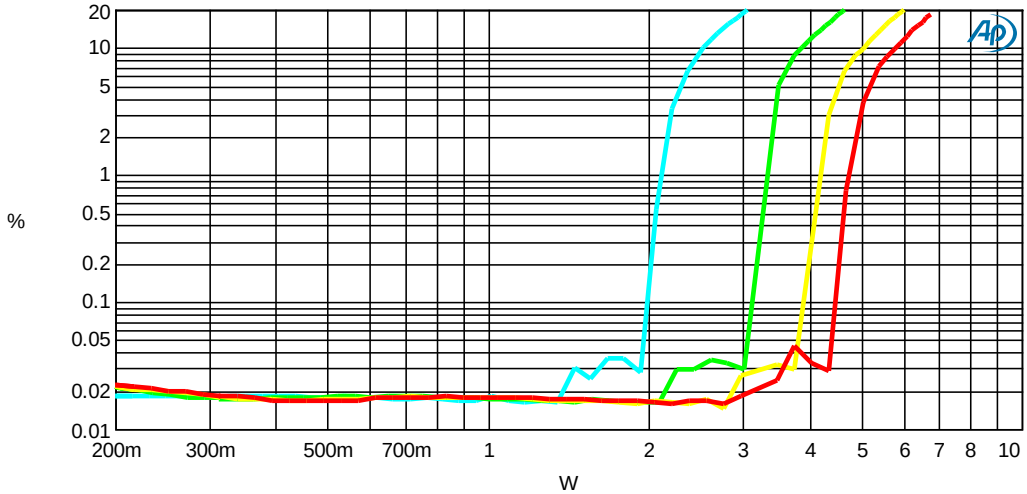
Audio Precision



Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Cyan	Solid	3	Analyzer.THD+N Ratio A	Left	PVCC=5V,RL=4ohm
2	1	Green	Solid	3	Analyzer.THD+N Ratio A	Left	PVCC=6V,RL=4ohm
3	1	Yellow	Solid	3	Analyzer.THD+N Ratio A	Left	PVCC=7.4V,RL=4ohm
4	1	Red	Solid	3	Analyzer.THD+N Ratio A	Left	PVCC=8.4V,RL=4ohm
5	1	Magenta	Solid	3	Analyzer.THD+N Ratio A	Left	PVCC=9V,RL=4ohm

PO VS THD@4ohm.ats2

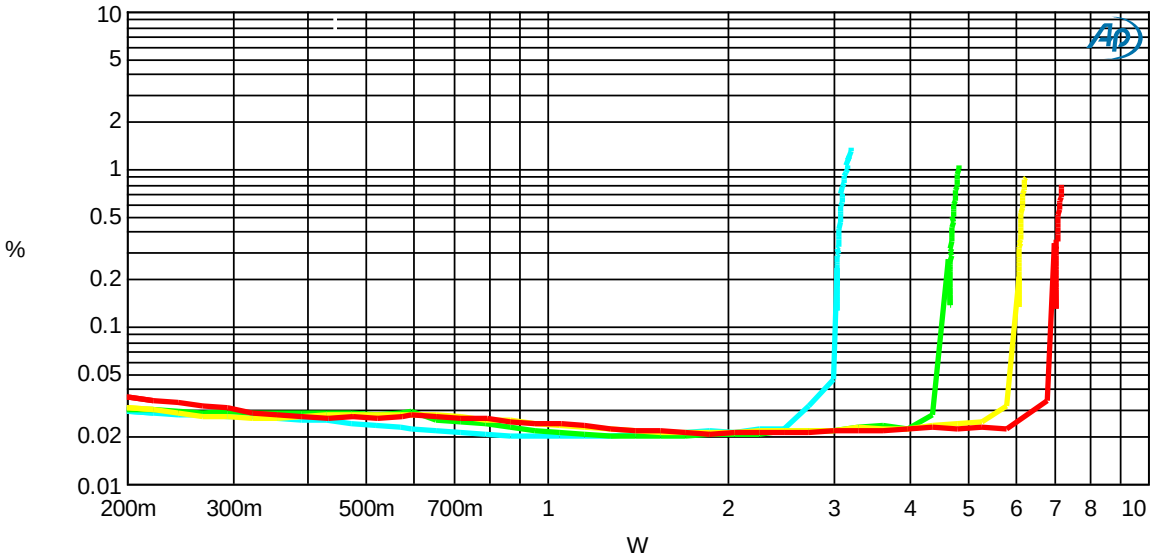
Audio Precision



Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Cyan	Solid	3	Analyzer.THD+N Ratio A	Left	PVCC=6V,RL=8ohm
2	1	Green	Solid	3	Analyzer.THD+N Ratio A	Left	PVCC=7.4V,RL=8ohm
3	1	Yellow	Solid	3	Analyzer.THD+N Ratio A	Left	PVCC=8.4V,RL=8ohm
4	1	Red	Solid	3	Analyzer.THD+N Ratio A	Left	PVCC=9V,RL=8ohm

PO VS THD@8ohm.ats2

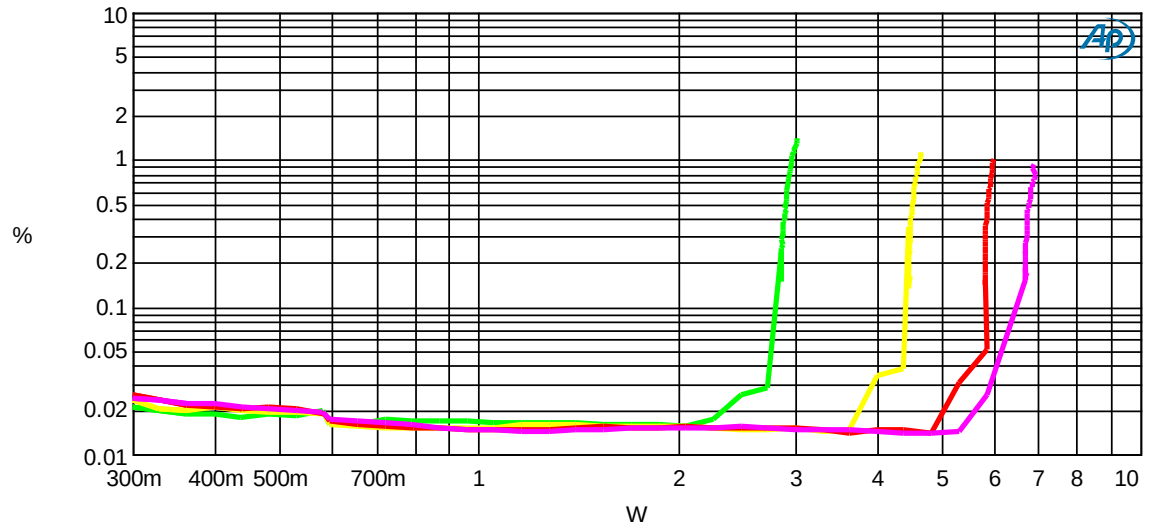
Audio Precision



Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Cyan	Solid	3	Analyzer.THD+N Ratio A	Left	PVCC=6V,RL=4ohm,NCN1
2	1	Green	Solid	3	Analyzer.THD+N Ratio A	Left	PVCC=7.4V,RL=4ohm,NCN
3	1	Yellow	Solid	3	Analyzer.THD+N Ratio A	Left	PVCC=8.4V,RL=4ohm,NCN
4	1	Red	Solid	3	Analyzer.THD+N Ratio A	Left	PVCC=9V,RL=4ohm,NCN1

PO VS THD@4ohm NCN1.ats2

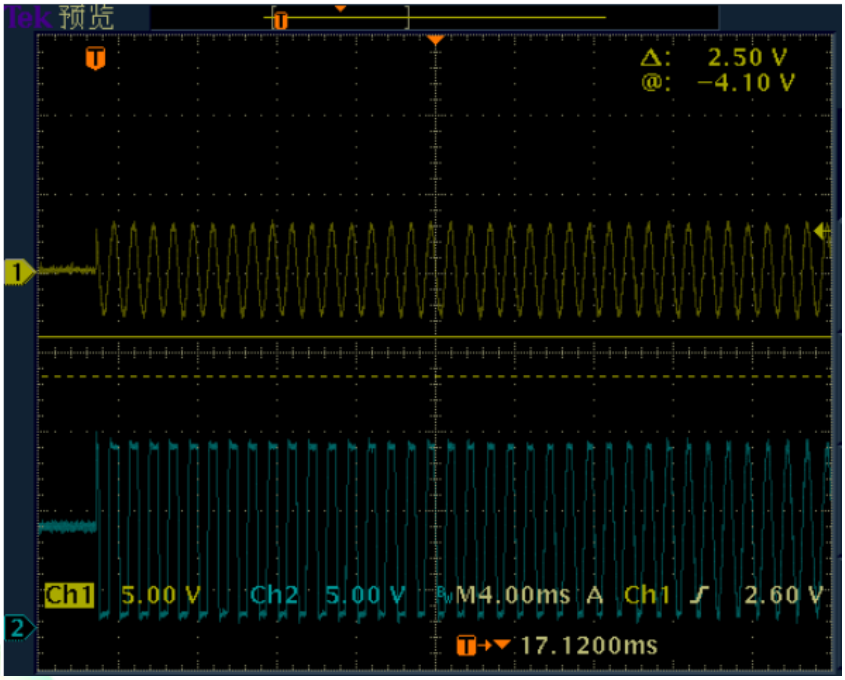
Audio Precision



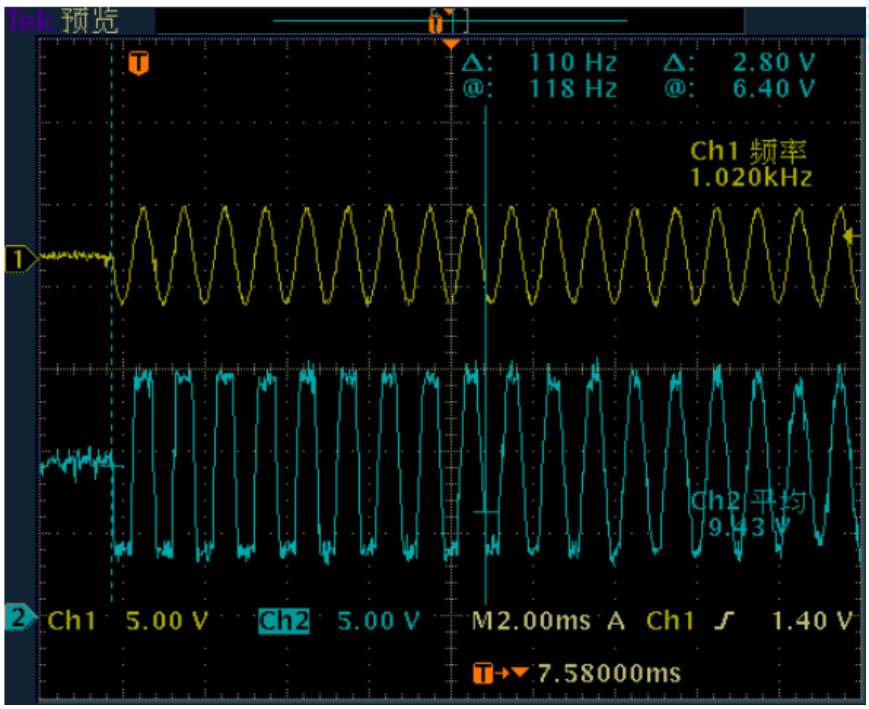
Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
2	1	Green	Solid	3	Analyzer.THD+N Ratio A	Left	PVCC=6V,RL=4ohm,NCN
3	1	Yellow	Solid	3	Analyzer.THD+N Ratio A	Left	PVCC=7.4V,RL=4ohm,NC
4	1	Red	Solid	3	Analyzer.THD+N Ratio A	Left	PVCC=8.4V,RL=4ohm,NC
5	1	Magenta	Solid	3	Analyzer.THD+N Ratio A	Left	PVCC=9V,RL=4ohm,NCN

PO VS THD@4ohm NCN2

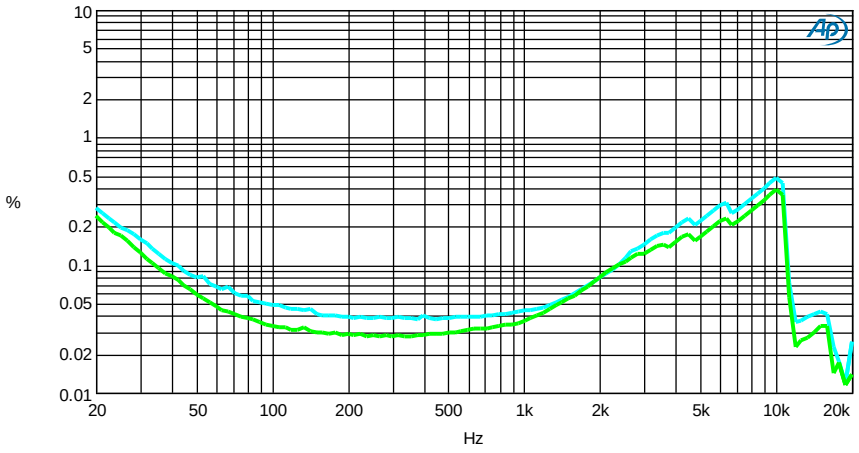
First degree NCN waveform



Second degree NCN waveform

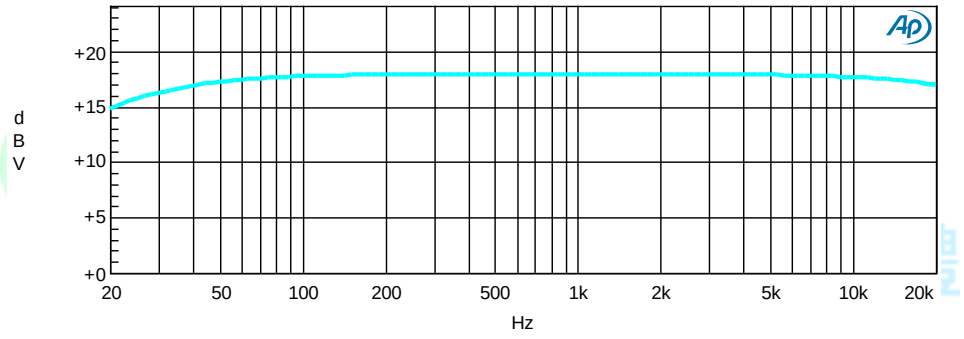


FRQ VS THD



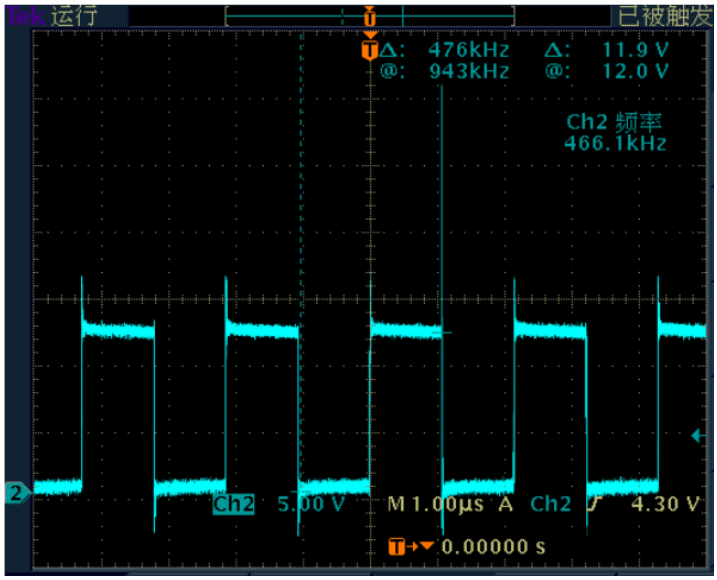
Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Cyan	Solid	3	Analyzer.THD+N Ratio A	Left	VDD=12V,RL=4ohm,Po=1W
2	1	Green	Solid	3	Analyzer.THD+N Ratio A	Left	VDD=9V,RL=4ohm,Po=1W

Frequency response

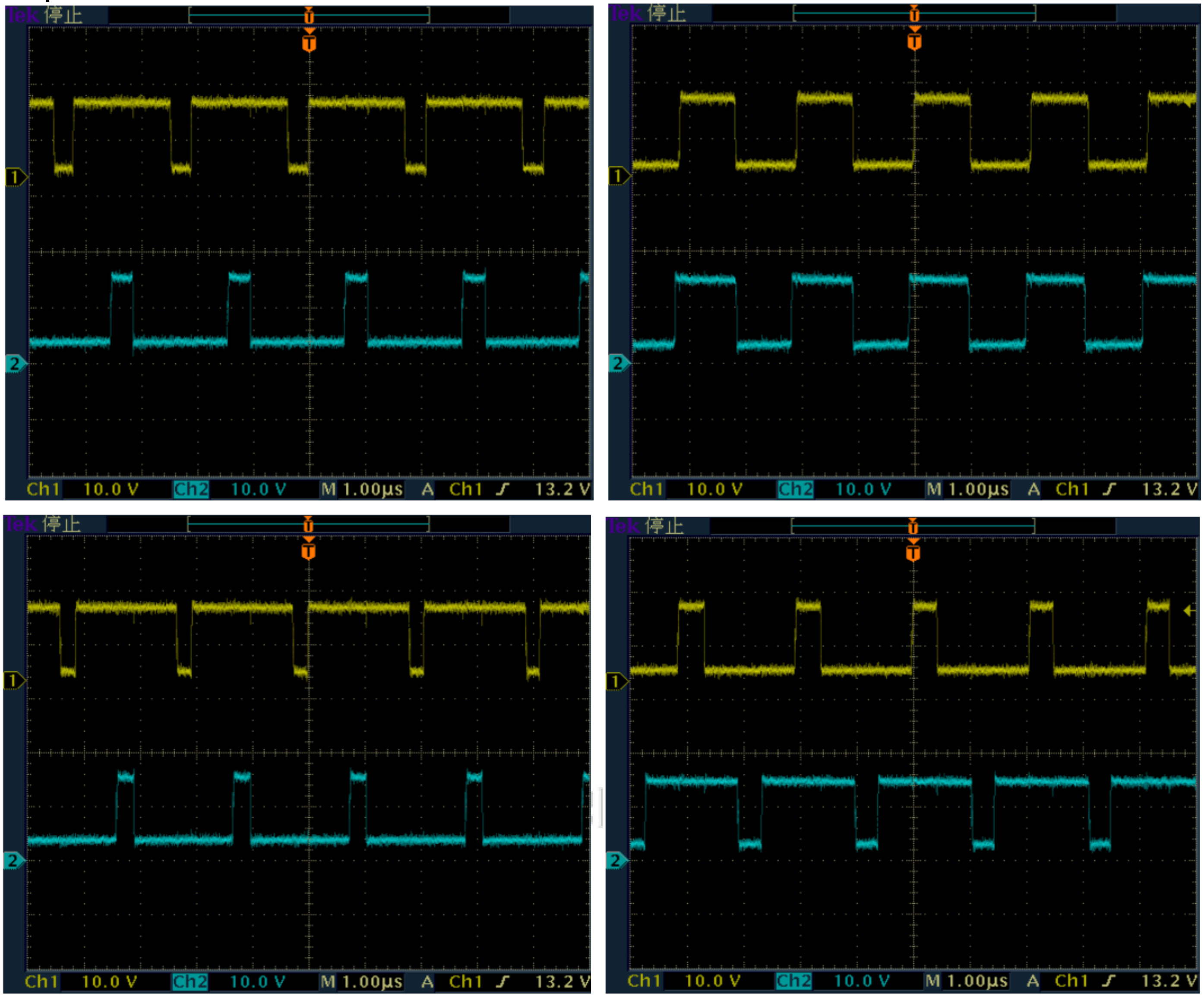


Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Cyan	Solid	3	Analyzer.Level A	Left	

Output waveform without load



Output waveform



Applications Information(for Amplifier)

AGC For NCN

The LPA2101 integrates an automatic gain control technology to achieve NCN(Non-Crack Noise). The circuit could set different NCN degree by different resistance divider applying to CTRL/SLV to protect speaker as showed below.R1+R2 should less than 100K.

The function of NCN(Non-Crack Noise) needs two key processes: Detection of Crack and Suppression gain. When an overload signal applied to speaker, chip will suppress the gain of circuit through real-time detection output signal in a certain time. The suppression will be stronger until the output signal fall to the available range with a stable balance between the signal and suppression. In the same way, the suppression will be weaker when the input signal amplitude decreases.

Sheet.1 NCN function and Master/Slave synchronization

Voltage on CTRL/SLV	NCN	Master/Slave
CTRL/SLV < 1/6 VDD	Disabled	Master
1/6 VDD < CTRL/SLV < 2/6 VDD	2degree	Master
2/6 VDD < CTRL/SLV < 3/6 VDD	1degree	Master

Note： 1degree：Detection delay time: 45ms，release of suppression: 2.6s；

2degree: Detection delay time: 10ms，release of suppression: 1.2s；

Shutdown operation

In order to reduce power consumption while not in use, the LPA2101 contains shutdown circuitry to turn off the amplifier's bias circuitry. This shutdown feature turns the amplifier off when logic low is applied to the EN pin. By switching the EN pin connected to GND, the LPA2101 supply current draw will be minimized in idle mode.

Power supply decoupling

The LPA2101 is a high performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output THD and PSRR a low as possible. Power supply decoupling affects low frequency response. Optimum decoupling is achieved by using two capacitors of different types targeting to different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 1.0μF, works best, placing it as close as possible to the device VDD terminal. For filtering lower- frequency noise signals, a large capacitor of 20μF (ceramic) and a capacitor of 220uF(electrolytic) are recommended, placing them near the audio power amplifier.

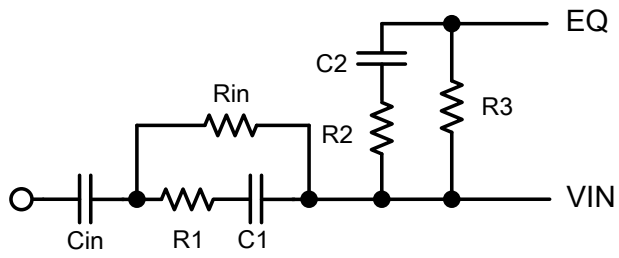
Short Circuit Protection (SCP)

The LPA2101 has short circuit protection circuitry on the outputs to prevent damage to the device when output-to-output or output-to-GND short occurs. When a short circuit is detected on the outputs, the outputs are disabled immediately. If the short was removed, the device activates again.

Signal Frequency suppress

The LPA2101 has an OPP/N pin which is the negative output of amplifier as show below. With R2 and C2, we can suppress high frequency part of signal. And the low frequency part of signal could be attenuated by R1 and C1.

$$f_H = \frac{1}{2\pi R_1 C_1} \quad ; \quad f_L = \frac{1}{2\pi R_2 C_2}$$



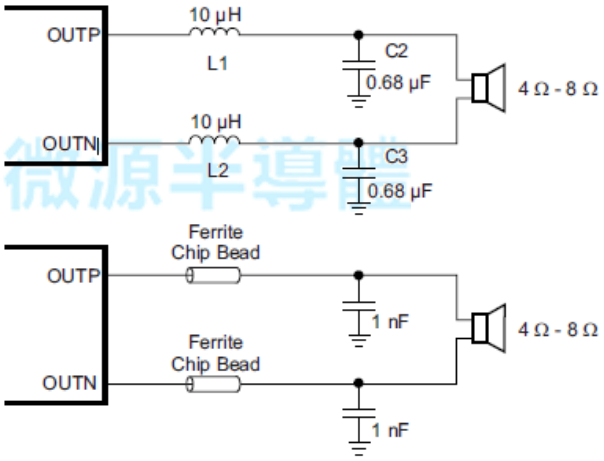
Over Temperature Protection

Thermal protection on the LPA2101 prevents the device from damage when the internal die temperature exceeds 150℃. There is a 15 degree tolerance on this trip point from device to device. Once the die temperature exceeds the thermal set point, the device outputs are disabled. This is not a latched fault. The thermal fault is cleared once the temperature of the die is reduced by 30℃. This large hysteresis will prevent motor boating sound well and the device begins normal operation at this point without external system intervention.

How to reduce EMI

A simple solution is to put an additional capacitor at power supply terminal for power line. The traces from amplifier to speakers should design as short as we can. The LPA2101 has been tested with a simple ferrite bead filter for a variety of applications. The LPA2101 EVM passes FCC class-B specifications under these conditions using twisted speaker wires. The size and type of ferrite bead can be selected to meet application requirements. Also, the filter capacitor can be increased if necessary with some impact on efficiency. There may be a few circuit instances where it is necessary to add a complete LC reconstruction filter. These circumstances might occur if there are nearby circuits which are sensitive to noise. In these cases a classic second order Butterworth filter similar to those shown in the figures below can be used.

Some systems have little power supply decoupling from the AC line but are also subject to line conducted interference (LCI) regulations. These include systems powered by "wall warts" and "power bricks." In these cases, LC reconstruction filters can be the lowest cost means to pass LCI tests. Common mode chokes using low frequency ferrite material can also be effective at preventing line conducted interference.



PCB Layout notices

1, In the path of the power supply, plus a 1uF and a 10uF to ground high-frequency filter capacitor. These caps can be connected to the thermal pad directly for an excellent ground connection. Consider adding a small, good quality low ESR ceramic capacitor may achieve better sound effects.

2, Large (470 μF or greater) bulk power supply decoupling capacitors should be placed near the LPA2101 on the PVCC supplies. Local, high-frequency bypass capacitors should be placed as close to the PVCC pins as possible.

3, The power line, ground line and filter capacitor and bypass capacitors as close to the chip's pins, remember not to put the capacitor on the back of the board, through tiny holes through the jumper even over. Keep the current loop from each of the outputs through the ferrite bead and the small filter cap and back to GND as small and tight as possible. The size of this current loop determines its effectiveness as an antenna.

4, Power, ground, and a large current line must try to be wide enough, if you want to add vias, the number of through-holes must be at least 6. The thermal pad must be soldered to the PCB for proper thermal performance and optimal reliability.

5, GND and VDD should be put independently, high-power signals to avoid interference.

6, If you want to pursue as large as the effect of power, a large selection of speakers or sound chamber with low resistance (such as 3.6Ω) speakers, or added to improve the supply voltage.

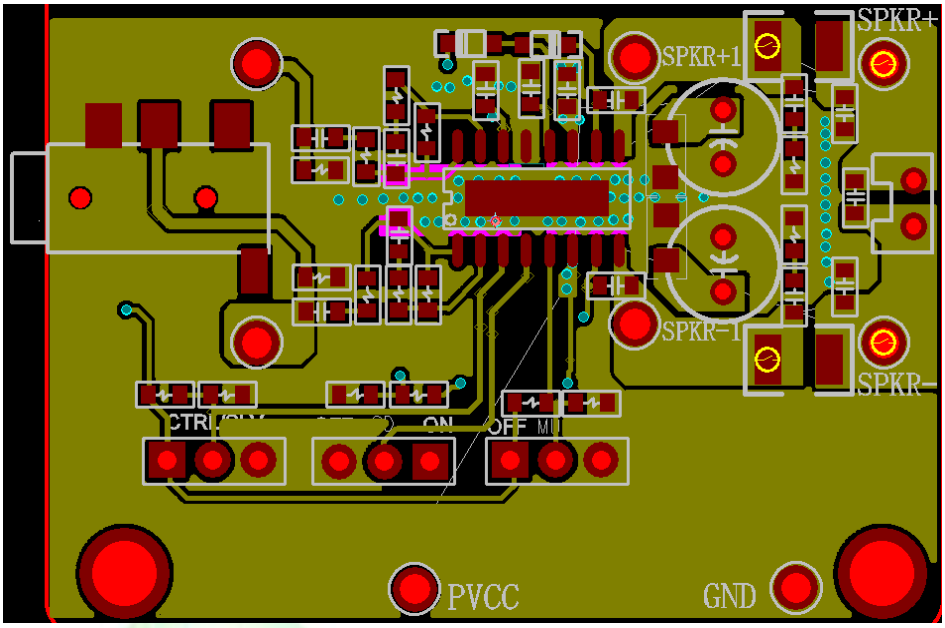
7, Including the line between large current cell and chip, the inductor should be as close and short as possible to chip for a high performance. Adding a coil to this pin would be helpful for EMI certification. If there is a high standards needed in LPA2101 application, we could add a coil and capacitor between chip and speaker constituting a LC filter which coil would be 100MHz, 600Ω and its DCI beyond 4A placing as close as possible to chip, the capacitor should be 1nF connecting the GND.

8, The position under the amplifier chip on the board must be added vents and large areas of exposed copper and tin to enhance heat dissipation.

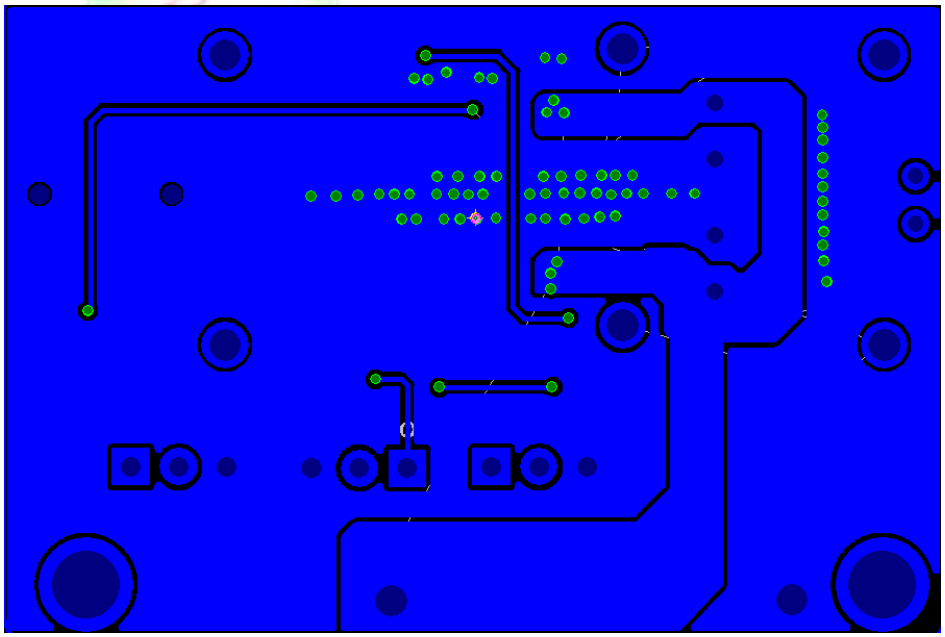
9, In case of fixed gain and meeting demand, it should make C_{IN} small as possible as we can because it constitute a high through filter with Rin which cutoff frequency is 1/2*3.414*Cin*Rin. A high capacitance cap could make POP worse.

PCB LAYOUT

TOP VIEW:

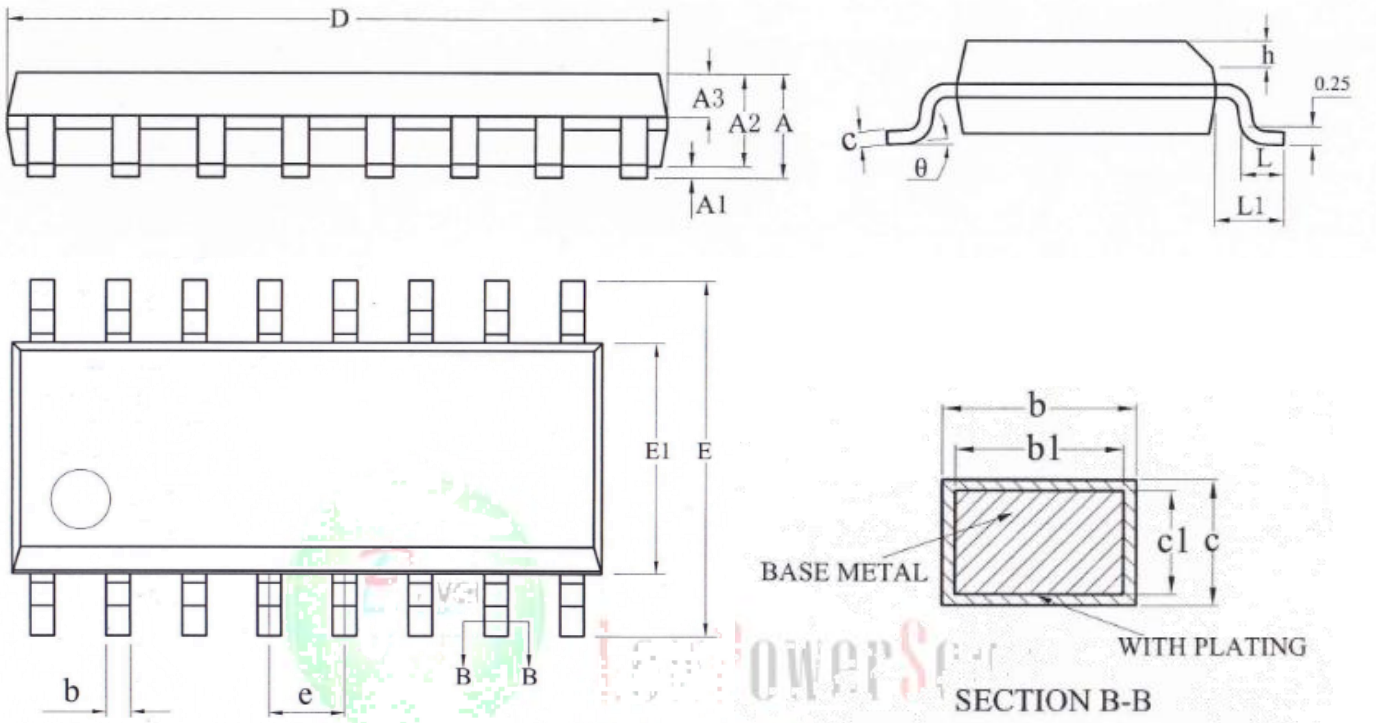


BOTTOM VIEW:



Packaging Information

SOP-16



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.75
A1	0.10	—	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	—	0.47
b1	0.38	0.41	0.44
c	0.20	—	0.24
c1	0.19	0.20	0.21
D	9.80	9.90	10.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27BSC		
h	0.25	—	0.50
L	0.50	—	0.80
L1	1.05REF		
θ	0	—	8°

单击下面可查看定价，库存，交付和生命周期等信息

>>LOW POWER(微源半导体)