High Slew Rate Rail-to-Rail Single Operational Amplifiers with OTP

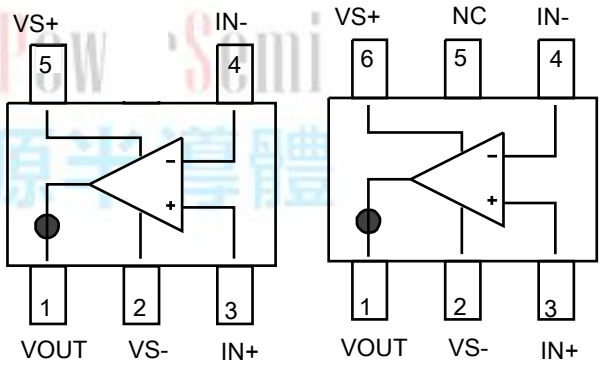
General Description

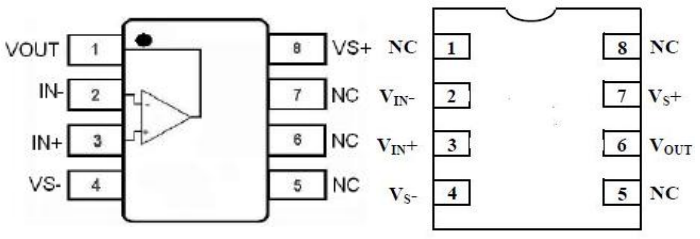
The LP6291 is a rail-to-rail one channel operational amplifier with wide supply range from 6V to 18V. It provides 0.5V beyond the supply rails of common mode input range and capability of rail-to-rail output swing as well. This enables the amplifier to offer maximum dynamic range at any supply voltage among many applications. A 20MHz gain bandwidth product allows LP6291 to perform more stable than other devices in Internet applications. With features of 40V/μs high slew rate and 200ns of fast settling time, as well as 100mA (sink and source) of high output driving capability, the LP6291 is ideal for the requirements of flat panel Thin Film Transistor Liquid Crystal Displays (TFT-LCD) panel grayscale reference buffers application. Due to insensitive to power supply variation, LP6291 offers flexibility of use in multitude of applications such as battery power, portable devices and anywhere low power consumption is concerned. With standard operational amplifier pin assignment, the LP6291 is offered in a space saving 6-Pin SOT-26 package and specified over the -40°C to +85°C temperature range.

Features

- Wide supply voltage range 6V ~ 18V
- Input range 500mV beyond the rails
- Unity-gain stable
- Rail-to-rail output swing
- High slew rate 40V/μs
- GBWP 20MHz
- 30MHz -3dB Bandwidth
- Ultra-small Package SOT-25、TSOT25、SOT-26、TSOT-26 and TSSOP-8

Pin Configurations





Order Information

LP6291 □ □ □

- F: Pb-Free
- Package Type
  - B5: SOT23-5
  - B6: SOT23-6
  - X5: TSOT23-5
  - X6: TSOT23-6
  - SO: SOP-8
  - QV: DFN-8

Applications

- TFT-LCD Reference Driver, ADC/DAC Buffer, Active Filter
- Office Automation, Wireless LANs, Portable Electronics
- Personal Communication Devices
- Direct Access Arrangement, Electronic Notebook
- Personal Digital Assistant (PDA)
- Touch-Screen Display, Sampling ADC Amplifier

Pin Description

Pin Name	Pin Function
VOUT	Operational Amplifier Output.
VS-	IC GROUND or Negative power supply.
IN+	Operational Amplifier Non-Inverting Input.
IN-	Operational Amplifier Inverting Input.
VS+	Supply Voltage VCC can range from 6V to 18V.

Absolute Maximum Ratings Note 1

- ✧ Supply Voltage VS+ to VS- ---------- 18V
- ✧ Input Voltage ----------VS- -0.5V to VS+ +0.5V
- ✧ Maximum Continuous Output Current ----------100mA
- ✧ Maximum Die Temperature ---------- 125°C
- ✧ Storage Temperature ---------- -65℃ to 150°C
- ✧ Operating Temperature Range (TJ) ---------- -40℃ to 85°C
- ✧ Maximum Soldering Temperature (at leads, 10 sec) ---------- 260°C

Important Note:

All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: TJ = TC = TA

Electrical Characteristics

(V_{S+}= +5V, V_{S-} = -5V, R_L = 10kΩ and C_L = 10pF to 0V, T_A = 25°C unless otherwise specified.)

Parameter	Description	Condition		Min	Typ	Max	Units
Input Characteristics							
V_{OS}	Input Offset Voltage	V_{CM}= 0V			2	12	mV
TCV_{OS}	Average Offset Voltage	[1]			5		µV/°C
I_B	InputDrift Bias Current	V_{CM}= 0V			2	50	nA
R_{IN}	Input Impedance				1		GΩ
C_{IN}	Input Capacitance				1.35		pF
CMIR	Common-Mode Input			-5.0		+5.5	V
CMRR	Common-ModeRange Rejection	for VIN from -5.5V to 5.5V		50	70		dB
A_{VOL}	Open-Loop Gain	0.5V ≦VOUT≦4.5V		75	90		dB
Output Characteristics							
V_{OL}	Output Swing Low-	VS+=8V,VS-=-8V,I_L=-5mA			-7.92	-	V
V_{OH}	Output Swing High	VS+=8V,VS-=-8V,I_L=5mA		7.85	7.92		V
I_{SC}	Short Circuit Current	(Note 1)			±350		mA
I_{OUT}	Output Current				±100		mA
I_{peak}	I_{peak} Current	VS+=14V, VS-=0V (Note 2)	Source Current: I load V_{OUT} to GND		450		mA
			Sink Current: I load V_{OUT} to V_{DD}				
Power Supply Performance							
PSRR	Power Supply Rejection Ratio	VS is moved from ±2.25V to ±7.75V		60	80		dB
I_S	Supply Current	No Load			3		mA

Parameter	Description	Condition	Min	Typ	Max	Units
Dynamic Performance						
SR	Slew Rate [2]	VS+=8V,VS-=-8V, -4.0V≦VOUT≦ 4.0V, 20% to 80%	30	40		V/μs
t_S	Settling to +0.1% (AV = +1)	(AV = +1), V_O=2V Step		500		Ns
BW	-3dB Bandwidth	R_L = 10kΩ, C_L=10pF		30		MHz
GBWP	Gain-Bandwidth Product	R_L = 10kΩ, CL=10pF		20		MHz
PM	Phase Margin	R_L = 10kΩ, CL = 10 pF		50		Degree
CS	Channel Separation	f = 1 MHz		75		S dB
Temperature Performance						
Temp	Thermal Shutdown			150		℃
1. Measured over operating temperature range 2. Slew rate is measured on rising and falling edges						

Note 1: Short circuit current is tested with one output at a time.
Note 2: I_{peak} current is for a 1μs pulsed current only , not to exceed thermal characteristics of package.

Typical Operating Characteristics

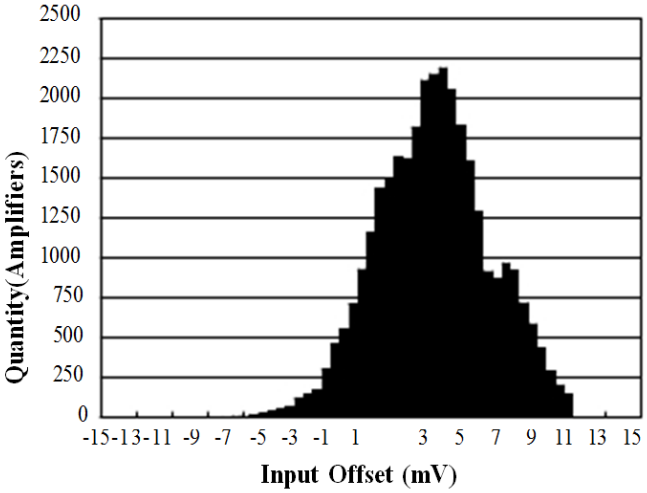


Figure (a) Input Offset Voltage Distribution

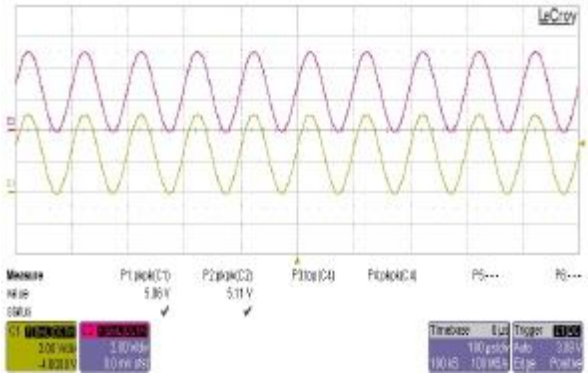


Figure (b) Rail to Rail Capability

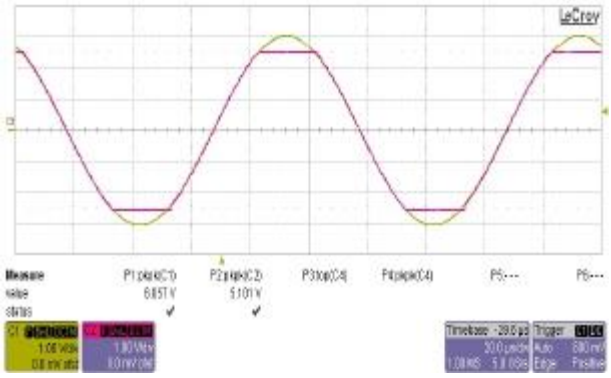


Figure (c) Input Beyond the Rails Signal

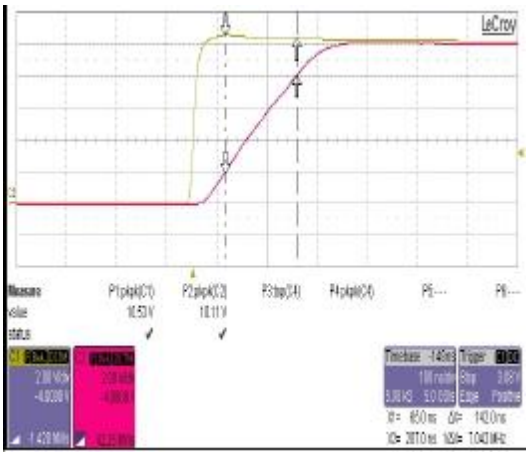


Figure (d) Large Signal Transient Response

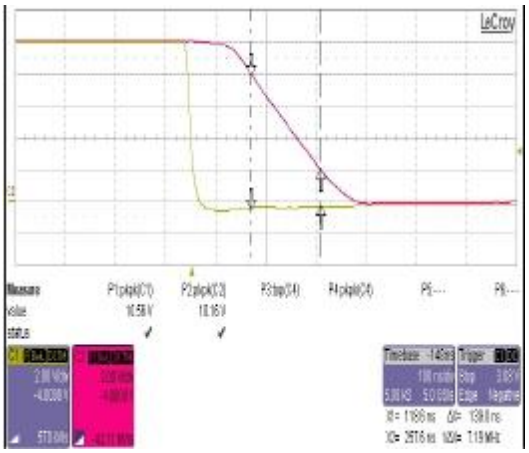


Figure (e) Large Signal Transient Response

APPLICATIONS INFORMATION

Product Description

The LP6291 rail-to-rail one channel amplifier is built on an advanced high voltage CMOS process. It's beyond rails input capability and full swing of output range makes itself an ideal amplifier for use in a wide range of general-purpose applications. The features of 40V/μs high slew rate, fast settling time, 30MHz of GBWP as well as high output driving capability have proven the LP6291 a good voltage reference buffer in TFT-LCD for grayscale reference applications. High phase margin and extremely low power consumption make the LP6291 ideal for connected in voltage follower mode for low power high drive applications.

Supply Voltage, Input Range and Output Swing

The LP6291 could be operated with a single nominal wide supply voltage ranging from 6V to 18V with stable performance over operating temperature of -40°C to +85°C. With 500mV greater than rail-to-rail input common mode voltage range and 70dB of Common Mode Rejection Ratio, the LP6291 allows a wide range sensing among many Applications without having any concerns over Exceeding the range and no compromise in accuracy. The output swings of the LP6291 typically extend to within 80mV of positive and negative supply rails with load currents of 5mA. The output voltage swing can be even closer to the supply rails by merely decreasing the load current. Figure 1 shows the input and output waveforms for The device in the unity-gain configuration. The amplifier is operated under ±5V supply with a 10KΩ load connected to GND. The input is a 10Vp-p sinusoid. An Approximately 9.985 Vp-p of output voltage swing can be easily achieved. .

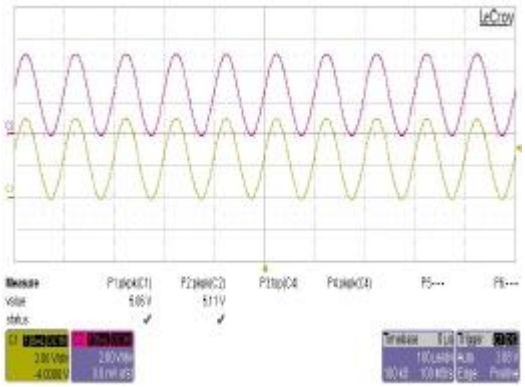


Figure 1. Operation with Rail-to-Rail Input and Output

Output Short Circuit Current Limit

A +/-350mA short circuit current will be limited by the LP6291 if the output is directly shorted to the positive or the negative supply. For an indefinitely output short circuit, the power dissipation could easily increase such that the device may be damaged. The internal metal interconnections are well designed to prevent the output continuous current from exceeding +/-100mA such that the maximum reliability can be well maintained.

Output Phase Reversal

The LP6291 is designed to prevent its output from being phase reversal as long as the input voltage is limited from VS- -0.5V to VS+ +0.5V. Figure 2 shows a photo of the device output with its input voltage driven beyond the supply rails. Although the phase of the device's output will not be reversed, the input's over-voltage should be avoided. An improper input voltage exceeds supply range by more than 0.6V may result in an over stress damage.

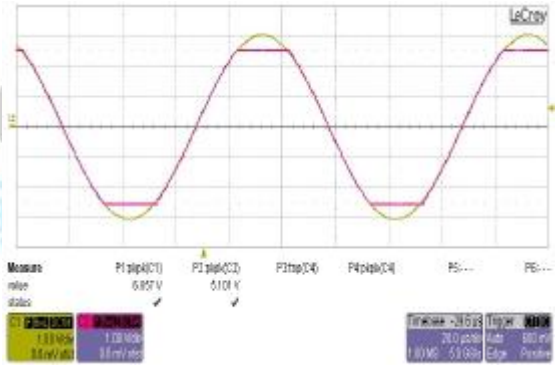


Figure 2. Operation with Beyond-the Rails Input

Power Dissipation

The LP6291 is designed for maximum output current capability. Even though momentary output shorted to ground causes little damage to device. For the high drive amplifier LP6291, it is possible To exceed the 'absolute-maximum junction . temperature' under certain load current conditions. Therefore, it is important to calculate the maximum junction temperature for the application to determine if load conditions need to be modified for theamplifier to remain in the safe operating area. .
The maximum power dissipation allowed in a package is determined according to:

$$P_{Dmax} = \frac{T_{Jmax} - T_{Amax}}{\Theta_{JA}}$$

Where:

T_{Jmax} = Maximum Junction Temperature

T_{Amax}= Maximum Ambient Temperature
Θ_{JA} = Thermal Resistance of the Package
P_{Dmax} = Maximum Power Dissipation in the Package.

The maximum power dissipation actually produced by an IC is the total quiescent supply current times the total power supply voltage, plus the power in the IC due to the loads, or:
$P_{Dmax} = \sum_i [VS * I_{Smax} + (VS+ - VO) * I_L]$
When sourcing, and
$P_{Dmax} = \sum_i [VS * I_{Smax} + (VO - VS-) * I_L]$
When sinking.
Where:
i = 1 to 1
VS = Total Supply Voltage
I_{Smax} = Maximum Supply Current Per Amplifier
VO = Maximum Output Voltage of the Application
I_L= Load current
R_L= Load Resistance = $(VS+ - VO)/I_L = (VO - VS-)/ I_L$

A calculation for R_L to prevent device from overheat can be easily solved by setting the two P_{Dmax} equations equal to each other.

Driving Capacitive Loads

The LP6291 is designed to drive a wide range of capacitive loads. In addition, the output current handling capability of the device allows for good slewing characteristics even with large capacitive loads. The combination of these features make the LP6291 ideally for applications such as TFT LCD panel grayscale reference voltage buffers, ADC input amplifiers, etc.

As load capacitance increases, however, the -3dB bandwidth of the device will decrease and the peaking increase. Depending on the application, it must be necessary to reduce peaking and to improve device stability. To improve device stability, a small value of series resistor (usually between 5Ωand 50Ω) must be placed in series with the output. The advantage is that it improves the settling and overshooting performance with very large capacitive loads. Figure 3. shows the typical application configuration.

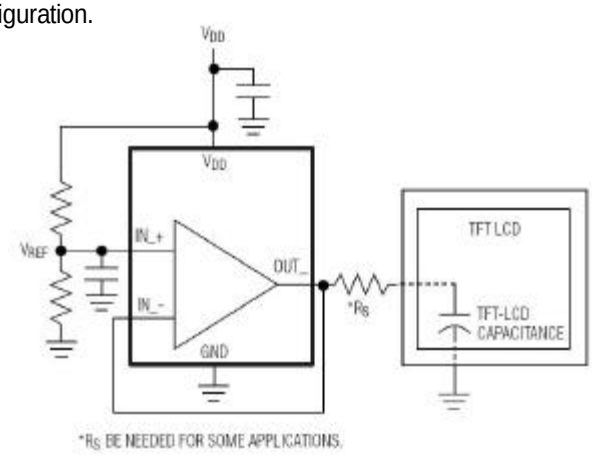


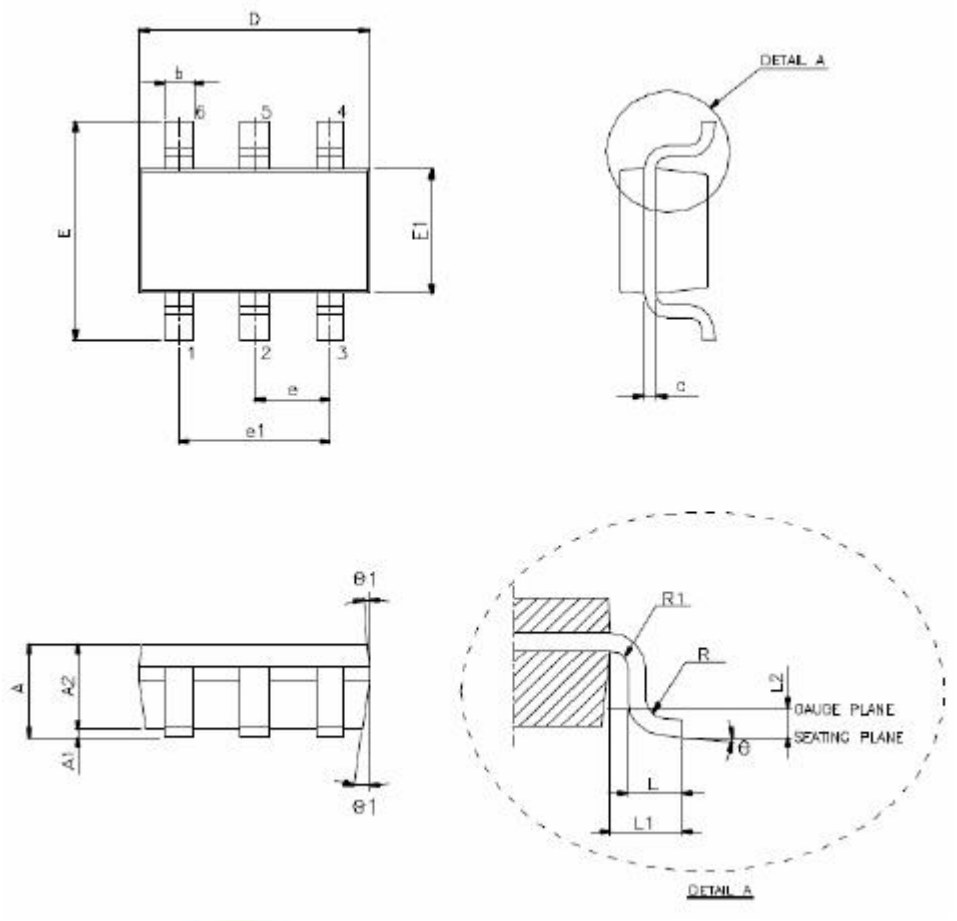
Figure 3. Typical Application Configuration.

Power Supply Bypassing and Printed Circuit Board Layout

With high phase margin, the LP6291 performs stable gain at high frequency. Like any high-frequency device, good layout of the printed circuit board usually comes with optimum performance. Ground plane construction is highly recommended, lead lengths should be as short as possible and the power supply pins must be well bypassed to reduce the risk of oscillation. For normal single supply operation, where the VS- pin is connected to ground, a 0.1 µF ceramic capacitor should be placed from VS+ pin to VS- pin as a bypassing capacitor. A 4.7µF tantalum capacitor should then be connected in parallel, placed in the region of the amplifier. One 4.7µF capacitor may be used for multiple devices. This same capacitor combination should be placed at each supply pin to ground if split supplies are to be used.

Packaging Information

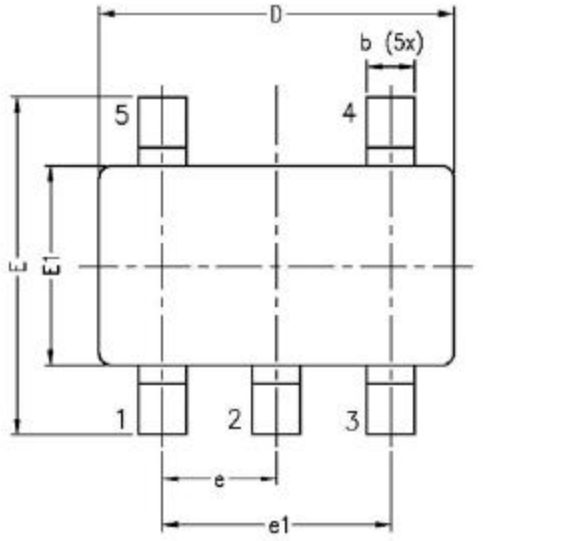
SOT23-6

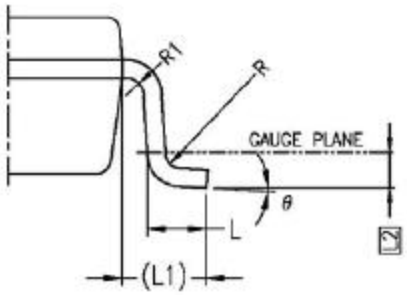


VARIATION(ALL DIMENSIONS SHOWN IN MM)

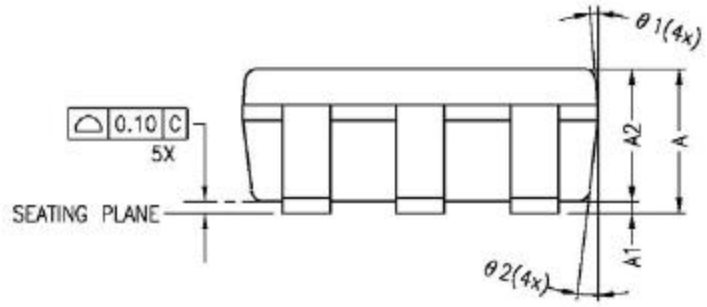
SYMBOL	MIN.	NOM.	MAX.
A	–	–	1.45
A1	–	–	0.15
A2	0.90	1.15	1.30
b	0.30	–	0.50
c	0.08	–	0.22
D		2.90 BSC.	
E		2.80 BSC.	
E1		1.60 BSC.	
e		0.95 BSC	
e1		1.90 BSC.	
L	0.30	0.45	0.60
L1		0.60 REF.	
L2		0.25 BSC.	
R	0.10	–	–
R1	0.10	–	0.25
θ	0°	4°	8°
θ1	5°	10°	15°

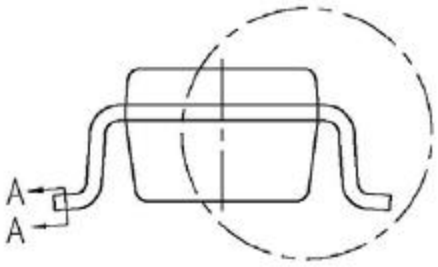
SOT23-5





VIEW B



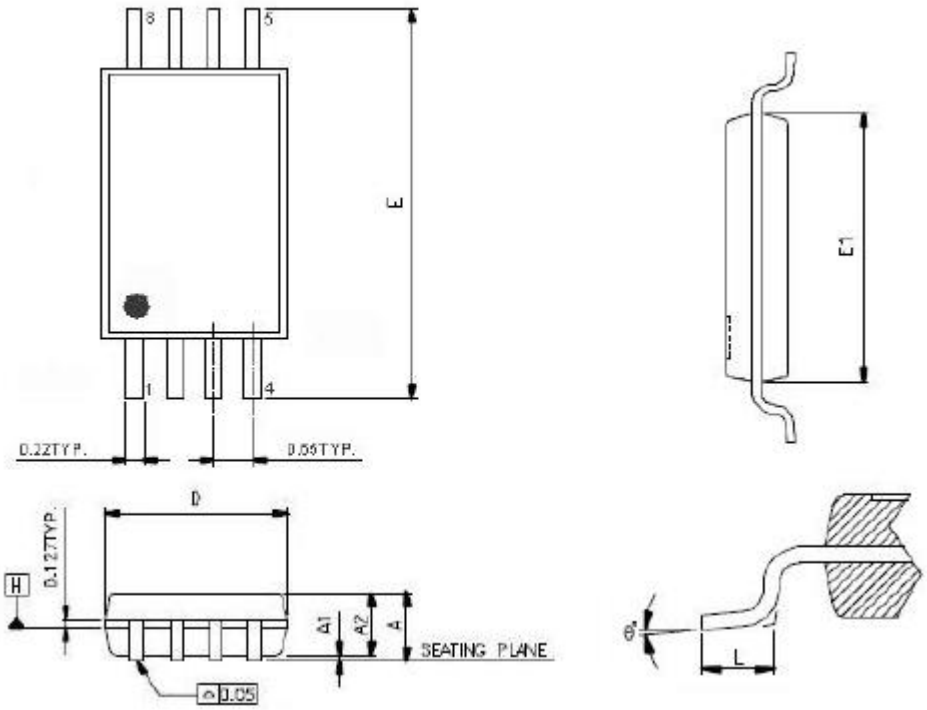


SEE VIEW B

VARIATION(ALL DIMENSIONS SHOWN IN MM)

SYMBOL	MIN.	NOM.	MAX.
A	–	–	1.45
A1	–	–	0.15
A2	0.90	1.15	1.30
b	0.30	–	0.50
c	0.08	–	0.22
D		2.90 BSC.	
E		2.80 BSC.	
E1		1.60 BSC.	
e		0.95 BSC	
e1		1.90 BSC.	
L	0.30	0.45	0.60
L1		0.60 REF.	
L2		0.25 BSC.	
R	0.10	–	–
R1	0.10	–	0.25
θ	0°	4°	8°
θ1	5°	10°	15°

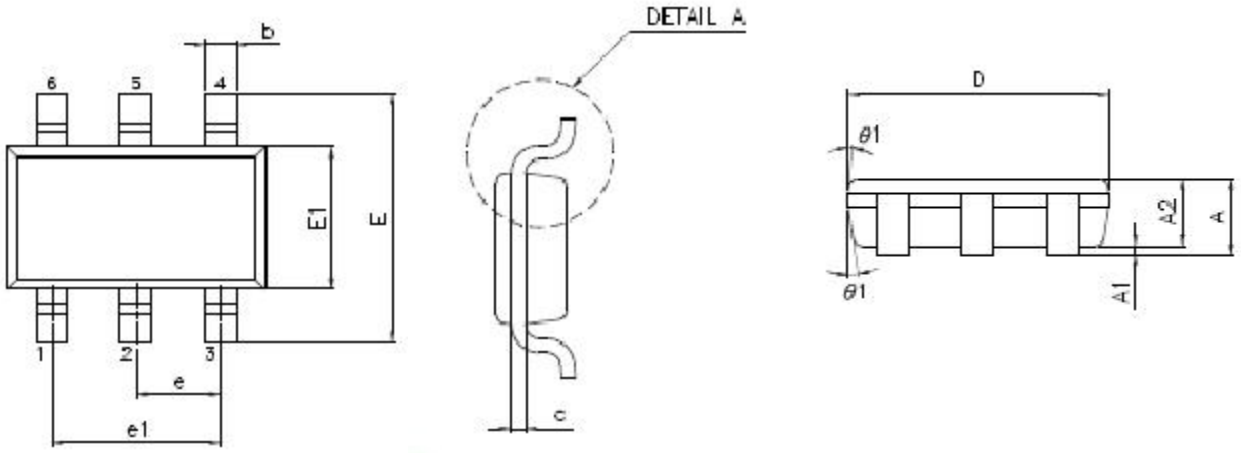
TSSOP-8

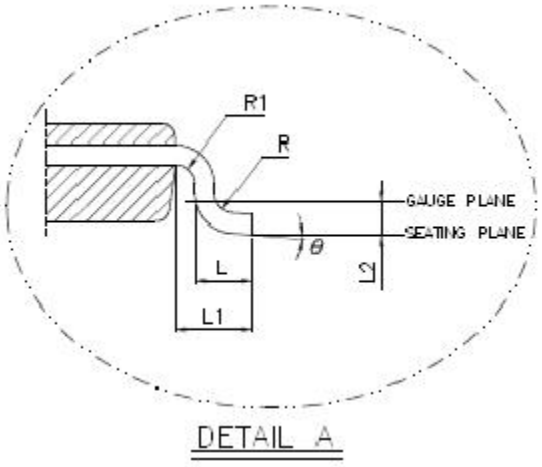


SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.20
A1	0.05	–	0.15
A2	0.96	1.01	1.06
D	2.90	3.00	3.10
E		6.40 BSC	
E1	4.30	4.40	4.50
L	0.45	0.60	0.75
θ°	0	–	8

UNIT : MM

TSOT23-6



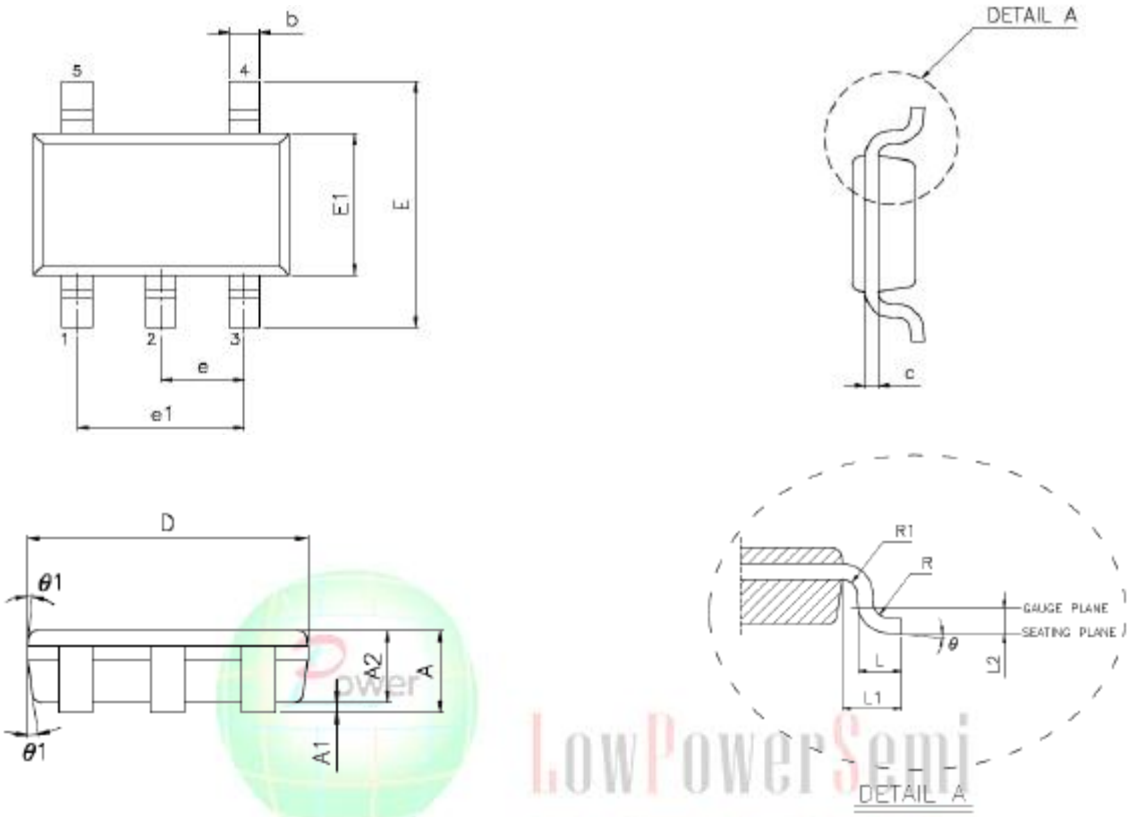


VARIATION(ALL DIMENSIONS SHOWN IN MM)

SYMBOL	MIN.	NOM.	MAX.
A	0.750	—	0.800
A1	0.000	—	0.050
A2	0.700	0.750	0.775
b	0.350	—	0.500
c	0.100	—	0.200
D	2.800	2.900	3.000
E	2.600	2.800	3.000
E1	1.500	1.600	1.700
e	0.950 BSC		
e1	1.900 BSC		
L	0.370	0.450	0.600
L1	0.600 REF		
L2	0.250 BSC		
R	0.100	—	—
R1	0.100	—	0.250
θ	0°	4°	8°
θ1	4°	10°	12°

NOTE :
1. JEDEC OUTLINE : N/A.

TSOT23-5



SYMBOL	MIN.	NOM.	MAX.
A	0.750	-	0.800
A1	0.000	-	0.050
A2	0.700	0.750	0.775
b	0.350	-	0.500
c	0.100	-	0.200
D	2.800	2.900	3.000
E	2.600	2.800	3.000
E1	1.500	1.600	1.700
e	0.950 BSC		
e1	1.900 BSC		
L	0.370	0.450	0.600
L1	0.600 REF		
L2	0.250 BSC		
R	0.100	-	-
R1	0.100	-	0.250
θ	0°	4°	8°
θ1	4°	10°	12°

单击下面可查看定价，库存，交付和生命周期等信息

>>LOW POWER(微源半导体)