

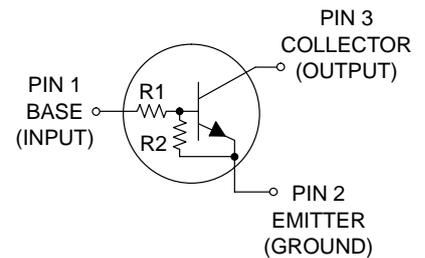
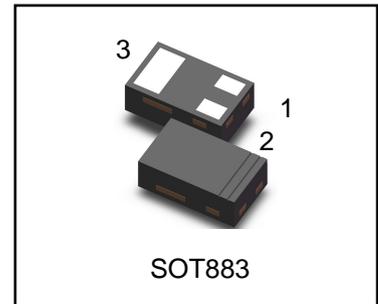
# Bias Resistor Transistors

## NPN Silicon Surface Mount Transistors with Monolithic Bias Resistor Network

### LDTC114EN3T5G Series S-LDTC114EN3T5G Series

This new series of digital transistors is designed to replace a single device and its external resistor bias network. The BRT (Bias Resistor Transistor) contains a single transistor with a monolithic bias network consisting of two resistors; a series base resistor and a base-emitter resistor. The BRT eliminates these individual components by integrating them into a single device. The use of a BRT can reduce both system cost and board space. The device is housed in the SC-89 package which is designed for low power surface mount applications.

- Simplifies Circuit Design
- Reduces Board Space
- Reduces Component Count
- The SOT883 package can be soldered using wave or reflow. The modified gull-winged leads absorb thermal stress during soldering eliminating the possibility of damage to the die.
- We declare that the material of product compliance with RoHS requirements.
- S- Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable.



#### MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Collector-Base Voltage	$V_{CB0}$	50	Vdc
Collector-Emitter Voltage	$V_{CEO}$	50	Vdc
Collector Current	$I_C$	100	mAdc

#### THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Total Device Dissipation FR-5 Board, (1) $T_A = 25^\circ\text{C}$	$P_D$	250	mW
Derate above $25^\circ\text{C}$		4	mW/ $^\circ\text{C}$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	500	$^\circ\text{C}/\text{W}$
Junction and Storage Temperature	$T_J, T_{stg}$	-55 to +150	$^\circ\text{C}$

1. FR-5 = 1.0 x 0.75 x 0.062 in.

## LDTC114EN3T5G Series; S-LDTC114EN3T5G Series

### ORDERING INFORMATION AND RESISTOR VALUES

Device	Marking	R1 (K)	R2 (K)	Package	Shipping <sup>†</sup>
LDTC114EN3T5G S-LDTC114EN3T5G	8A	10	10	SOT883	10000 Tape & Reel
LDTC124EN3T5G S-LDTC124EN3T5G	8B	22	22	SOT883	10000 Tape & Reel
LDTC144EN3T5G S-LDTC144EN3T5G	8C	47	47	SOT883	10000 Tape & Reel
LDTC114YN3T5G S-LDTC114YN3T5G	8D	10	47	SOT883	10000 Tape & Reel
LDTC114TN3T5G S-LDTC114TN3T5G	94	10	∞	SOT883	10000 Tape & Reel
LDTC143TN3T5G S-LDTC143TN3T5G	8F	4.7	∞	SOT883	10000 Tape & Reel
LDTC123EN3T5G S-LDTC123EN3T5G	8H	2.2	2.2	SOT883	10000 Tape & Reel
LDTC143EN3T5G S-LDTC143EN3T5G	8J	4.7	4.7	SOT883	10000 Tape & Reel
LDTC143ZN3T5G S-LDTC143ZN3T5G	8K	4.7	47	SOT883	10000 Tape & Reel
LDTC124XN3T5G S-LDTC124XN3T5G	8L	22	47	SOT883	10000 Tape & Reel
LDTC123JN3T5G S-LDTC123JN3T5G	8M	2.2	47	SOT883	10000 Tape & Reel
LDTC115EN3T5G S-LDTC115EN3T5G	8N	100	100	SOT883	10000 Tape & Reel
LDTC144WN3T5G S-LDTC144WN3T5G	8P	47	22	SOT883	10000 Tape & Reel

### ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>					
Collector–Base Cutoff Current (V <sub>CB</sub> = 50 V, I <sub>E</sub> = 0)	I <sub>CBO</sub>	–	–	100	nAdc
Collector–Emitter Cutoff Current (V <sub>CE</sub> = 50 V, I <sub>B</sub> = 0)	I <sub>CEO</sub>	–	–	500	nAdc
Emitter–Base Cutoff Current (V <sub>EB</sub> = 6.0 V, I <sub>C</sub> = 0)	I <sub>EBO</sub>	–	–	0.5	mAdc
		–	–	0.2	
		–	–	0.1	
		–	–	0.2	
		–	–	0.9	
		–	–	1.9	
		–	–	2.3	
		–	–	1.5	
		–	–	0.18	
		–	–	0.13	
		–	–	0.2	
		–	–	0.05	
		–	–	0.13	
Collector–Base Breakdown Voltage (I <sub>C</sub> = 10 μA, I <sub>E</sub> = 0)	V <sub>(BR)CBO</sub>	50	–	–	Vdc
Collector–Emitter Breakdown Voltage (Note 2) (I <sub>C</sub> = 2.0 mA, I <sub>B</sub> = 0)	V <sub>(BR)CEO</sub>	50	–	–	Vdc

2. Pulse Test: Pulse Width < 300 μs, Duty Cycle < 2.0%

# LDTCC114EN3T5G Series;S-LDTCC114EN3T5G Series

Characteristic	Symbol	Min	Typ	Max	Unit	
<b>ON CHARACTERISTICS</b> (Note 3)						
DC Current Gain ( $V_{CE} = 10\text{ V}$ , $I_C = 5.0\text{ mA}$ )	LDTCC114EN3T5G LDTCC124EN3T5G LDTCC144EN3T5G LDTCC114YN3T5G LDTCC114TN3T5G LDTCC143TN3T5G LDTCC123EN3T5G LDTCC143EN3T5G LDTCC143ZN3T5G LDTCC124XN3T5G LDTCC123JN3T5G LDTCC115EN3T5G LDTCC144WN3T5G	$h_{FE}$	35 60 80 80 160 160 8.0 15 80 80 80 80 80	60 100 140 140 350 350 15 30 200 150 140 150 140	– – – – – – – – – – – – –	
Collector–Emitter Saturation Voltage ( $I_C = 10\text{ mA}$ , $I_B = 0.3\text{ mA}$ ) ( $I_C = 10\text{ mA}$ , $I_B = 5\text{ mA}$ ) LDTCC123EN3T5G ( $I_C = 10\text{ mA}$ , $I_B = 1\text{ mA}$ ) LDTCC143TN3T5G/LDTCC114TN3T5G/ LDTCC143EN3T5G/LDTCC143ZN3T5G/LDTCC124XN3T5G		$V_{CE(sat)}$	–	–	0.25	Vdc
Output Voltage (on) ( $V_{CC} = 5.0\text{ V}$ , $V_B = 2.5\text{ V}$ , $R_L = 1.0\text{ k}\Omega$ )  ( $V_{CC} = 5.0\text{ V}$ , $V_B = 3.5\text{ V}$ , $R_L = 1.0\text{ k}\Omega$ ) ( $V_{CC} = 5.0\text{ V}$ , $V_B = 5.5\text{ V}$ , $R_L = 1.0\text{ k}\Omega$ ) ( $V_{CC} = 5.0\text{ V}$ , $V_B = 4.0\text{ V}$ , $R_L = 1.0\text{ k}\Omega$ )	LDTCC114EN3T5G LDTCC124EN3T5G LDTCC114YN3T5G LDTCC114TN3T5G LDTCC143TN3T5G LDTCC123EN3T5G LDTCC143EN3T5G LDTCC143ZN3T5G LDTCC124XN3T5G LDTCC123JN3T5G LDTCC144EN3T5G LDTCC115EN3T5G LDTCC144WN3T5G	$V_{OL}$	– – – – – – – – – – – – –	– – – – – – – – – – – – –	0.2 0.2 0.2 0.2 0.2 0.2 0.2 0.2 0.2 0.2 0.2 0.2 0.2	Vdc
Output Voltage (off) ( $V_{CC} = 5.0\text{ V}$ , $V_B = 0.5\text{ V}$ , $R_L = 1.0\text{ k}\Omega$ ) ( $V_{CC} = 5.0\text{ V}$ , $V_B = 0.25\text{ V}$ , $R_L = 1.0\text{ k}\Omega$ )	LDTCC143TN3T5G LDTCC143ZN3T5G LDTCC114TN3T5G LDTCC115EN3T5G	$V_{OH}$	4.9	–	–	Vdc

3. Pulse Test: Pulse Width < 300  $\mu\text{s}$ , Duty Cycle < 2.0%

## ELECTRICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ unless otherwise noted) (Continued)

Characteristic	Symbol	Min	Typ	Max	Unit	
Input Resistor	LDTCC114EN3T5G LDTCC124EN3T5G LDTCC144EN3T5G LDTCC114YN3T5G LDTCC114TN3T5G LDTCC143TN3T5G LDTCC123EN3T5G LDTCC143EN3T5G LDTCC143ZN3T5G LDTCC124XN3T5G LDTCC123JN3T5G LDTCC115EN3T5G LDTCC144WN3T5G	$R_1$	7.0 15.4 32.9 7.0 7.0 3.3 1.5 3.3 3.3 15.4 1.54 70 32.9	10 22 47 10 10 4.7 2.2 4.7 4.7 22 2.2 100 47	13 28.6 61.1 13 13 6.1 2.9 6.1 6.1 28.6 2.86 130 61.1	$\text{k}\Omega$
Resistor Ratio	LDTCC114EN3T5G/LDTCC124EN3T5G/ LDTCC144EN3T5G/LDTCC115EN3T5G LDTCC114YN3T5G LDTCC143TN3T5G/LDTCC114TN3T5G LDTCC123EN3T5G/LDTCC143EN3T5G LDTCC143ZN3T5G LDTCC124XN3T5G LDTCC123JN3T5G LDTCC144WN3T5G	$R_1/R_2$	0.8 0.17 – 0.8 0.055 0.38 0.038 1.7	1.0 0.21 – 1.0 0.1 0.47 0.047 2.1	1.2 0.25 – 1.2 0.185 0.56 0.056 2.6	

# LDTTC114EN3T5G Series; S-LDTTC114EN3T5G Series

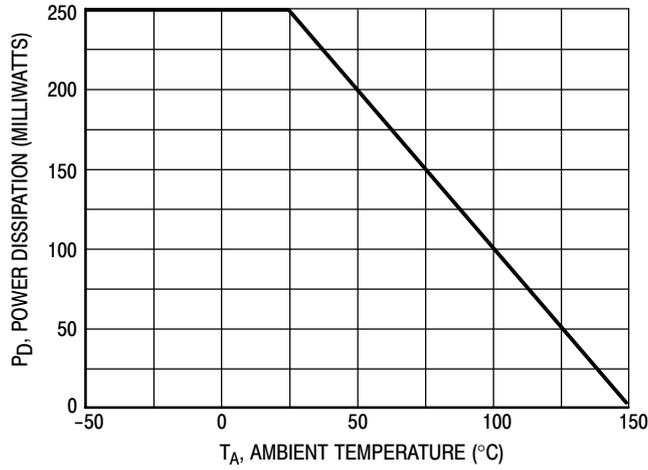


Figure 1. Derating Curve

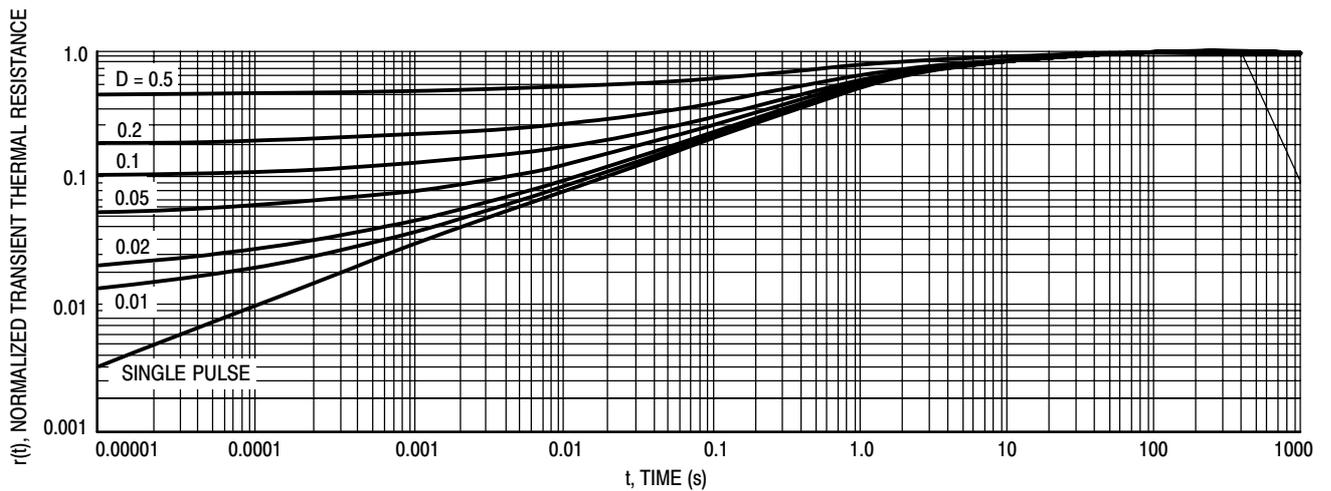


Figure 2. Normalized Thermal Response

# LDT C114EN3T5G Series; S-LDT C114EN3T5G Series

## TYPICAL ELECTRICAL CHARACTERISTICS – LDT C114EN3T5G

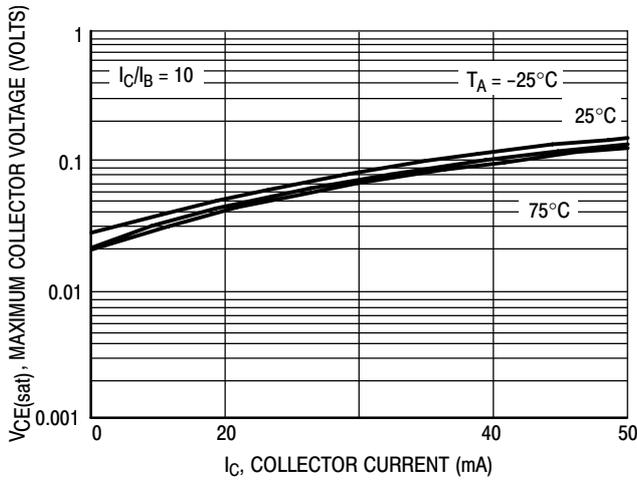


Figure 3.  $V_{CE(sat)}$  versus  $I_C$

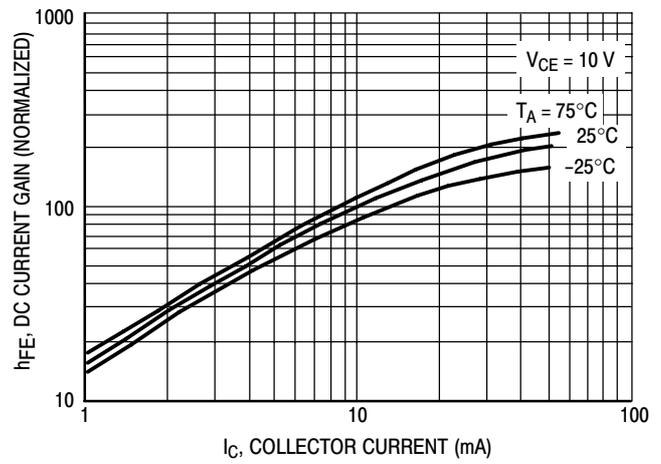


Figure 4. DC Current Gain

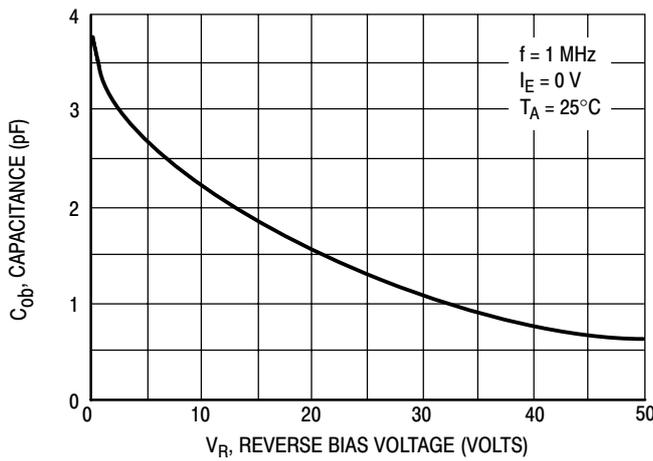


Figure 5. Output Capacitance

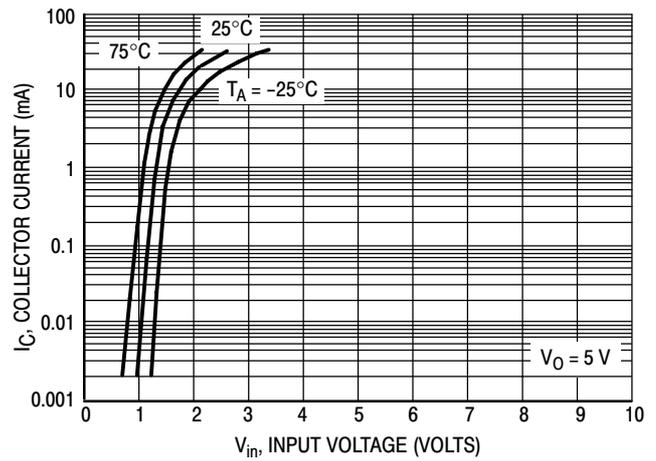


Figure 6. Output Current versus Input Voltage

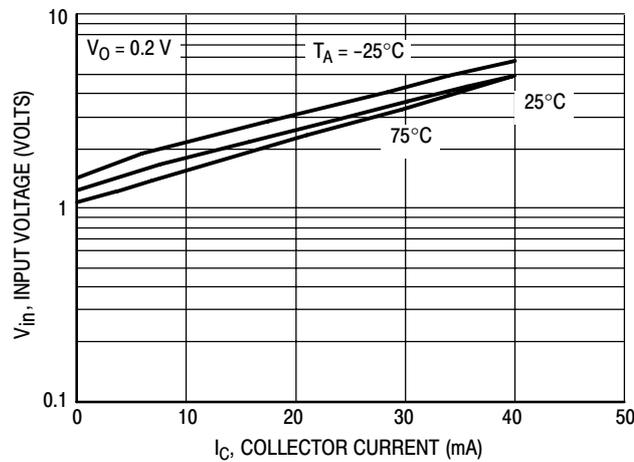


Figure 7. Input Voltage versus Output Current

# LDT C114EN3T5G Series; S-LDT C114EN3T5G Series

## TYPICAL ELECTRICAL CHARACTERISTICS – LDT C123EN3T5G

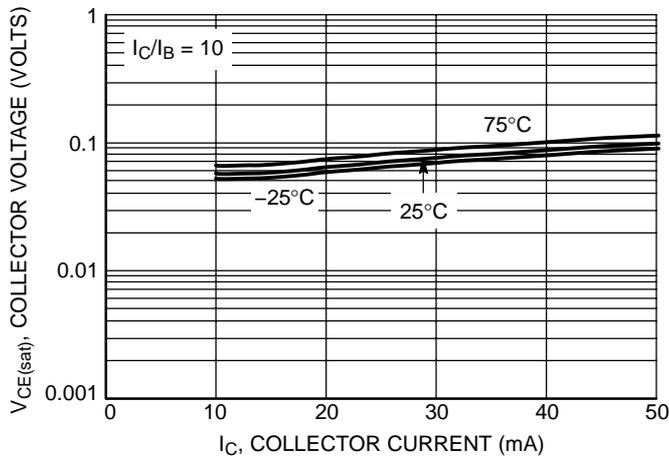


Figure 8.  $V_{CE(sat)}$  versus  $I_C$

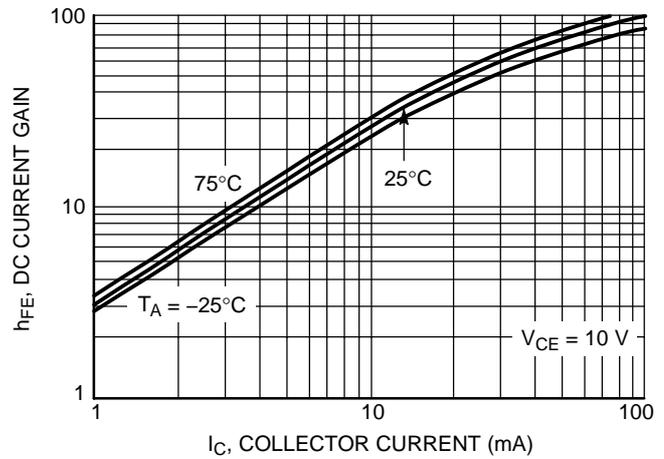


Figure 9. DC Current Gain

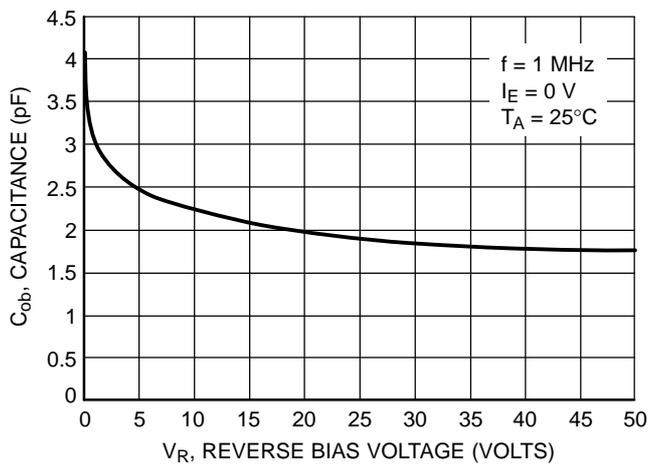


Figure 10. Output Capacitance

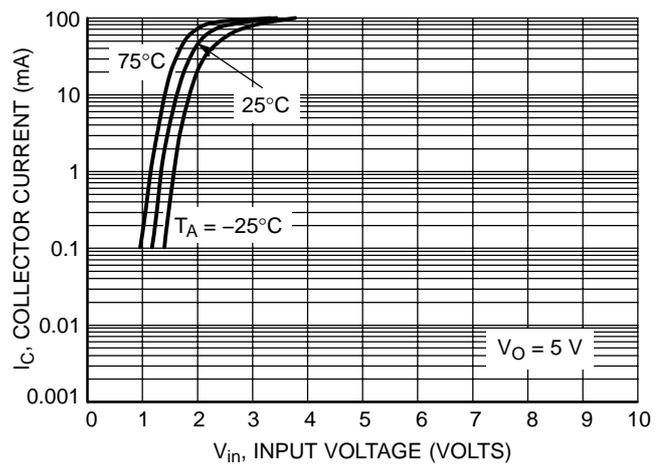


Figure 11. Output Current versus Input Voltage

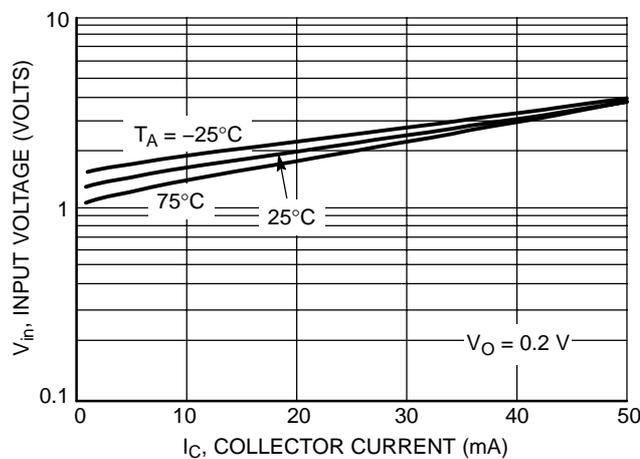


Figure 12. Input Voltage versus Output Current

# LDTCC114EN3T5G Series; S-LDTCC114EN3T5G Series

## TYPICAL ELECTRICAL CHARACTERISTICS – LDTCC124EN3T5G

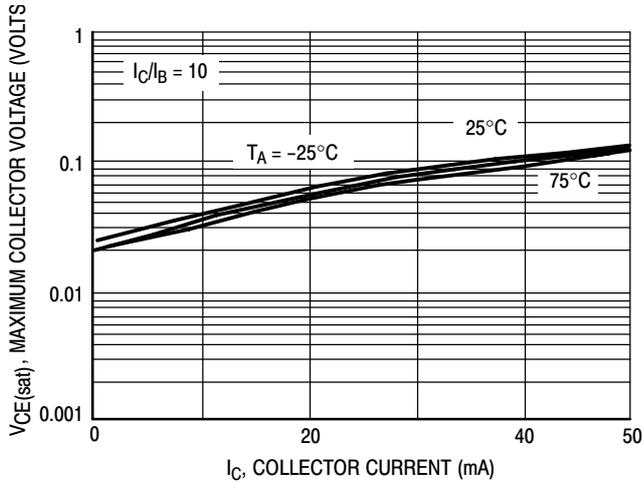


Figure 13.  $V_{CE(sat)}$  versus  $I_C$

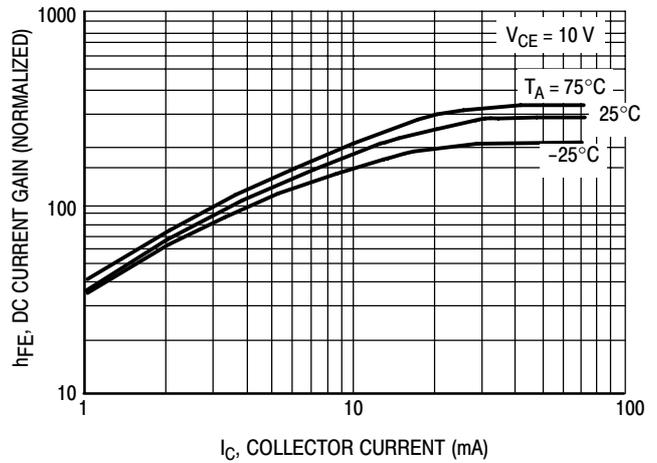


Figure 14. DC Current Gain

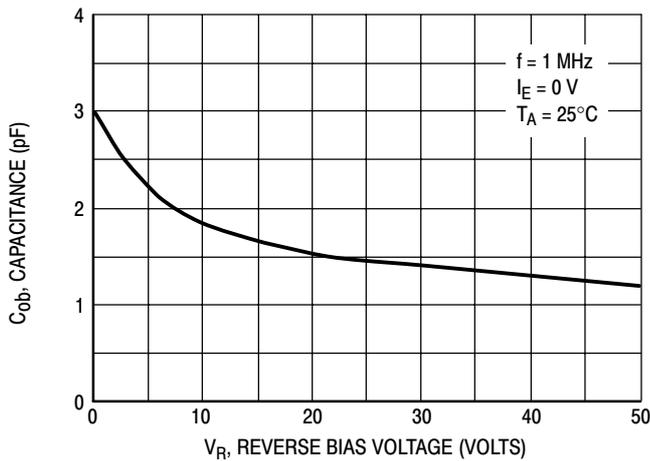


Figure 15. Output Capacitance

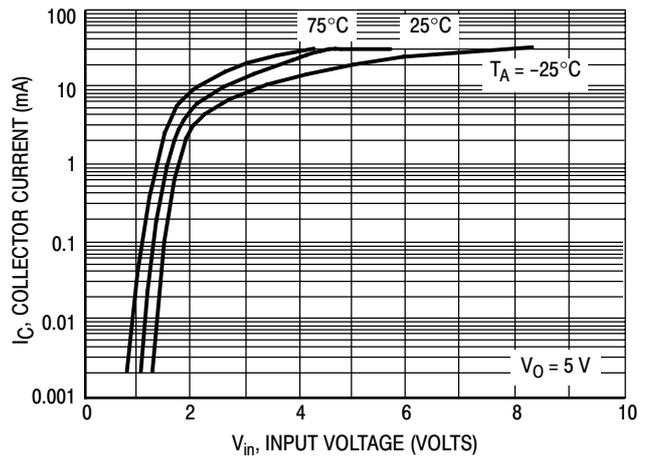


Figure 16. Output Current versus Input Voltage

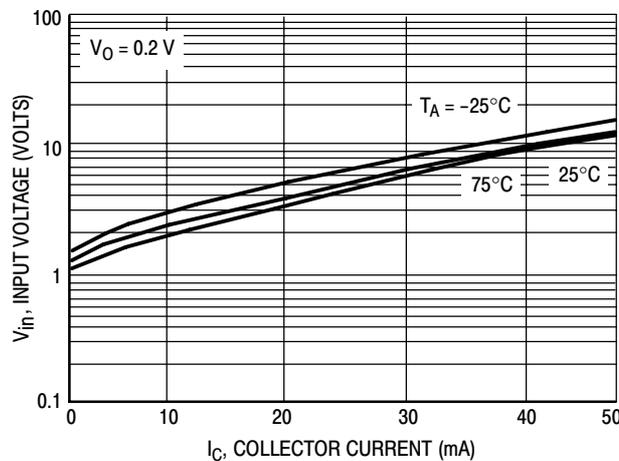


Figure 17. Input Voltage versus Output Current

# LDTC114EN3T5G Series; S-LDTC114EN3T5G Series

## TYPICAL ELECTRICAL CHARACTERISTICS – LDTC144EN3T5G

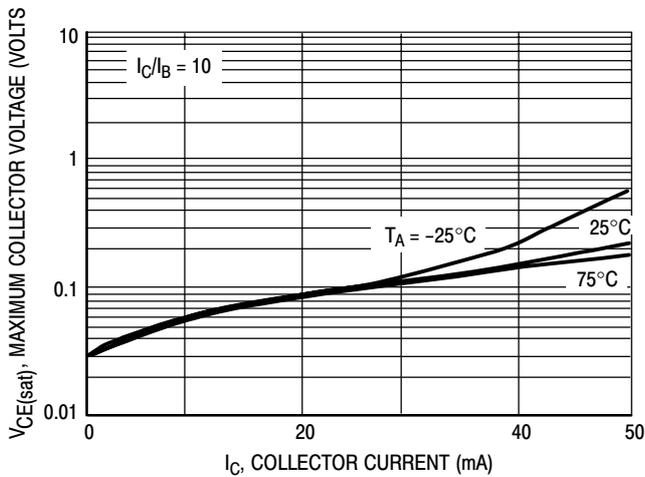


Figure 18.  $V_{CE(sat)}$  versus  $I_C$

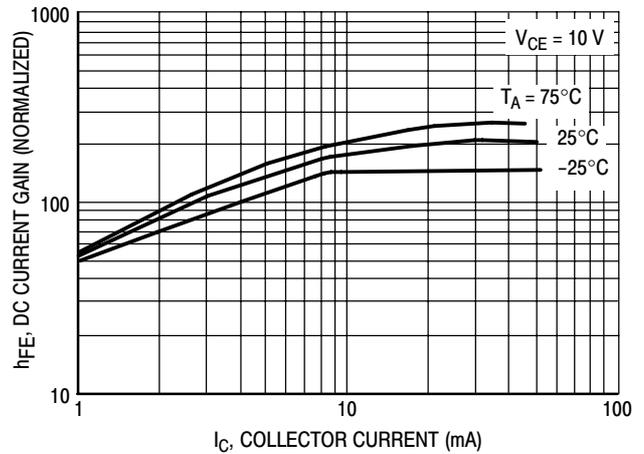


Figure 19. DC Current Gain

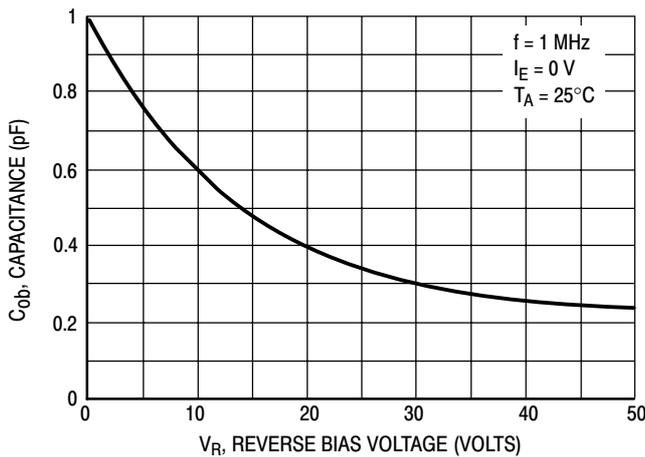


Figure 20. Output Capacitance

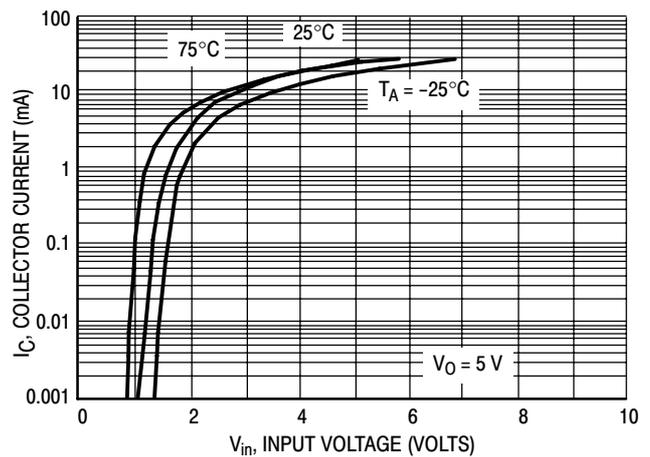


Figure 21. Output Current versus Input Voltage

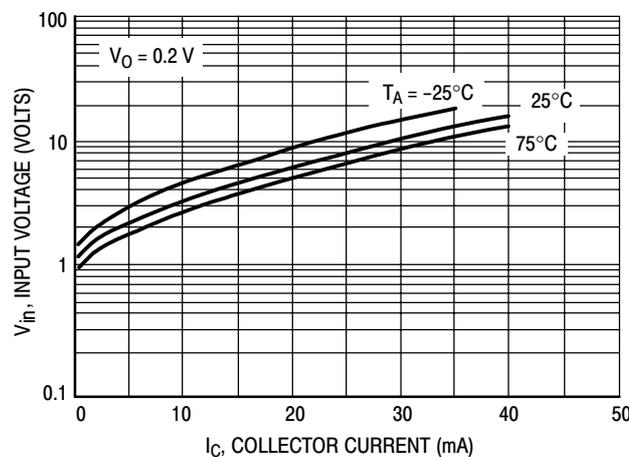


Figure 22. Input Voltage versus Output Current

# LDT C114EN3T5G Series; S-LDT C114EN3T5G Series

## TYPICAL ELECTRICAL CHARACTERISTICS – LDT C114YN3T5G

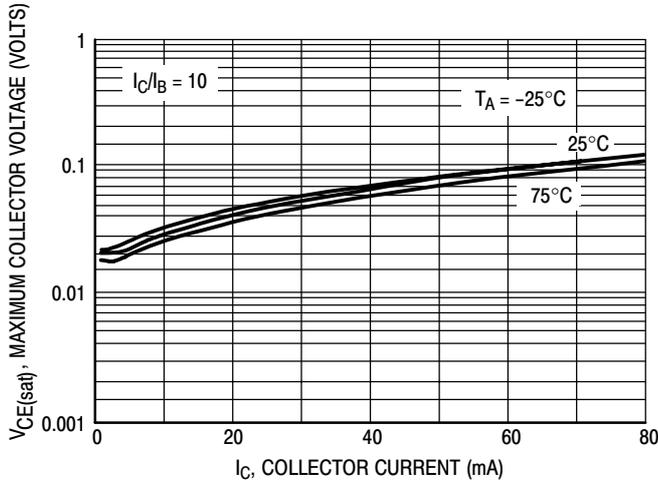


Figure 23.  $V_{CE(sat)}$  versus  $I_C$

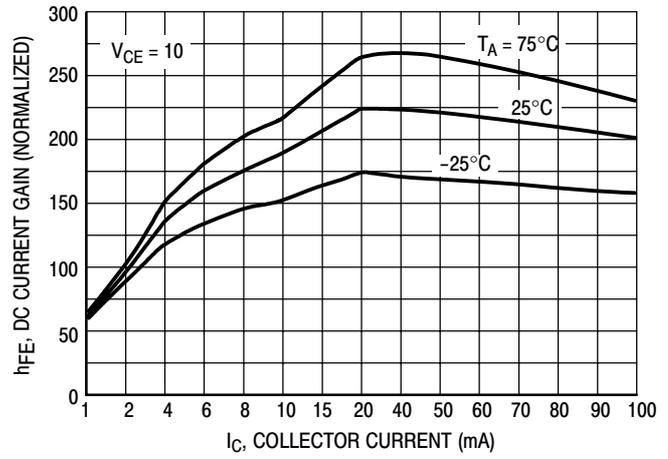


Figure 24. DC Current Gain

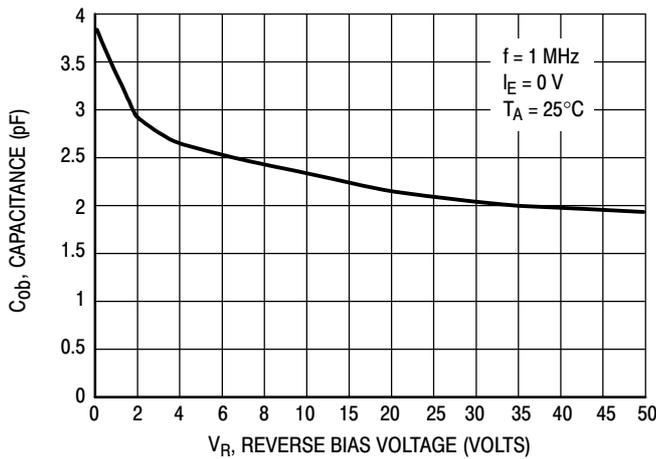


Figure 25. Output Capacitance

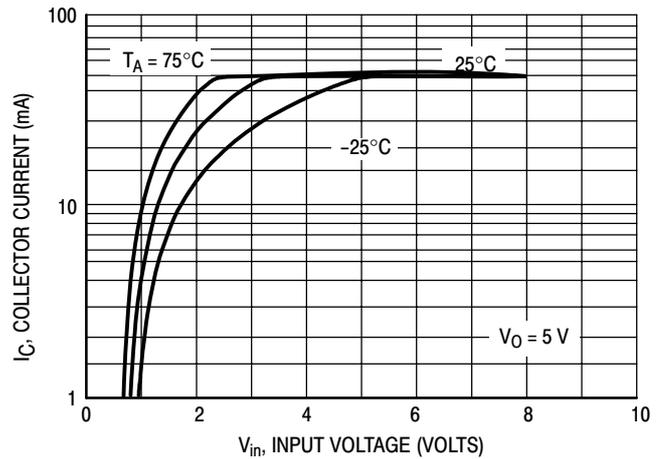


Figure 26. Output Current versus Input Voltage

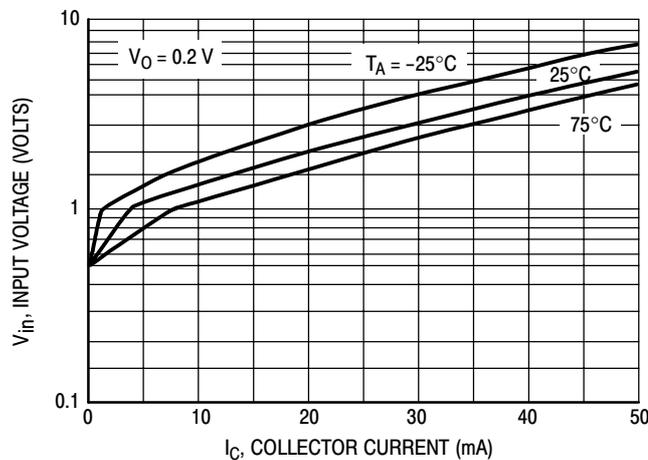


Figure 27. Input Voltage versus Output Current

# LDTTC114EN3T5G Series;S-LDTTC114EN3T5G Series

## TYPICAL APPLICATIONS FOR NPN BRTs

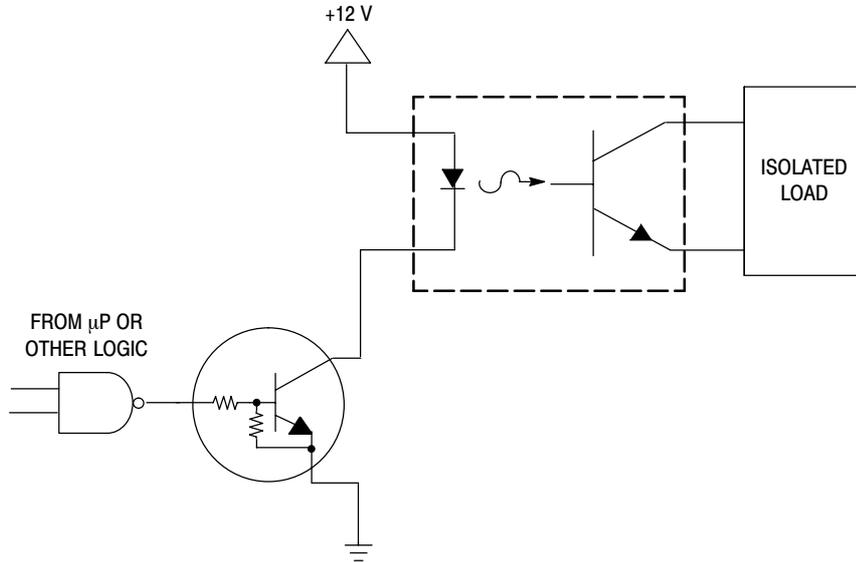


Figure 28. Level Shifter: Connects 12 or 24 Volt Circuits to Logic

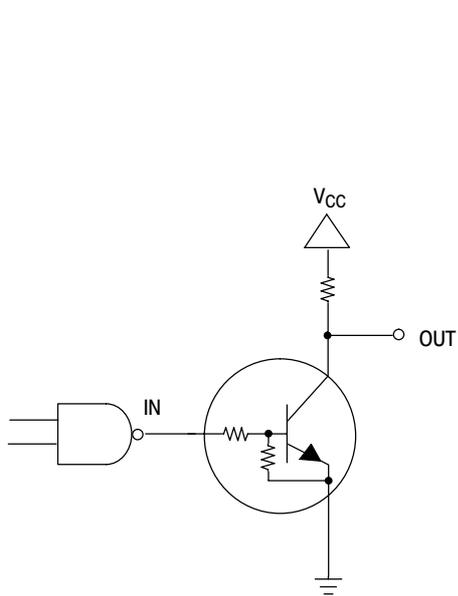


Figure 29. Open Collector Inverter: Inverts the Input Signal

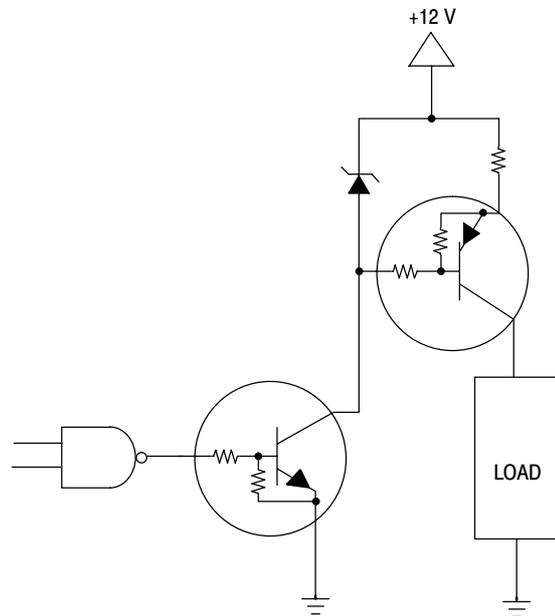
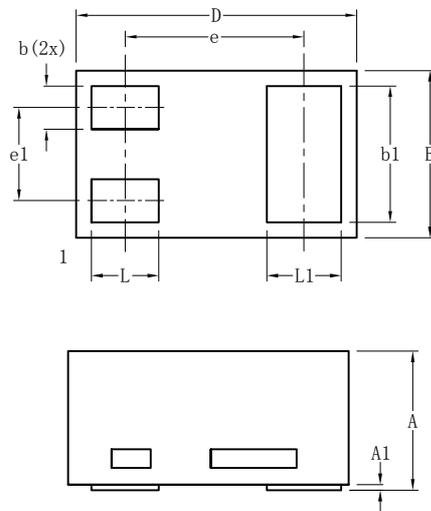


Figure 30. Inexpensive, Unregulated Current Source

# LDTTC114EN3T5G Series; S-LDTTC114EN3T5G Series

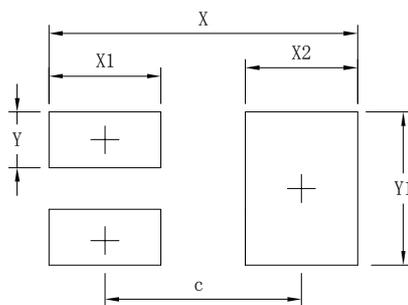
## SOT883

### Package Outline Dimensions



SOT883A			
Dim	Min	Typ	Max
D	0.95	1.00	1.05
E	0.50	0.60	0.65
e	-	0.64	-
e1	-	0.34	-
L	0.19	0.24	0.29
L1	0.22	0.27	0.32
b	0.10	0.15	0.20
b1	0.44	0.49	0.54
A	0.43	0.48	0.53
A1	0	-	0.05
All Dimensions in mm			

### Suggested Pad Layout



Dimensions	Value (in mm)
c	0.70
X	1.10
X1	0.40
X2	0.40
Y	0.20
Y1	0.55

单击下面可查看定价，库存，交付和生命周期等信息

[>>LRC\(乐山无线电\)](#)