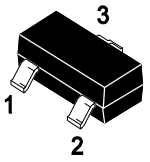
LN2502LT1G

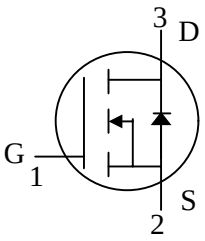
20V N-Channel Enhancement-Mode MOSFET



SOT23(TO-236)

1. FEATURES

- VDS= 20V
- RDS(ON), VGS@2.5V, IDS@5.2A = 50mΩ
- RDS(ON), VGS@4.5V, IDS@6A = 40mΩ
- We declare that the material of product compliance with RoHS requirements and Halogen Free.



2. DEVICE MARKING AND ORDERING INFORMATION

Device	Marking	Shipping
LN2502LT1G	N25	3000/Tape&Reel
LN2502LT3G	N25	10000/Tape&Reel

3. MAXIMUM RATINGS(Ta = 25ºC)

Parameter	Symbol	Limits	Unit
Drain–Source Voltage	VDSS	20	V
Gate–to–Source Voltage – Continuous	VGS	±12	V
Drain Current			A
– Continuous TA = 25°C	ID	6	
– Pulsed(Note 1)	IDM	33	
Maximum Power Dissipation	PD	1	W
Operating Junction and Storage Temperature Range	TJ/Tstg	-55~+150	℃

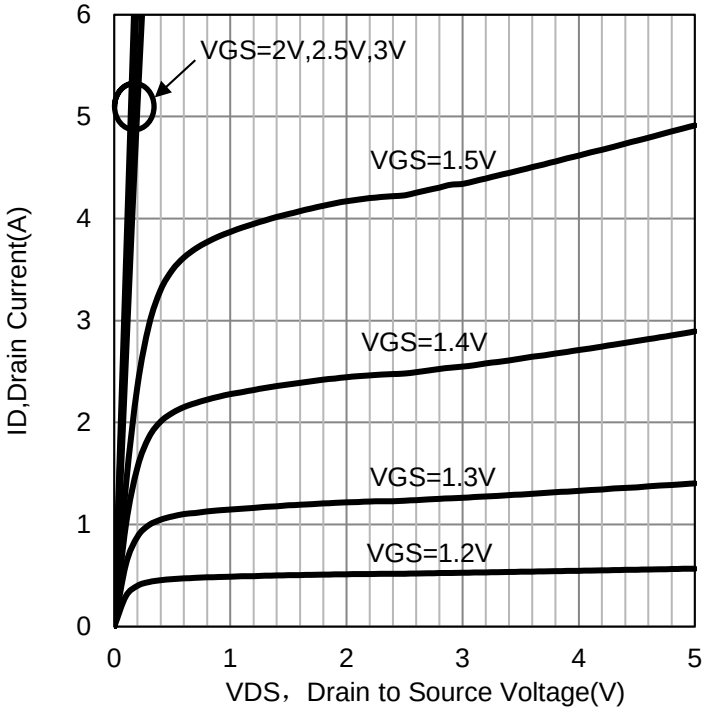
1. Repetitive Rating: Pulse width limited by the maximum junction temperature

4. ELECTRICAL CHARACTERISTICS (Ta= 25°C)

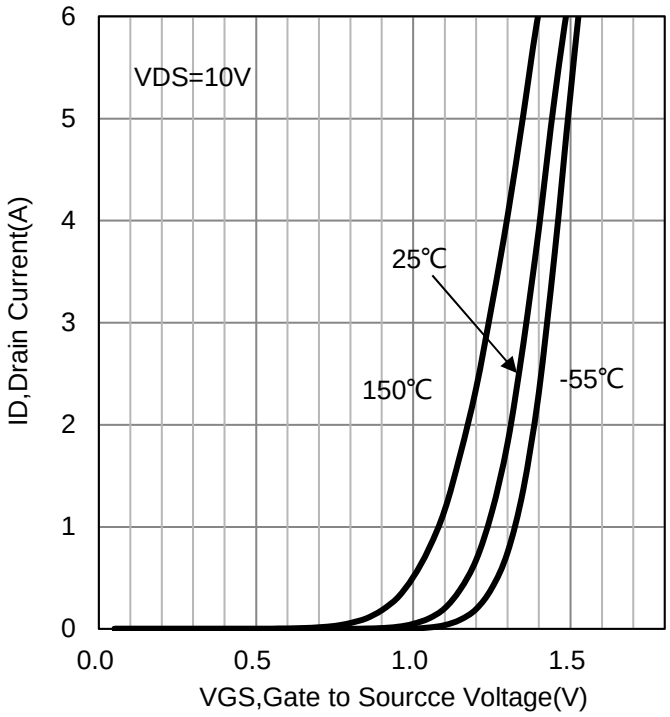
Characteristic		Symbol	Min.	Typ.	Max.	Unit
Static						
Drain–Source Breakdown Voltage (VGS = 0, ID = 250μA)		V(BR)DSS	20	-	-	V
Zero Gate Voltage Drain Current (VDS=20V, VGS=0V)		IDSS	-	-	1	μA
Gate–Body Leakage Current (VDS = 0 V, VGS = ±12 V)		IGSS	-	-	±100	nA
Forward Transconductance (VDS = 10 V, ID = 6 A)		gfs	-	5	-	S
Gate Threshold Voltage (VDS = VGS, ID = 250μA)		VGS(th)	0.4	-	0.9	V
Static Drain–Source On–State Resistance (VGS = 2.5V, ID= 5.2A)		RDS(on)	-	42	50	mΩ
(VGS = 4.5 V, ID = 6 A)			-	33	40	
Dynamic						
Input Capacitance (VGS = 0 V, f = 1.0MHz,VDS= 8 V)		Ciss	-	565	-	pF
Output Capacitance (VGS = 0 V, f = 1.0MHz,VDS= 8 V)		Coss	-	105	-	pF
Reverse Transfer Capacitance (VGS = 0 V, f = 1.0MHz,VDS= 8 V)		Crss	-	75	-	pF
Total Gate Charge	(VDS = 10V, ID = 6A,VGS = 4.5V)	Qg		5	7	nC
Gate-Source Charge		Qgs		1		
Gate-Drain Charge		Qgd		1.5		
Turn-On Delay Time	(VDD = 10V, ID = 1A, VGS = 4.5V,RG = 6 Ω)	td(on)	-	8	20	ns
Rise Time		tr	-	10	20	
Turn-Off Delay Time		td(off)	-	22	45	
Fall Time		tf	-	6	15	
Max. Diode Forward Current		IS			1.7	A
Diode Forward Voltage (VGS = 0 V, IS = 1.7 A)		VSD	-	-	1.2	V

2.Pulse Test: Pulse Width ≤300 μs, Duty Cycle ≤2.0%.

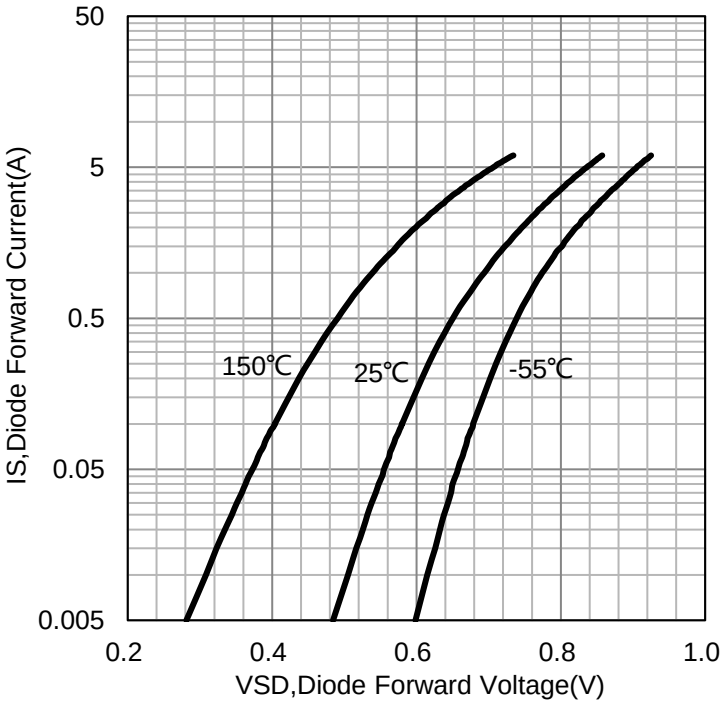
5.ELECTRICAL CHARACTERISTICS CURVES



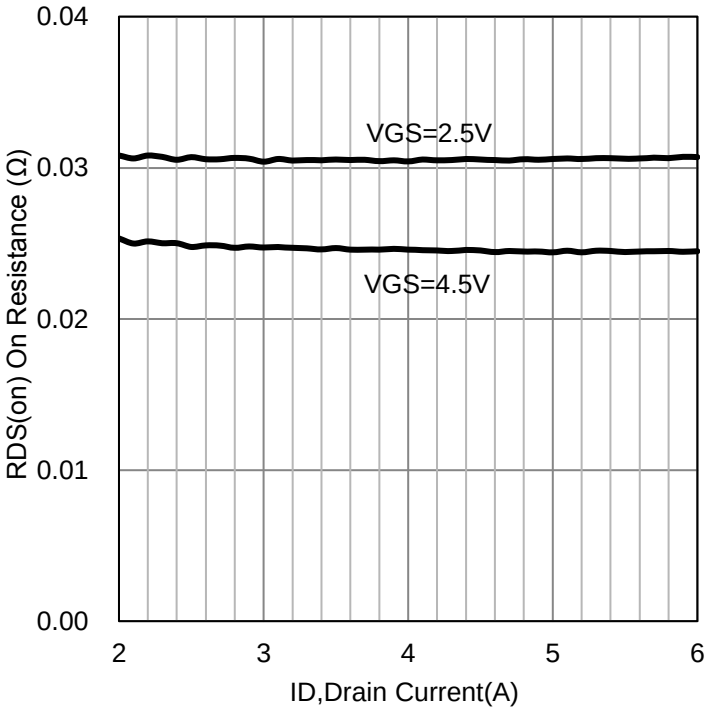
ID vs. VDS



ID vs. VGS

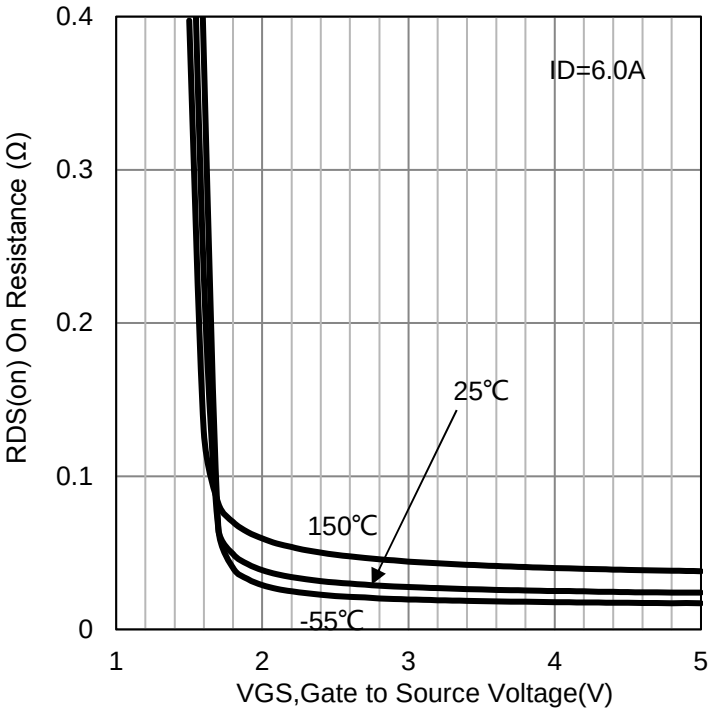


IS vs. VSD

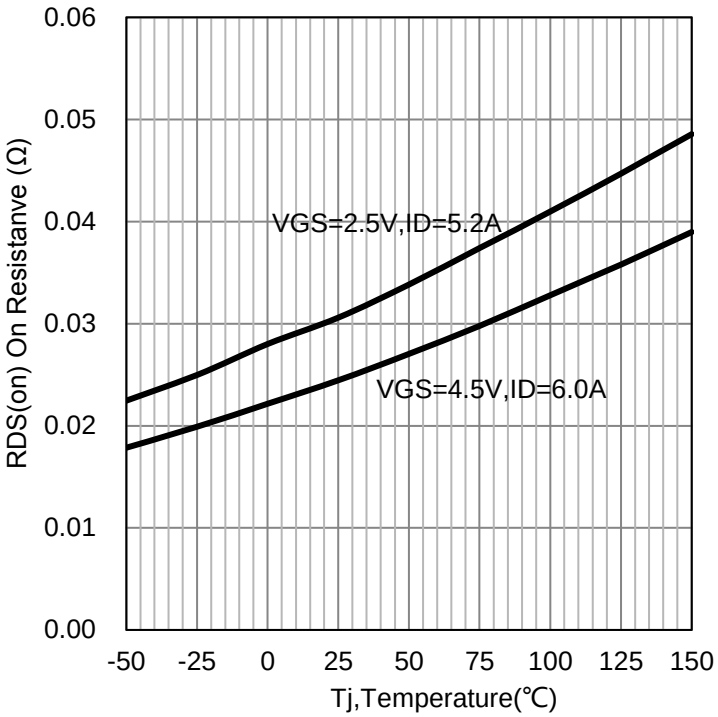


RDS(on) vs. ID

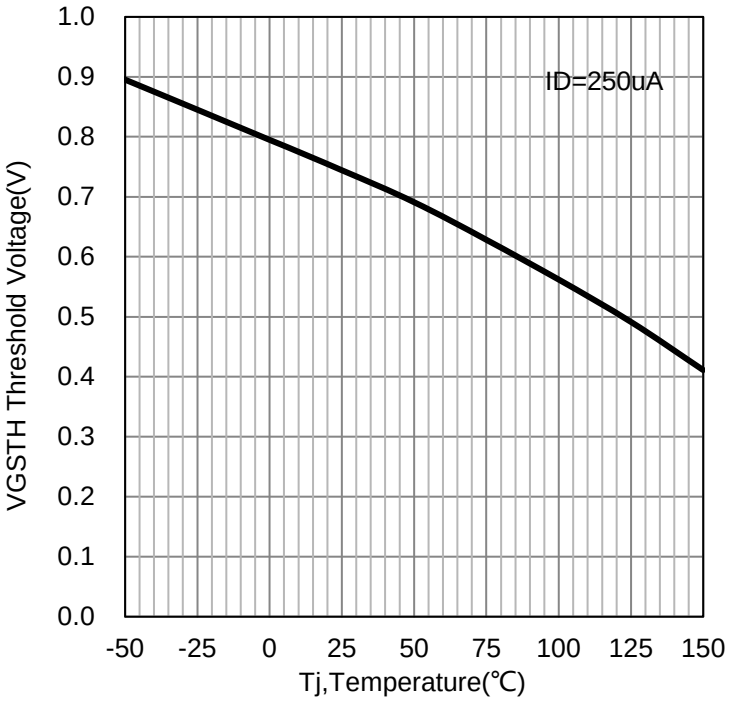
5.ELECTRICAL CHARACTERISTICS CURVES（Con.）



RDS(on) vs. VGS

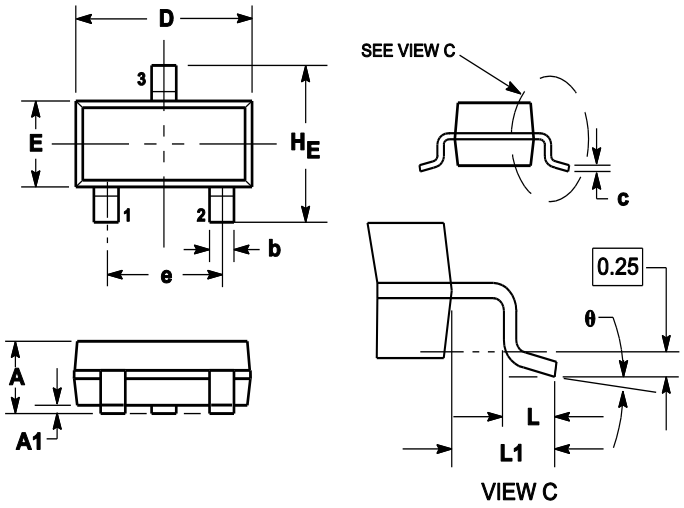


RDS(on) vs. Tj



VGSTH vs. Tj

6.OUTLINE AND DIMENSIONS



Notes:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.89	1	1.11	0.035	0.04	0.044
A1	0.01	0.06	0.1	0.001	0.002	0.004
b	0.37	0.44	0.5	0.015	0.018	0.02
c	0.09	0.13	0.18	0.003	0.005	0.007
D	2.80	2.9	3.04	0.11	0.114	0.12
E	1.20	1.3	1.4	0.047	0.051	0.055
e	1.78	1.9	2.04	0.07	0.075	0.081
L	0.10	0.2	0.3	0.004	0.008	0.012
L1	0.35	0.54	0.69	0.014	0.021	0.029
H_E	2.10	2.4	2.64	0.083	0.094	0.104
θ	0°	---	10°	0°	---	10°

7.SOLDERING FOOTPRINT