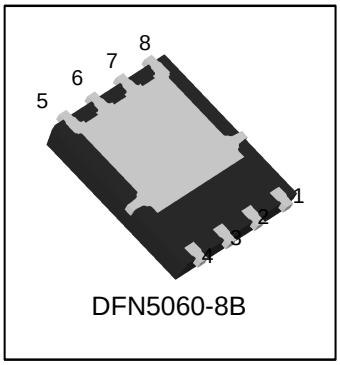
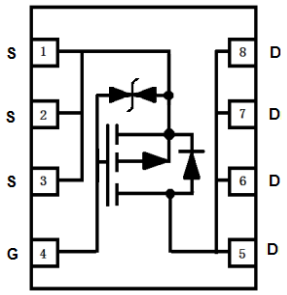
S-LP7337DT1WG

P-Channel 30-V (D-S) MOSFET





1. FEATURES

- Low RDS(on) trench technology.
- Low thermal impedance.
- Fast switching speed.
- Gate to Source ESD protected.
- We declare that the material of product compliance with RoHS requirements and Halogen Free.
- S- prefix for automotive and other applications requiring unique site and control change requirements; AEC-Q101 qualified and PPAP capable.

2. APPLICATIONS

- Load Switches.
- DC/DC Conversion.
- Motor Drives.

3. DEVICE MARKING AND RESISTOR VALUES

Device	Marking	Shipping
S-LP7337DT1WG	LP7337	3000/Tape&Reel

4. MAXIMUM RATINGS(Ta = 25ºC)

Parameter		Symbol	Limits	Unit
Drain−to−Source Voltage		VDSS	-30	V
Gate−to−Source Voltage		VGS	± 20	V
Avalanche Current		IAS	35	A
Avalanche energy L=0.1mH		EAS	61.25	mJ
Continuous Drain Current(Note 1)	TA =25°C	ID	-18	A
	TA =70°C		-13	
	TC =25°C		-70	
	TC =70°C		-50	
Pulsed Drain Current (Note 2)	TC =25°C	IDM	-200	
Power Dissipation(Note 1)	TA =25°C	PD	5	W
	TA =70°C		3.2	
Operating Junction Temperature		TJ	−55 ~+150	ºC
Storage Temperature Range		Tstg	−55 ~+150	

5. THERMAL CHARACTERISTICS

Parameter		Symbol	Limits	Units
Maximum Junction-to-Ambient(Note 1)	t <= 10 sec	RθJA	25	°C/W
	Steady State		65	
Maximum Junction-to-Case		RθJC	2.5	°C/W

1.Surface mounted on "1.5 x 1.5" FR4 board using 1 sq in pad, 2 oz Cu.

2.Pulse width limited by maximum junction temperature

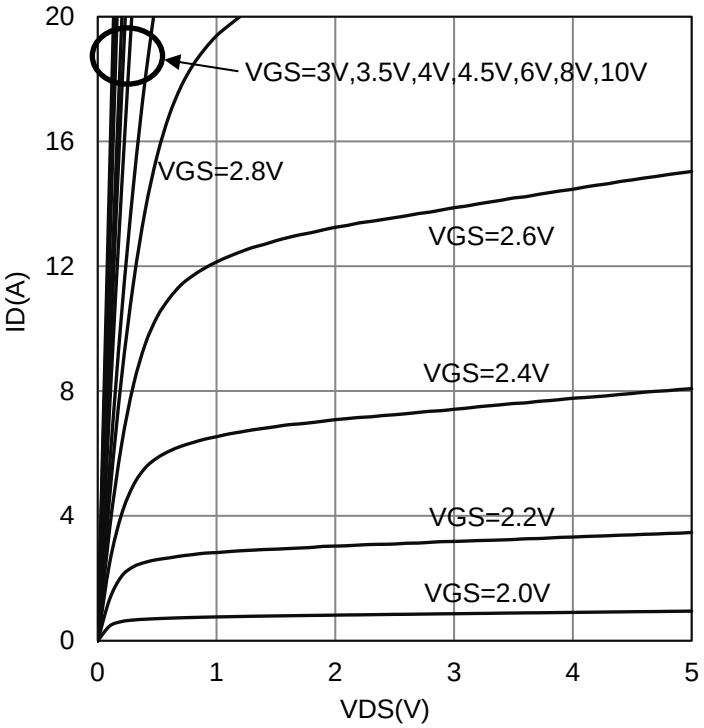
6. ELECTRICAL CHARACTERISTICS (Ta= 25°C)

Characteristic		Symbol	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage (VGS=0 , ID = -250 uA)		V(BR)DSS	-30	-	-	V
Gate-Source Threshold Voltage (VDS = VGS , ID = -250 uA)		VGS(th)	-1	-1.3	-3	V
Gate-Body Leakage (VDS = 0 V, VGS = ± 20 V)		IGSS	-	-	± 10	μA
Zero Gate Voltage Drain Current (VDS = -24 V, VGS = 0 V) (VDS = -24 V, VGS = 0 V, TJ = 55° C)		IDSS	- -	- -	-1 -25	μA
Drain-Source On-Resistance(Note 3) (VGS = -10 V, ID = -13.6 A) (VGS = -4.5 V, ID = -10.9 A)		RDS(on)	- -	7.5 10.5	9 13	mΩ
Diode Forward Voltage(Note 3) (IS = -2.3 A, VGS = 0 V)		VSD	-	-0.76	-1.2	V
Dynamic(Note 4)						
Total Gate Charge	(VDS = -15 V, VGS = -4.5 V,ID = -13.6 A)	Qg	-	35	-	nC
Gate-Source Charge		Qgs	-	10	-	
Gate-Drain Charge		Qgd	-	12.3	-	
Input Capacitance	(VDS = -15 V, VGS = 0 V, f = 1 MHz)	Ciss	-	4391	-	pF
Output Capacitance		Coss	-	440	-	
Reverse Transfer Capacitance		Crss	-	372	-	
Turn-On Delay Time	(VDS=-15 V, RL=1.2 Ω,ID=-13.6 A,VGEN=-10 V,RGEN=6 Ω)	td(on)	-	14	-	ns
Rise Time		tr	-	37	-	
Turn-Off Delay Time		td(off)	-	124	-	
Fall Time		tf	-	55	-	
Source-Drain DIODE Ratings and Characteristics(Tc= 25° C)						
Continuous Current(Note 1)		IS	-	-	-25	A
Plused Current(Note 1)		ISM	-	-	-100	A
Reverse Recovery Time (IF=IS,dIf/dt=100A/us)		trr	-	62	-	ns
Reverse Recovery Charge (IF=IS,dIf/dt=100A/us)		Qrr	-	68	-	nC

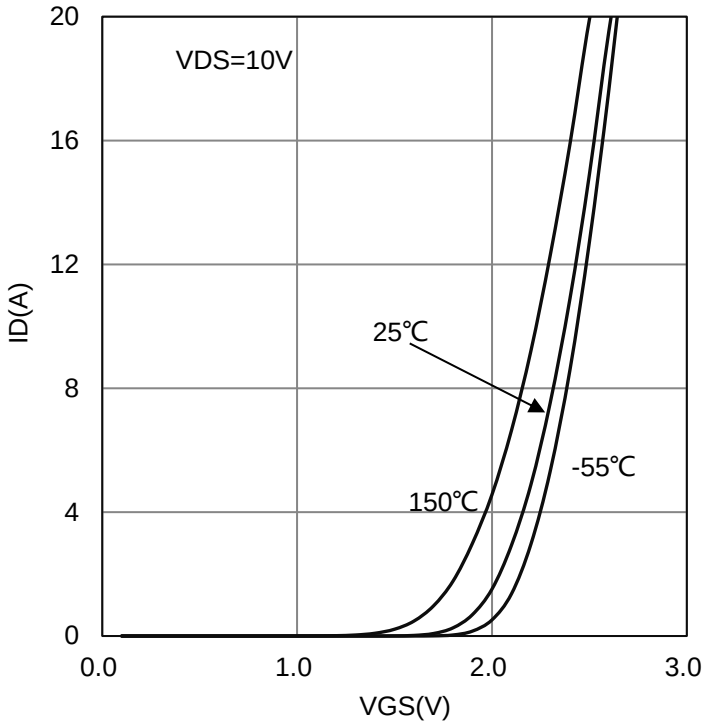
3.Pulse test: PW≤ 300μs duty cycle ≤ 2%.

4.Guaranteed by design, not subject to production testing.

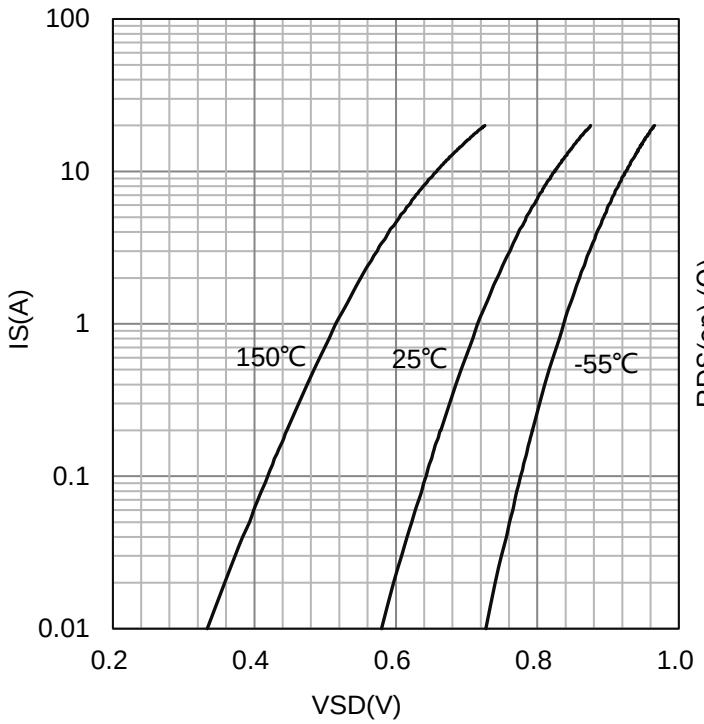
7.ELECTRICAL CHARACTERISTICS CURVES



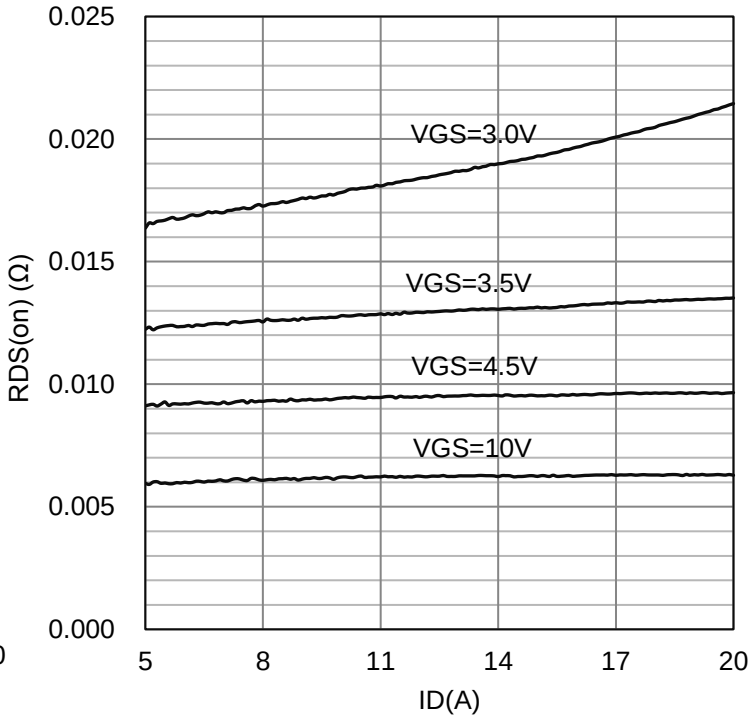
ID vs. VDS



ID vs. VGS

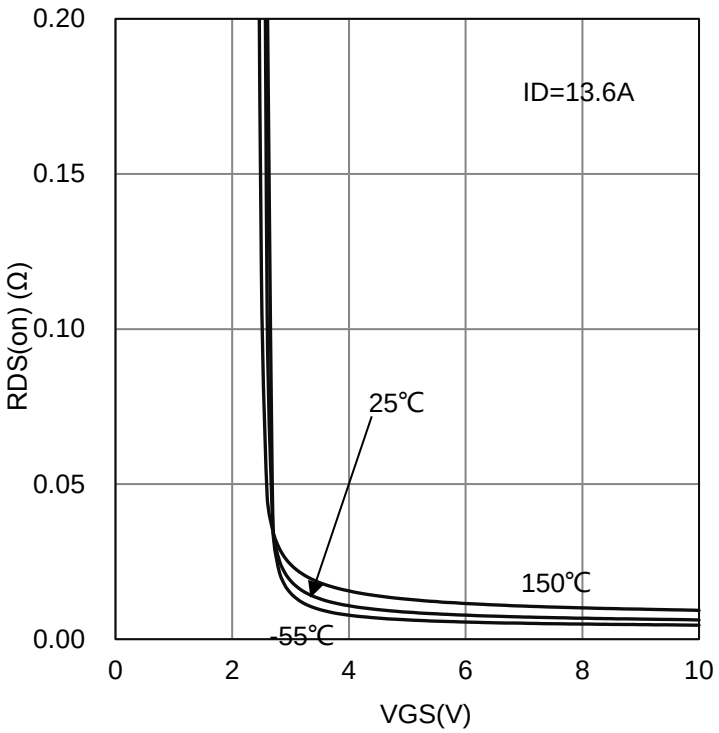


IS vs. VSD

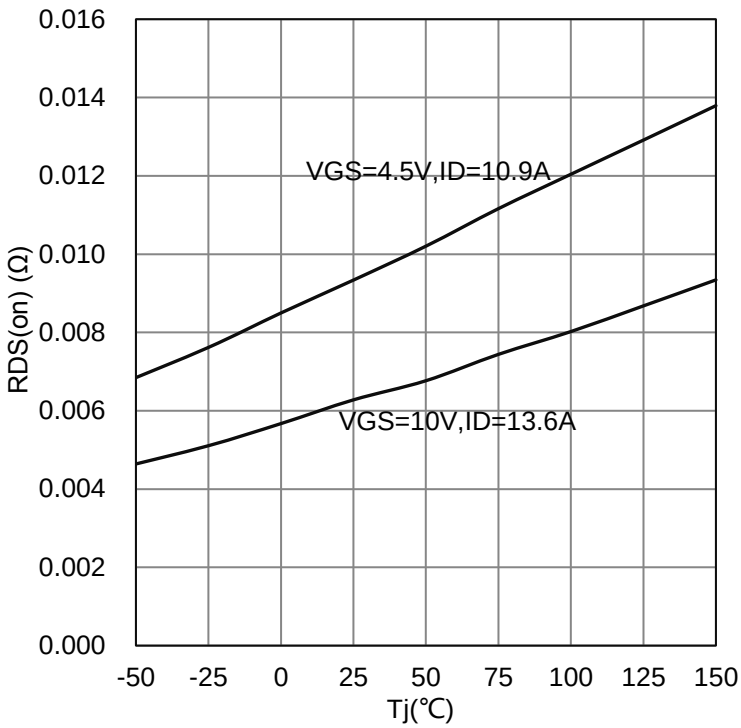


RDS(on) vs. ID

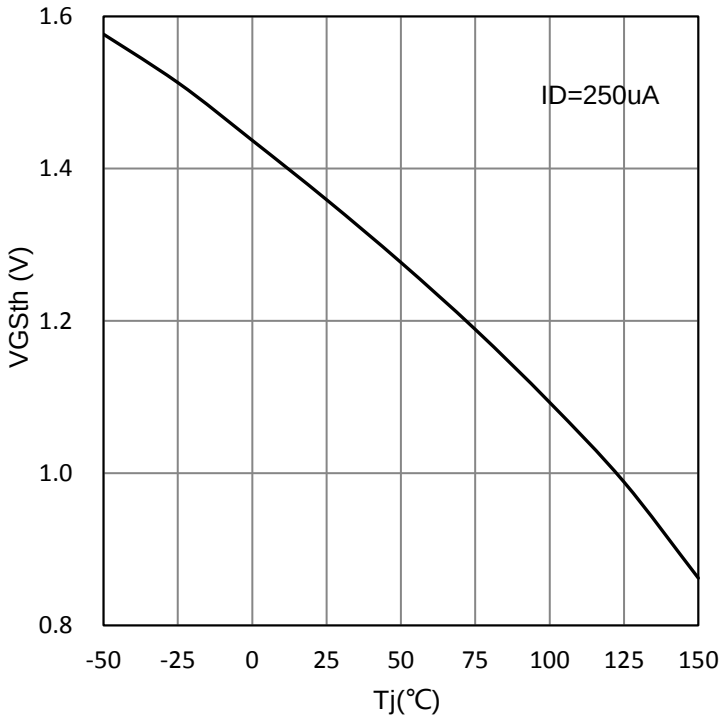
7.ELECTRICAL CHARACTERISTICS CURVES(Con.)



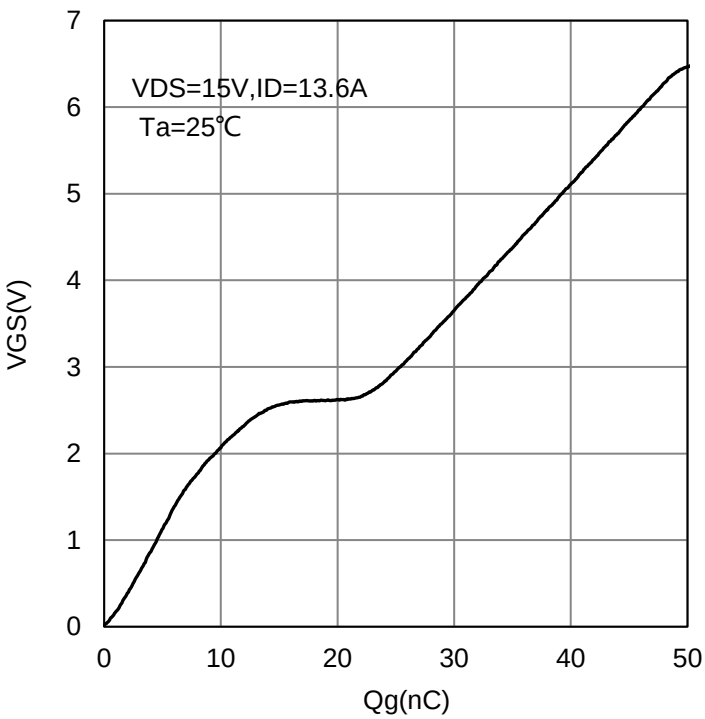
RDS(on) vs. VGS



RDS(on) vs. Tj

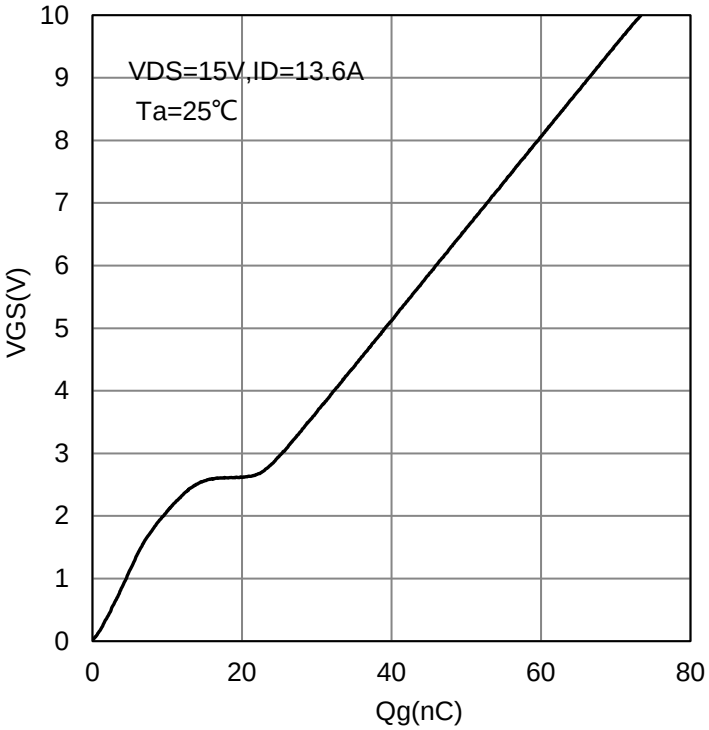


VGSTH vs. Tj

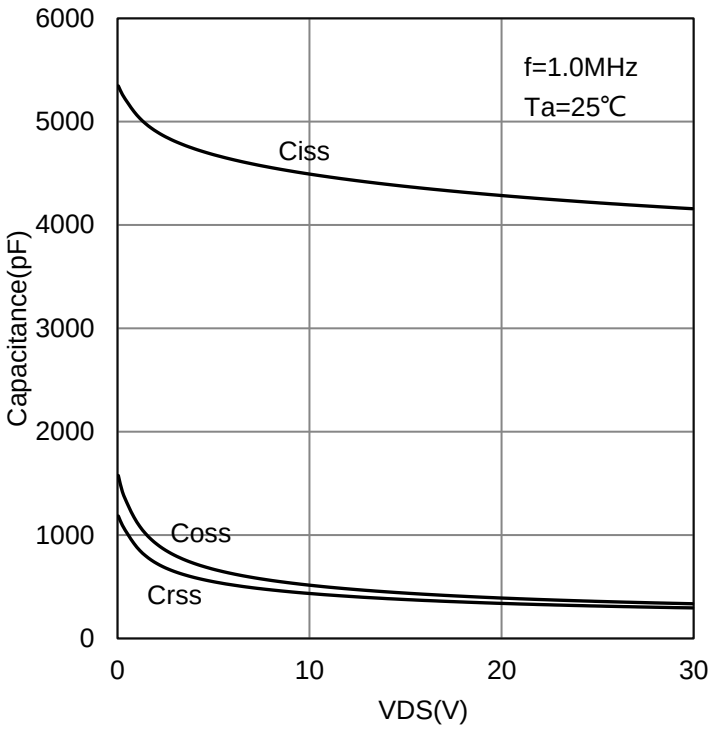


VGS vs. Qg (VGS=4.5V)

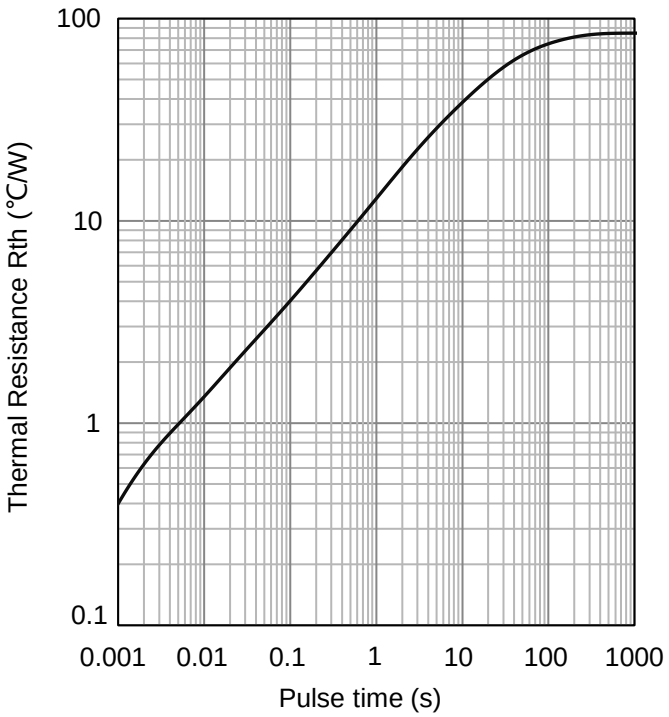
7.ELECTRICAL CHARACTERISTICS CURVES(Con.)



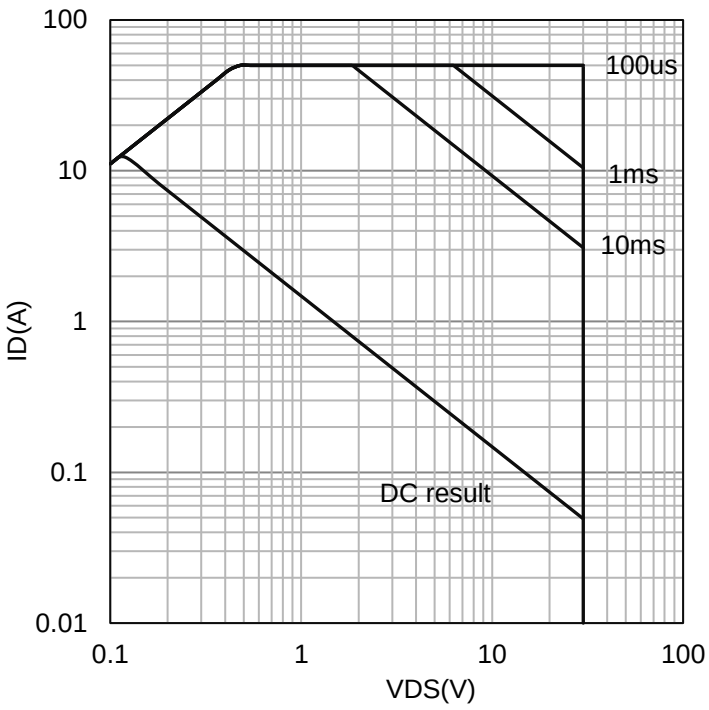
VGS vs. Qg (VGS=10V)



Capacitance

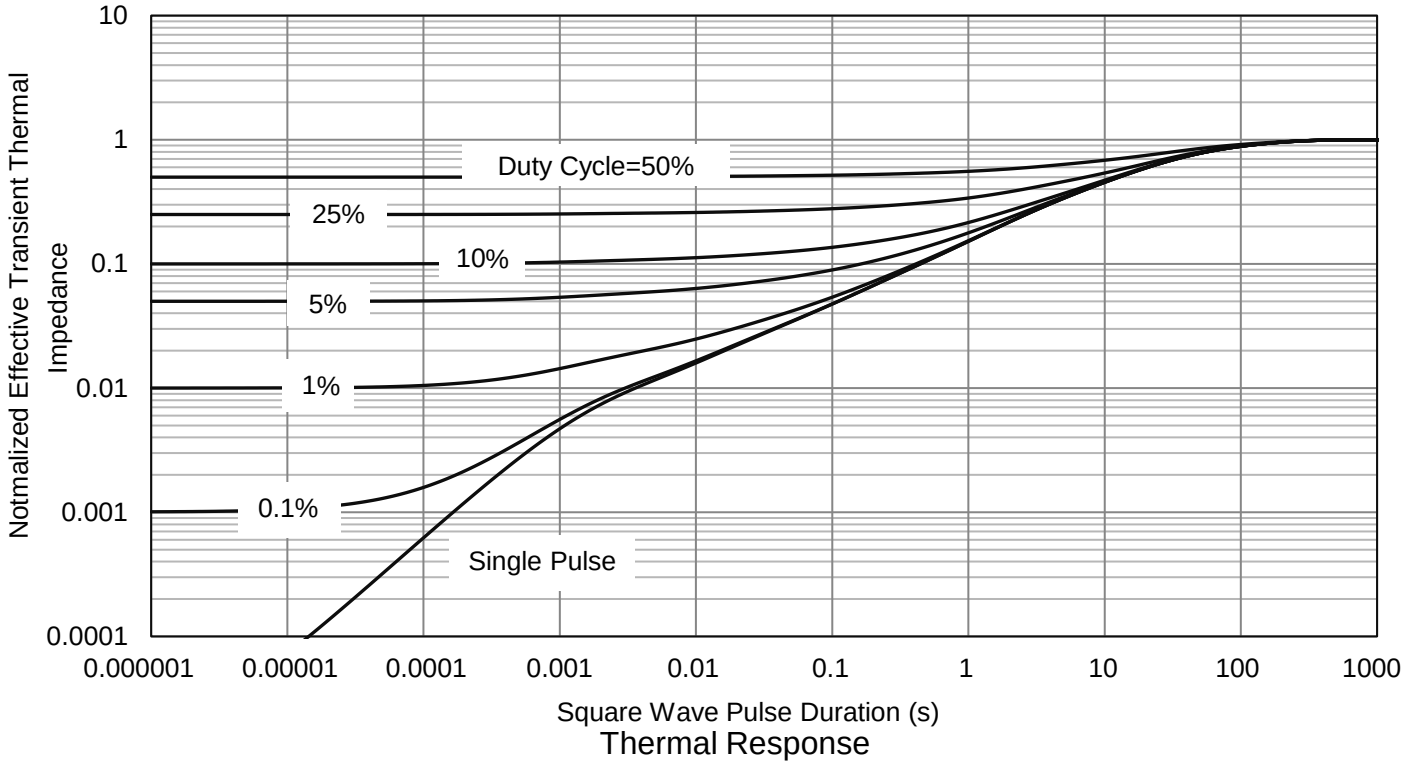


Rth vs. tsw



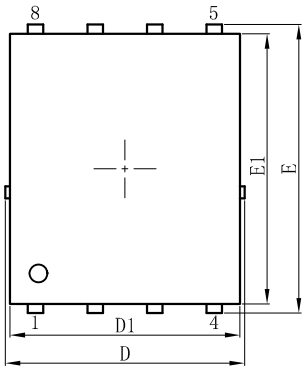
SOA

7.ELECTRICAL CHARACTERISTICS CURVES(Con.)

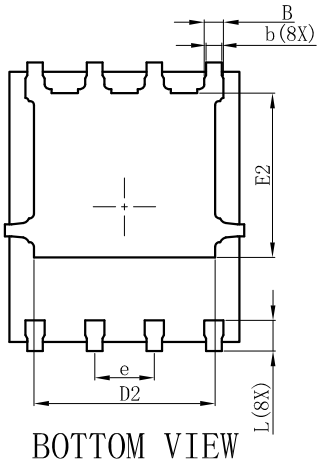


8.OUTLINE AND DIMENSIONS

DFN5060-8B

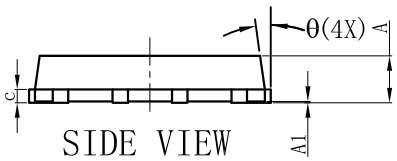


TOP VIEW



BOTTOM VIEW

DFN5060-8B			
DIM	MIN	NOR	MAX
A	0.90	1.00	1.10
A1	0.00	0.02	0.05
E	6.00	6.15	6.30
E1	5.66	5.76	5.86
E2	3.40	3.50	3.60
D	4.95	5.10	5.25
D1	4.80	4.90	5.00
D2	3.76	3.86	3.96
b	0.30	0.35	0.40
B	0.36	0.41	0.46
L	0.56	0.66	0.76
e	1.27BSC		
c	0.254REF.		
θ	0°	-	12°
All Dimensions in mm			

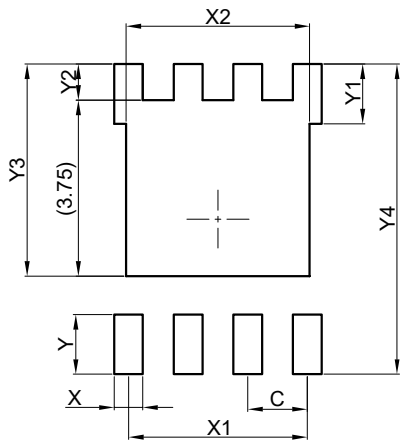


SIDE VIEW

GENERAL NOTES

1. Top package surface finish Ra0.4±0.2um
2. Bottom package surface finish Ra0.7±0.2um
3. Side package surface finish Ra0.4±0.2um
4. Protrusion or Gate Burrs shall not exceed 0.05mm per side.
5. Offcenter Max0.038mm; Mismatch Max 0.038mm.

9.SOLDERING FOOTPRINT



DFN5060-8B	
DIM	(mm)
C	1.27
X	0.61
X1	3.81
X2	3.91
Y	1.27
Y1	1.27
Y2	0.77
Y3	4.52
Y4	6.61

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