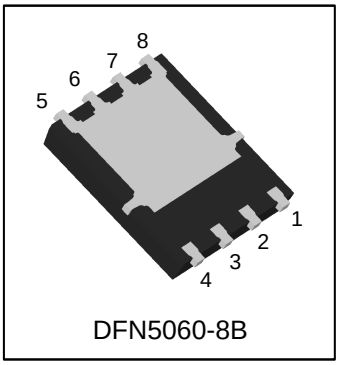
S-LP7516DT3WG

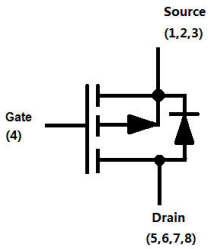
60V P-Channel Power MOSFET



DFN5060-8B

1. FEATURES

- Low thermal impedance.
- Fast switching speed.
- We declare that the material of product compliance with RoHS requirements and Halogen Free.
- S-prefix for automotive and other applications requiring unique site and control change requirements; AEC-Q101 qualified and PPAP capable.



2. APPLICATIONS

- Power Tools
- DC−DC conversion
- Motor Control

3. DEVICE MARKING AND RESISTOR VALUES

Device	Marking	Shipping
S-LP7516DT3WG	LP7516	5000/Tape&Reel

4. MAXIMUM RATINGS

Parameter		Symbol	Limits	Unit
Drain-to-Source Voltage		VDS	-60	V
Gate-to-Source Voltage		VGS	± 20	V
Continuous Drain Current(Note 1)	TA=25℃	ID	-12	A
	TA=100℃		-8	
Pulsed Drain Current(Note 2)	TA=25℃	IDM	-48	A
Continuous Drain Current	TC=25℃	ID	-60	A
	TC=100℃		-36	
Pulsed Drain Current	TC=25℃	IDM	-240	A
Avalanche Current		IAS	38.4	A
Avalanche Energy(L=0.1mH)		EAS	73.72	mJ
Power Dissipation(Note 1)	TA=25℃	PD	3	W
	TA=100℃		1.5	
Power Dissipation	TC=25℃		100	
	TC=100℃		50	
Operating Junction and Storage Temperature Range		TJ/TSTG	-55~+175	℃

5. THERMAL CHARACTERISTICS

Parameter	Symbol	Max	Unit
Junction-to-Ambient(Note 1)	RθJA	50	℃/W
Junction-to-Case	RθJC	1.5	

Note:1.Surface mounted on "1.5in x 1.5in" FR4 board using 1*1 in pad, 2 oz Cu.

2.Pulse width limited by maximum junction temperature.

6. ELECTRICAL CHARACTERISTICS

Characteristic		Symbol	Min.	Typ.	Max.	Unit
STATIC						
Drain–Source Breakdown Voltage (VGS = 0 V, ID = -250 μA)		VBRDSS	-60	-	-	V
Gate Threshold Voltage (VDS = VGS , ID = -250 μA)		VGS(th)	-1.3	-1.8	-2.3	V
Gate-Body leakage current (VDS = 0 V, VGS = ±20 V)		IGSS	-	-	±100	nA
Zero Gate Voltage Drain Current (VDS = -60 V, VGS = 0 V)		IDSS	-	-	-1	μA
Drain-to-Source On-Resistance (Note 3) (VGS = -10 V, ID = -20 A) (VGS = -4.5 V, ID = -10 A)		RDS(on)	- -	11 15	16 19	mΩ
DYNAMIC						
Input Capacitance	(VGS = 0 V, VDS = -30 V, f = 100kHz)	Ciss	-	2670	-	pF
Output Capacitance		Coss	-	478	-	
Reverse Transfer Capacitance		Crss	-	29	-	
Total Gate Charge	(VDS = -30 V,VGS = -10 V,ID = -20 A)	Qg	-	43.7	-	nC
Gate Source Charge		Qgs	-	9	-	
Gate Drain Charge		Qgd	-	8	-	
Turn-On DelayTime	(VDS = -30 V, ID = -20 A, VGS = -10 V, RG = 6 Ω)	td(on)	-	12	-	ns
Turn-On Rise Time		tr	-	14	-	
Turn-Off DelayTime		td(off)	-	138	-	
Turn-Off Fall Time		tf	-	67	-	
Diode characteristics						
Continuous Current TC =25° C		IS	-	-	-60	A
Plused Current TC =25° C		ISM	-	-	-240	A
Diode Forward Voltage (IS = -10 A,VGS = 0 V)		VSD	-	-0.82	-1.2	V
Reverse Recovery Time (VR=-30V,IF=-6A,dIF/dt=100A/us)		trr	-	54	-	ns
Reverse Recovery Charge (VR=-30V,IF=-6A,dIF/dt=100A/us)		Qrr	-	65	-	nC
Reverse Recovery Current (VR=-30V,IF=-6A,dIF/dt=100A/us)		IRRM	-	2.45	-	A

3.Pulse test: PW ≤ 300us duty cycle ≤ 2%.

7. ELECTRICAL CHARACTERISTICS CURVES

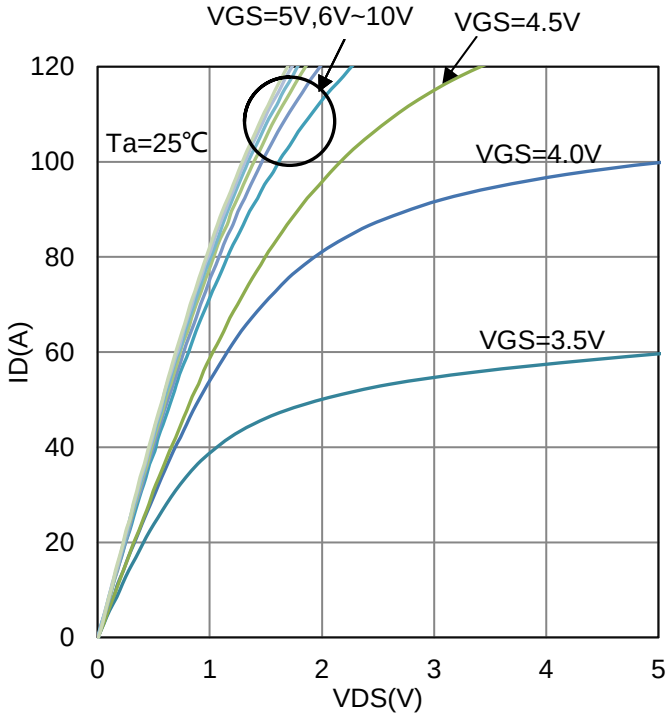


Figure 1.ID vs. VDS

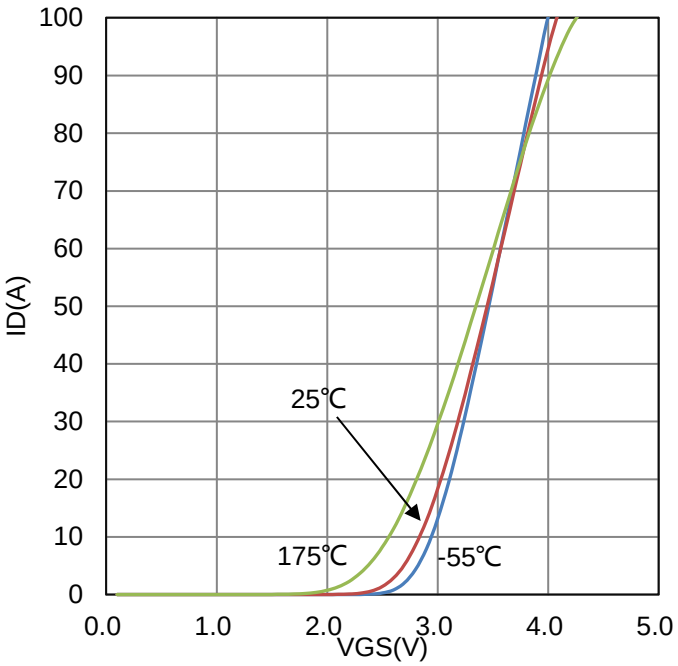


Figure 2.ID vs. VGS

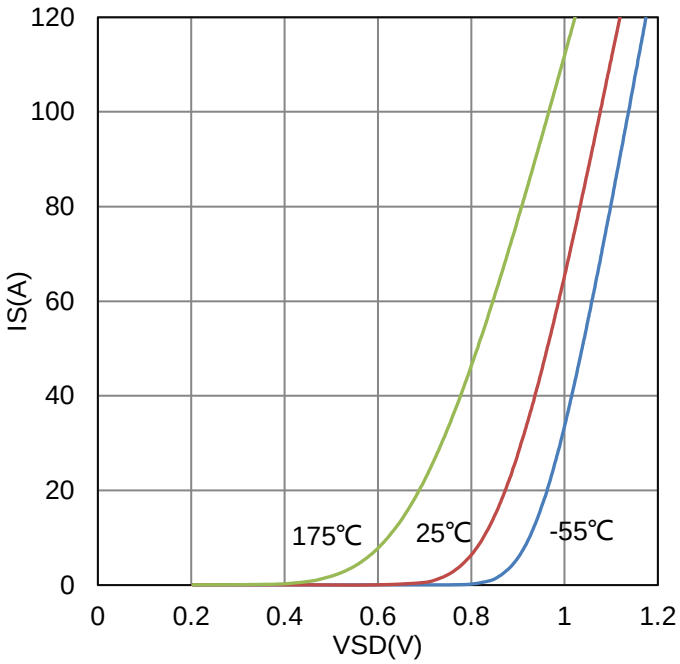


Figure 3.IS vs. VSD

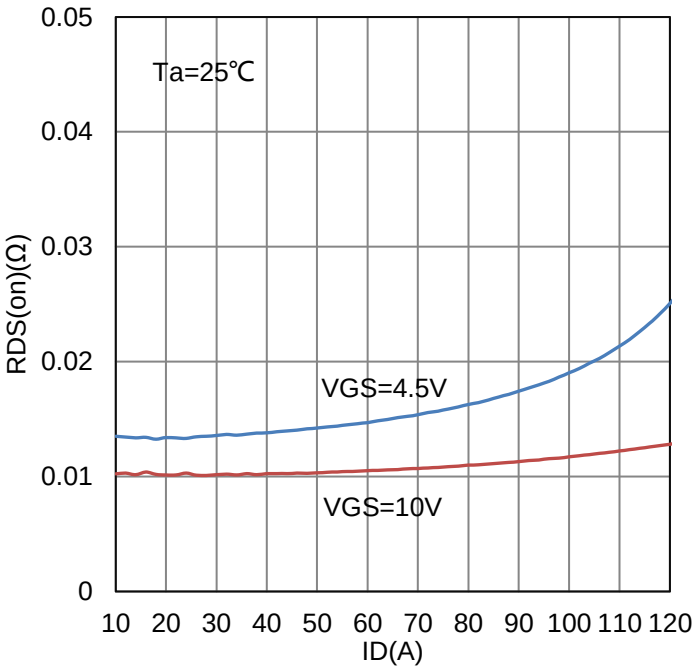


Figure 4.RDS(on) vs. ID

7. ELECTRICAL CHARACTERISTICS CURVES(Con.)

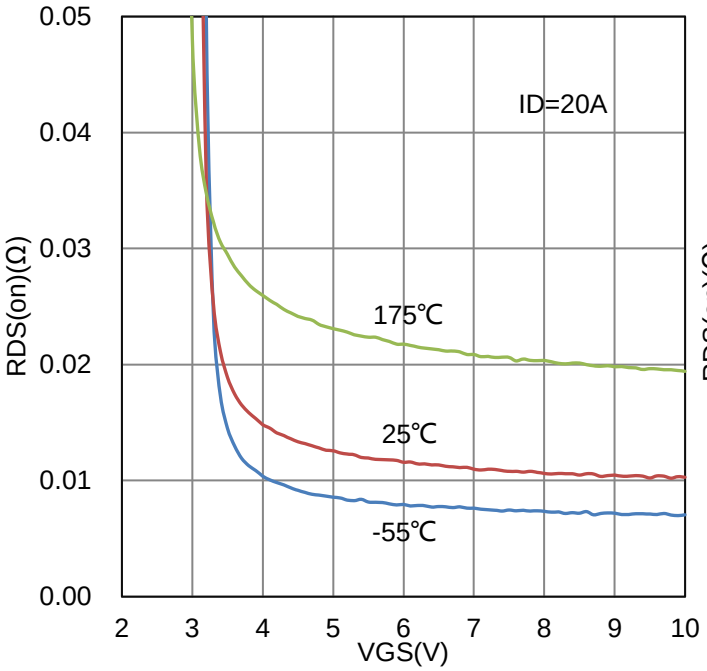


Figure 5.RDS(on) vs. VGS

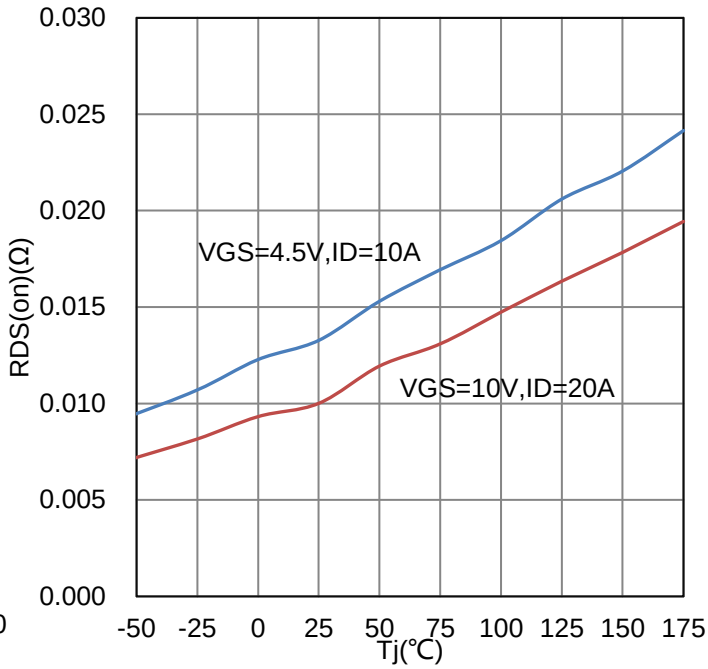


Figure 6.RDS(on) vs. Tj

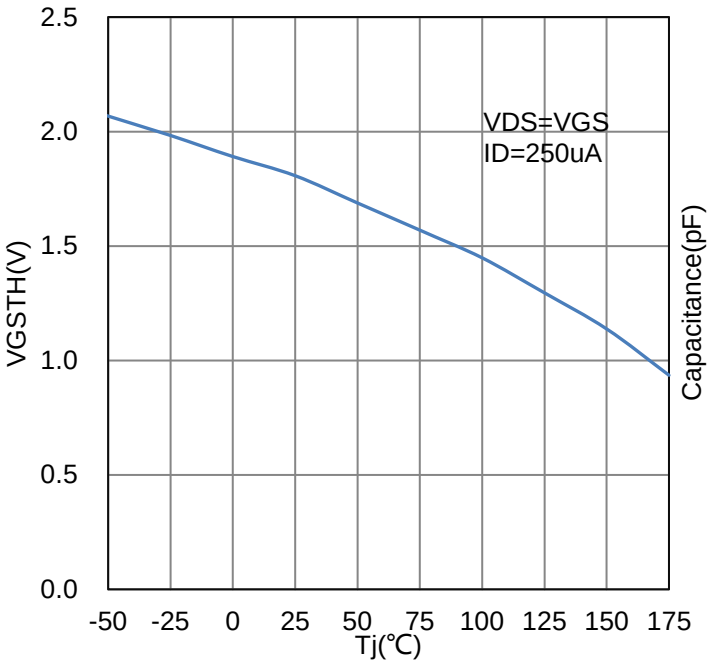


Figure 7.VGSth vs. Tj

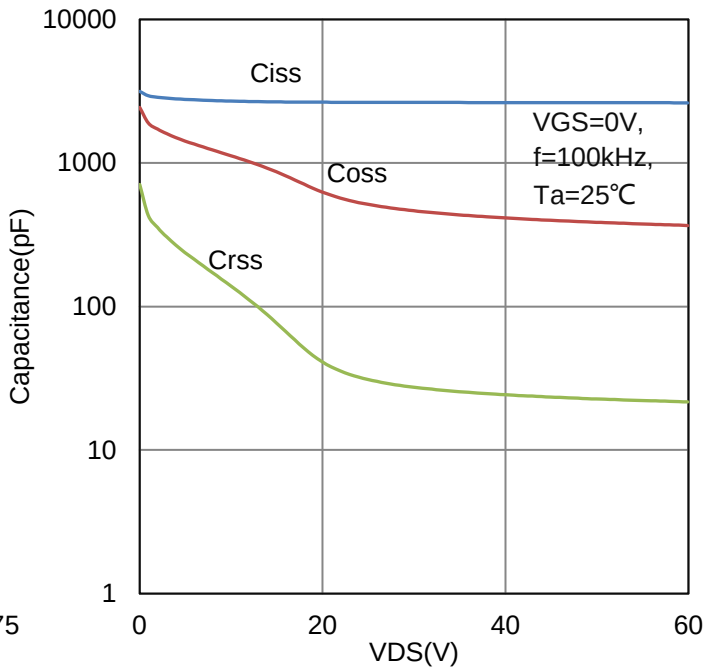


Figure 8.Capacitance

7. ELECTRICAL CHARACTERISTICS CURVES(Con.)

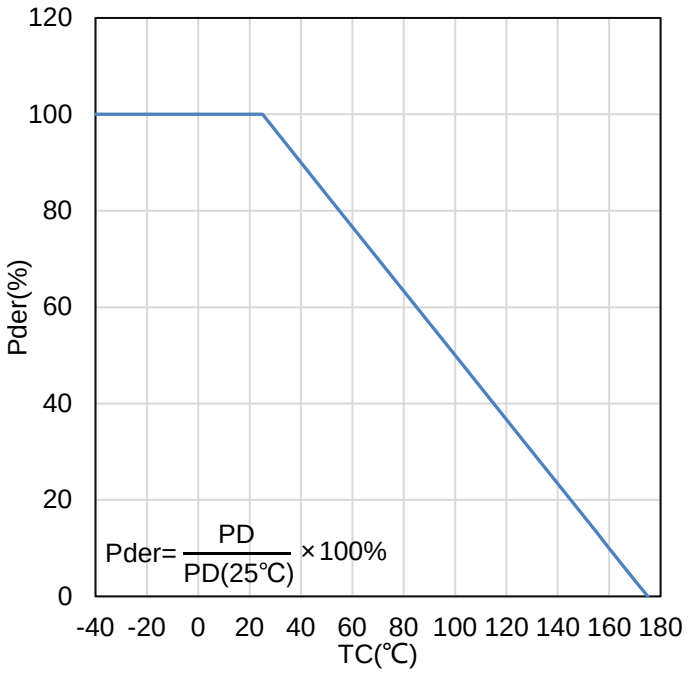


Figure 9.Normalized Derating Curve

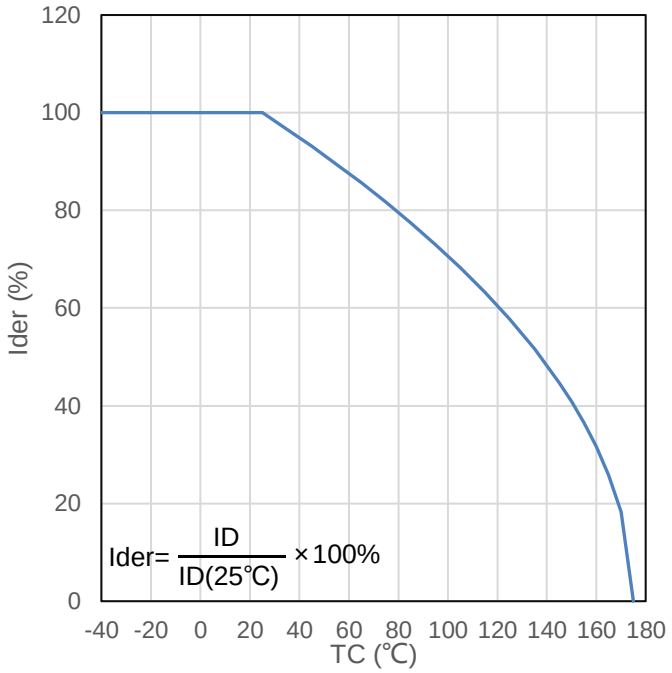


Figure 10.Normalized drain Current

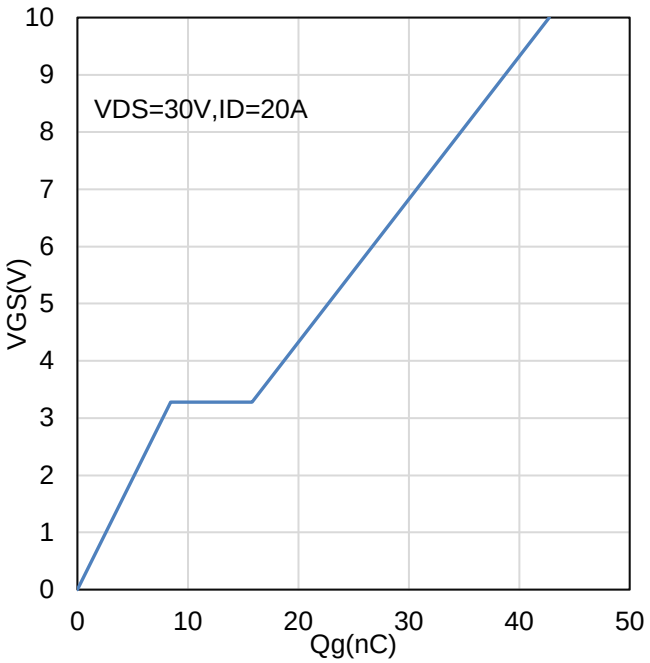


Figure 11.VGS vs. Qg

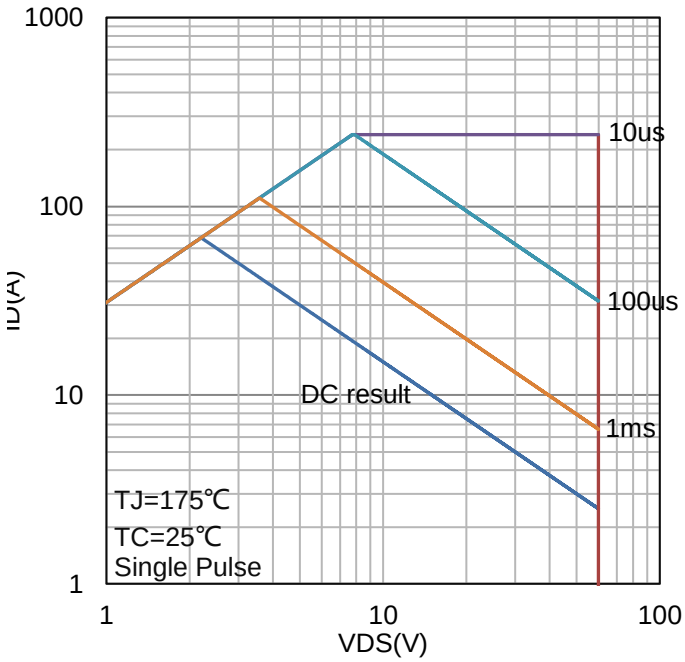


Figure 12.Safe Operating Area

7. ELECTRICAL CHARACTERISTICS CURVES(Con.)

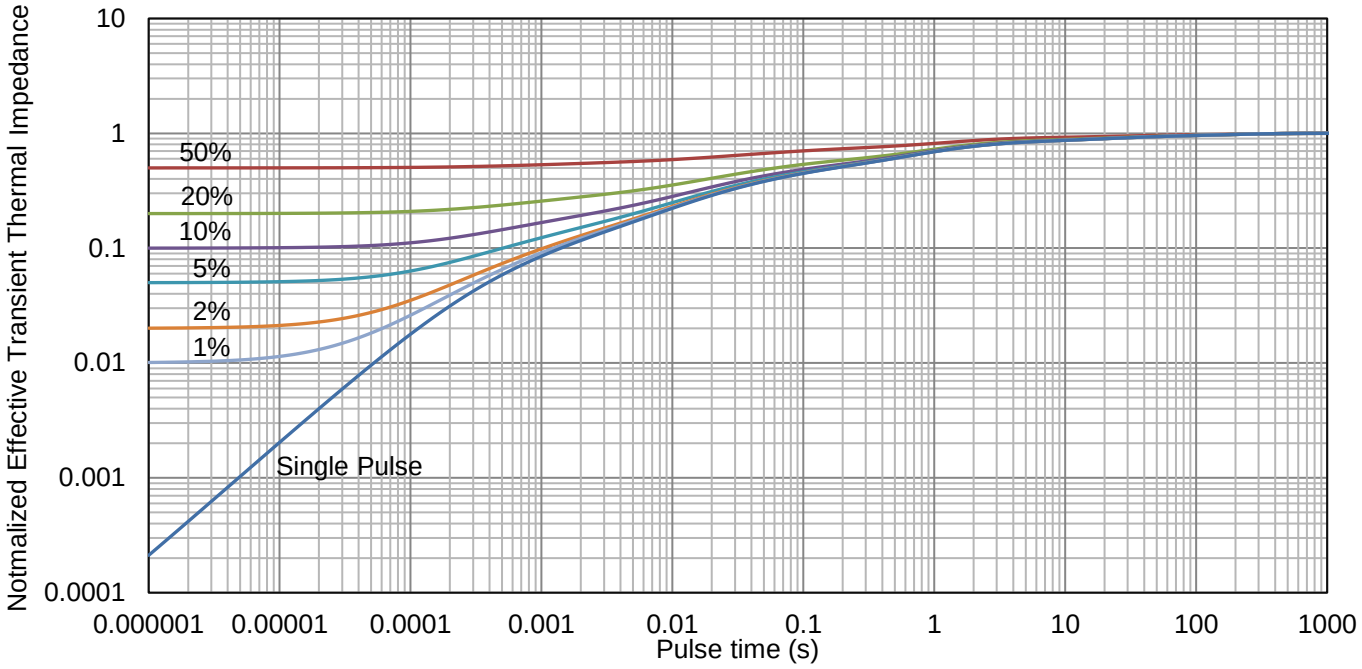
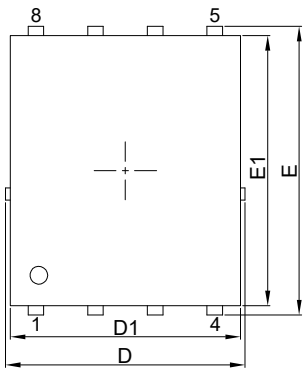


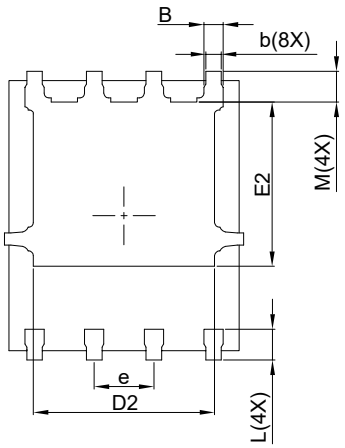
Figure 13.Thermal Response

8.OUTLINE AND DIMENSIONS

DFN5060-8B

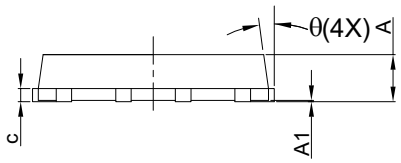


TOP VIEW



BOTTOM VIEW

DFN5060-8B			
DIM	MIN	NOR	MAX
A	0.90	1.00	1.10
A1	0.00	0.02	0.05
E	6.00	6.15	6.30
E1	5.66	5.76	5.86
E2	3.40	3.50	3.60
D	4.95	5.10	5.25
D1	4.80	4.90	5.00
D2	3.76	3.86	3.96
b	0.30	0.35	0.40
B	0.36	0.41	0.46
L	0.56	0.66	0.76
M	0.56	0.66	0.76
e	1.27BSC		
c	0.254REF.		
θ	0 °	-	12°

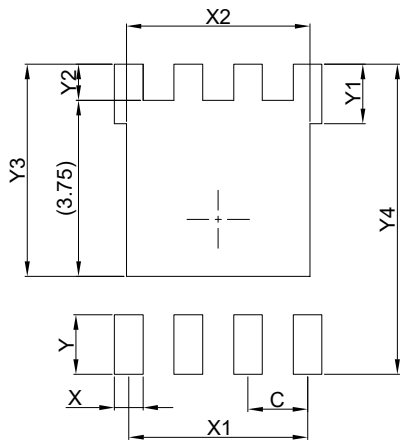


SIDE VIEW

GENERAL NOTES

1. Top package surface finish Ra Max0.4um
2. Bottom package surface finish Ra Max0.4um
3. Side package surface finish Ra Max0.4um
4. Protrusion or Gate Burrs shall not exceed 0.05mm per side
5. Offcenter Max0.038mm; Mismatch Max 0.038mm.

9.SOLDERING FOOTPRINT



DFN5060-8B	
DIM	(mm)
C	1.27
X	0.61
X1	3.81
X2	3.91
Y	1.27
Y1	1.27
Y2	0.77
Y3	4.52
Y4	6.61

DISCLAIMER

- Curve guarantee in the specification. The curve of test items with electric parameter is used as quality guarantee. The curve of test items without electric parameter is used as reference only.

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