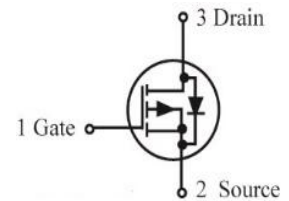
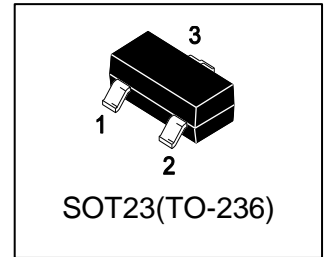


# LP3443LT1G

## S-LP3443LT1G

20V P-Channel Enhancement-Mode MOSFET



### 1. FEATURES

- $V_{DS} = -20V$
- $R_{DS(ON)} \leq 70m\Omega, @V_{GS} = -4.5V, I_{DS} = -4.7A$
- $R_{DS(ON)} \leq 110m\Omega, @V_{GS} = -2.5V, I_{DS} = -1.0A$
- We declare that the material of product compliance with RoHS requirements and Halogen Free.
- S- prefix for automotive and other applications requiring unique site and control change requirements; AEC-Q101 qualified and PPAP capable.
- ESD rating of class 0 (<100V) per Human Body Model

### 2. APPLICATIONS

- Advanced trench process technology
- High density cell design for ultra low on-resistance.

### 3. DEVICE MARKING AND ORDERING INFORMATION

Device	Marking	Shipping
LP3443LT1G	P34	3000/Tape&Reel
LP3443LT3G	P34	10000/Tape&Reel

### 4. MAXIMUM RATINGS( $T_a = 25^\circ C$ )

Parameter	Symbol	Limits	Unit
Drain-Source Voltage	$V_{DSS}$	-20	V
Gate-to-Source Voltage – Continuous	$V_{GS}$	$\pm 12$	V
Drain Current			A
– Continuous $T_a = 25^\circ C$	$I_D$	-4.7	
– Pulsed (Note 1)	$I_{DM}$	-20	
Avalanche Current( $L=0.1mH$ )	$I_{AS}$	10	A
Avalanche Energy( $L=0.1mH$ )	$E_{AS}$	5	mJ

### 5. THERMAL CHARACTERISTICS

Parameter	Symbol	Limits	Unit	
Power Dissipation	PD	$T_a = 25^\circ C$	1.1	W
		$T_a = 75^\circ C$	0.7	W
Thermal Resistance, Junction-to-Ambient(Note 2)	$R_{\theta JA}$	110	$^\circ C/W$	
Junction and Storage temperature	$T_J, T_{stg}$	$-55 \sim +150$	$^\circ C$	

1. Repetitive Rating: Pulse width limited by the maximum junction temperature.

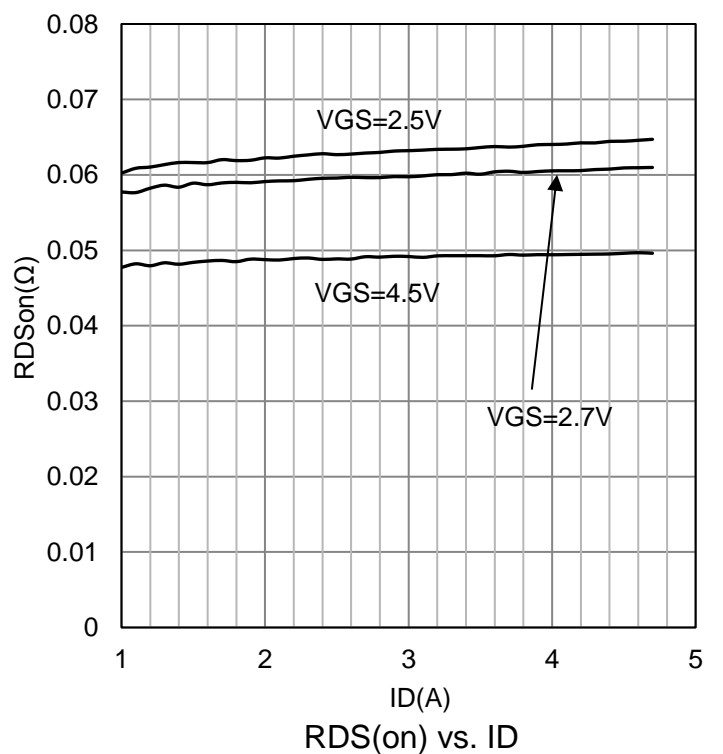
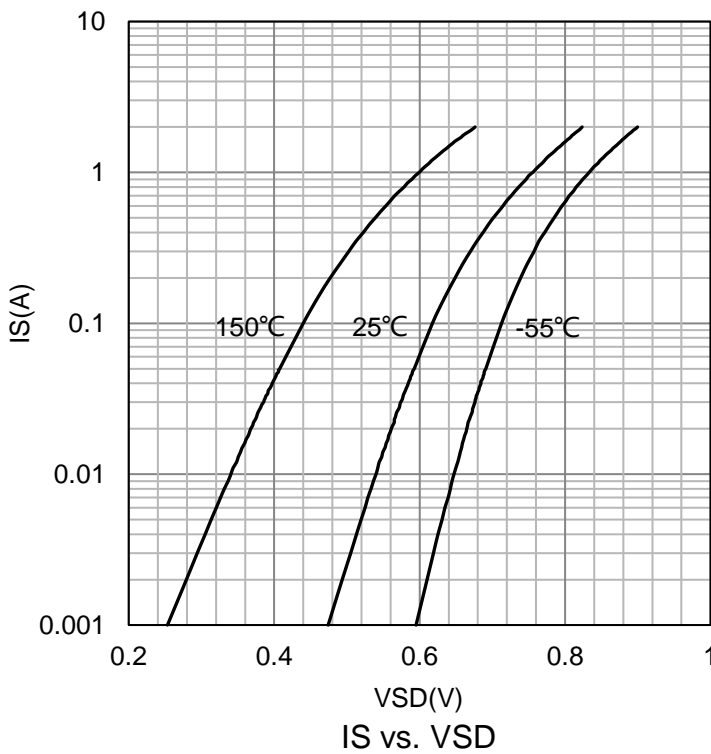
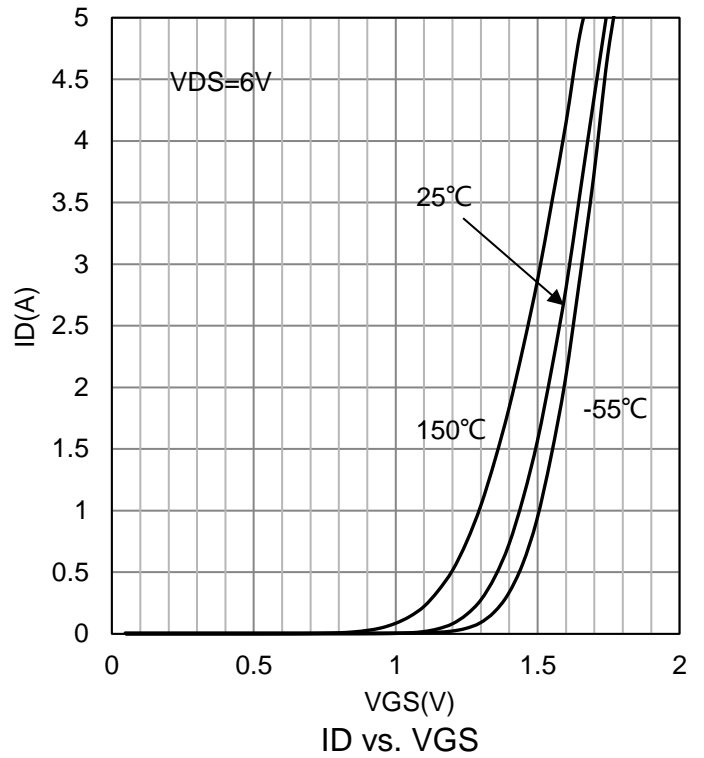
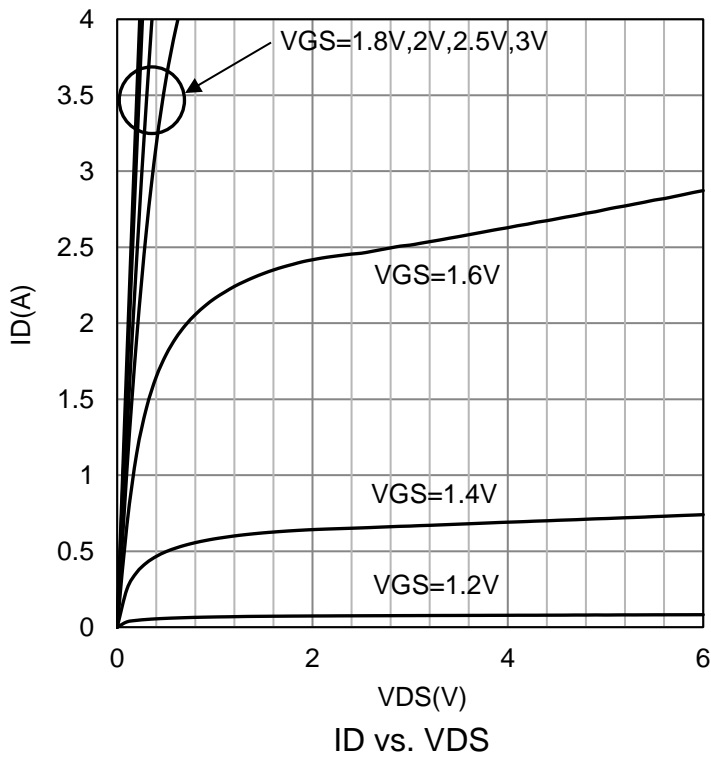
2. 1-in<sup>2</sup> 2oz Cu PCB board.

**6. ELECTRICAL CHARACTERISTICS (Ta= 25°C)**

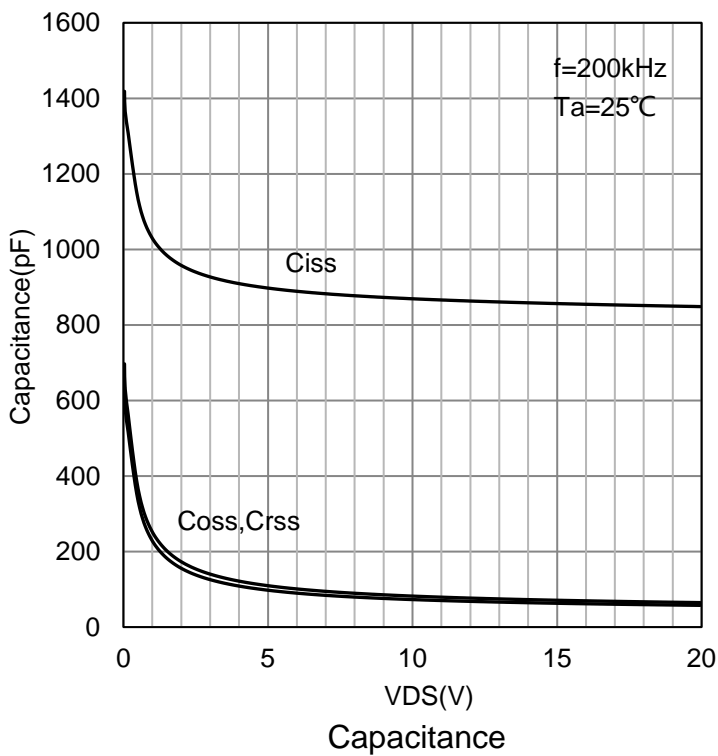
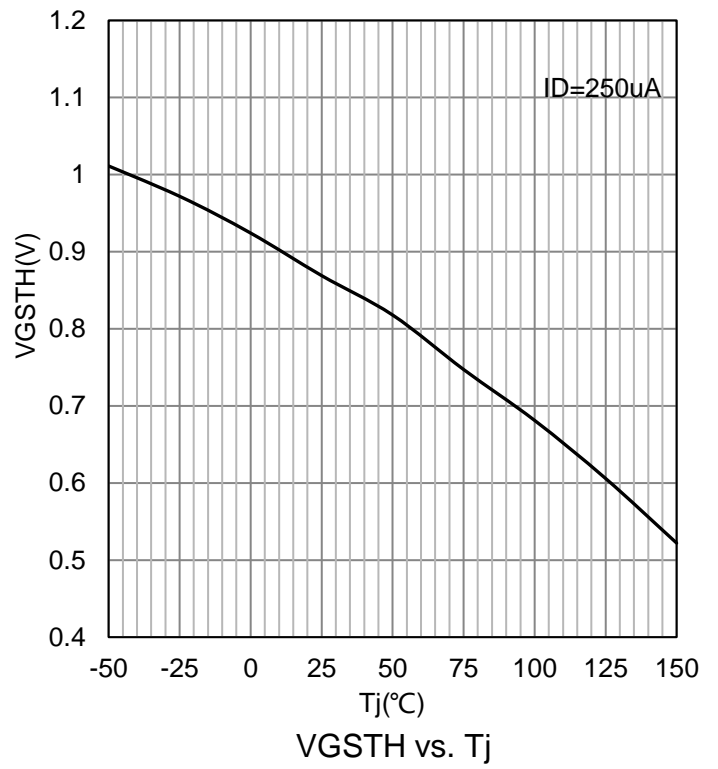
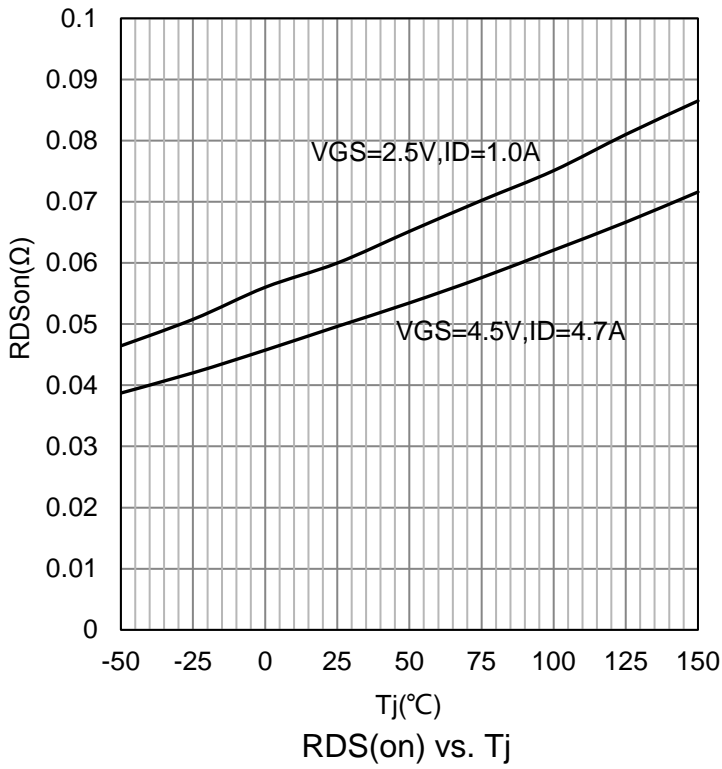
Characteristic	Symbol	Min.	Typ.	Max.	Unit
<b>STATIC</b>					
Drain–Source Breakdown Voltage (VGS = 0, ID = -250μA)	VBRDSS	-20	-	-	V
Gate Threshold Voltage (VDS = VGS, ID = -250μA)	VGS(th)	-0.6	-0.85	-1.4	V
Zero Gate Voltage Drain Current (VGS = 0, VDS = -20 V)	IDSS	-	-	-1	μA
Gate-to–Source Leakage Current (VDS = 0 V, VGS = ±12 V)	IGSS	-	-	±100	nA
Static Drain–Source On–State Resistance(Note 3) (VGS = -4.5V, ID = -4.7A) (VGS = -2.7V, ID = -3.8A) (VGS = -2.5V, ID = -1.0A)	RDS(on)	-	58 63 75	70 90 110	mΩ
Diode Forward Voltage (VGS = 0 V, ISD = -1.7 A)	VSD	-	-	-1.2	V
<b>DYNAMIC</b>					
Total Gate Charge@10V	Qg	-	20	-	nC
Total Gate Charge@4.5V	Qg	-	9	-	
Gate-to–Source Gate Charge	Qgs	-	1.5	-	
Gate-to–Drain Charge	Qgd	-	2.7	-	
Turn-On Delay Time	td(on)	-	18	-	ns
Rise Time	tr	-	25	-	
Turn-Off Delay Time	td(off)	-	88	-	
Fall Time	tf	-	42	-	
Input Capacitance	Ciss	-	869	-	pF
Output Capacitance	Coss	-	82	-	
Reverse Transfer Capacitance	Crss	-	73	-	
Body Diode Reverse Recovery Time (IF=-4A,dl/dt=80A/μs)	trr	-	22.15	-	ns
Body Diode Reverse Recovery Charge (IF=-4A,dl/dt=80A/μs)	Qrr	-	6.61	-	nC
Gate-Resistance (VDS = 0 V, VGS = 0 V,f =1MHz)	Rg	-	8	-	Ω

3.Pulse Test: Pulse Width ≤300 μs, Duty Cycle ≤2.0%.

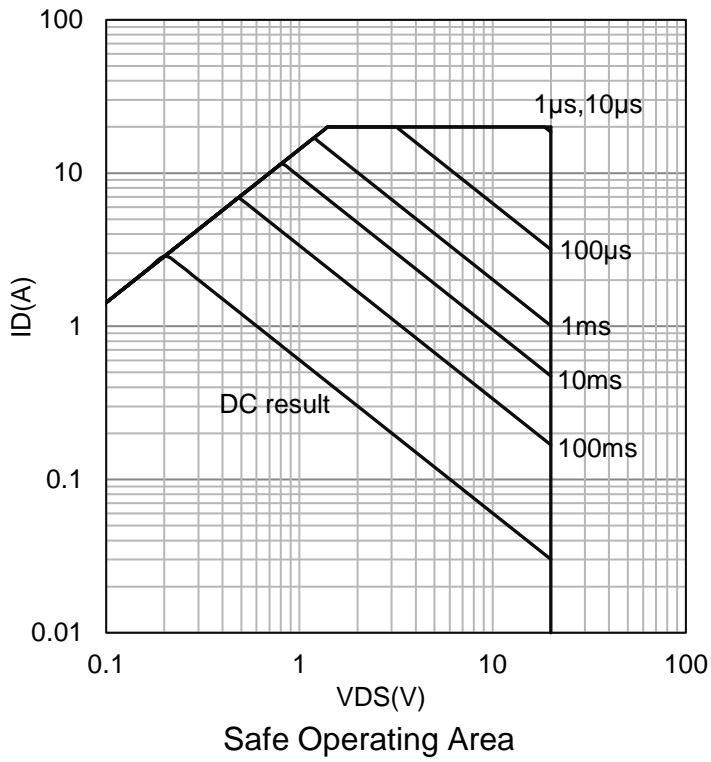
**7. ELECTRICAL CHARACTERISTICS CURVES**



**7. ELECTRICAL CHARACTERISTICS CURVES(Con.)**



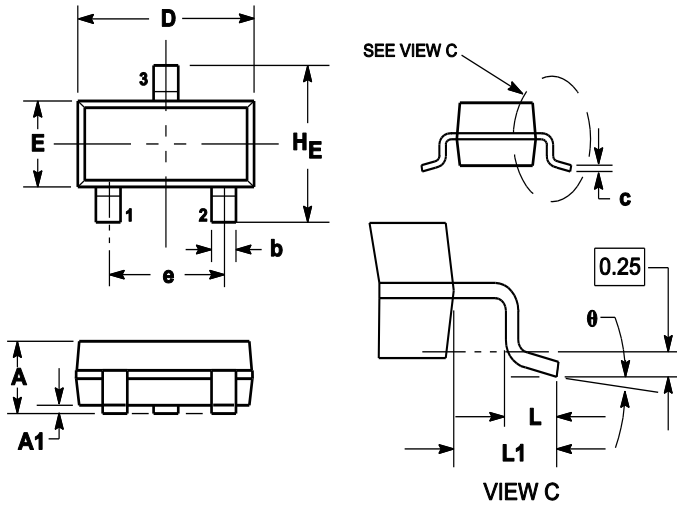
## 7. ELECTRICAL CHARACTERISTICS CURVES(Con.)



### 8. OUTLINE AND DIMENSIONS

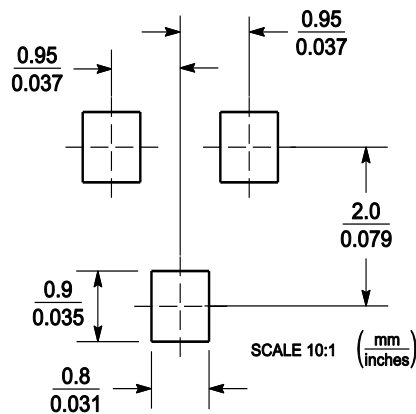
Notes:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.



DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.89	1	1.11	0.035	0.04	0.044
A1	0.01	0.06	0.1	0.001	0.002	0.004
b	0.37	0.44	0.5	0.015	0.018	0.02
c	0.09	0.13	0.18	0.003	0.005	0.007
D	2.80	2.9	3.04	0.11	0.114	0.12
E	1.20	1.3	1.4	0.047	0.051	0.055
e	1.78	1.9	2.04	0.07	0.075	0.081
L	0.10	0.2	0.3	0.004	0.008	0.012
L1	0.35	0.54	0.69	0.014	0.021	0.029
HE	2.10	2.4	2.64	0.083	0.094	0.104
theta	0°	---	10°	0°	---	10°

### 9. SOLDERING FOOTPRINT



单击下面可查看定价，库存，交付和生命周期等信息

[>>LRC\(乐山无线电\)](#)