

20V N-Channel Enhancement-Mode MOSFET

$V_{DS} = 20V$

$R_{DS(ON)}, V_{GS}@4.5V, I_{DS}@2.8A = 60m\Omega$

$R_{DS(ON)}, V_{GS}@2.5V, I_{DS}@2.0A = 115m\Omega$

Features

High Density Cell Design For Ultra Low On-Resistance

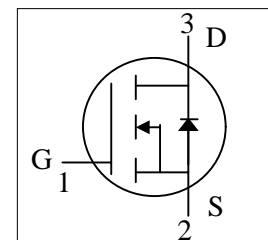
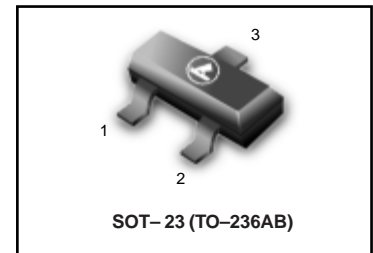
Improved Shoot-Through FOM

we declare that the material of product compliance with RoHS requirements.

S- Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable.

▼ High Density Cell Design For Ultra Low On - Resistance
Improved Shoot-Through FOM

LN2302LT1G
S-LN2302LT1G



Ordering Information

Device	Marking	Shipping
LN2302LT1G S-LN2302LT1G	N02	3000/Tape & Reel
LN2302LT3G S-LN2302LT3G	N02	10,000/Tape & Reel

Maximum Ratings and Thermal Characteristics ($T_A = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	V_{DS}	20	V	
Gate-Source Voltage	V_{GS}	± 8		
Continuous Drain Current	I_D	2.3	A	
Pulsed Drain Current ¹⁾	I_{DM}	8		
Maximum Power Dissipation	P_D	$T_A = 25^\circ C$	0.9	W
		$T_A = 75^\circ C$	0.57	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ C$	
Junction-to-Case Thermal Resistance	R_{qJC}		$^\circ C/W$	
Junction-to-Ambient Thermal Resistance (PCB mounted) ²⁾	R_{qJA}	145		

Note: 1. Repetitive Rating; Pulse width limited by the Maximum junction temperature

2. 1-in² 2oz Cu PCB board

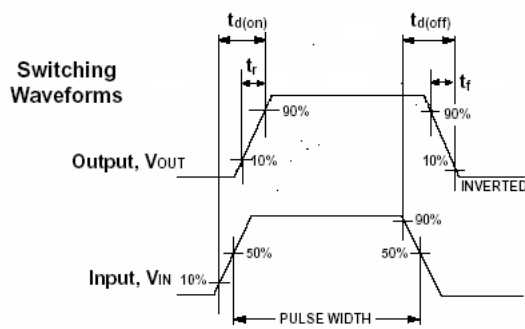
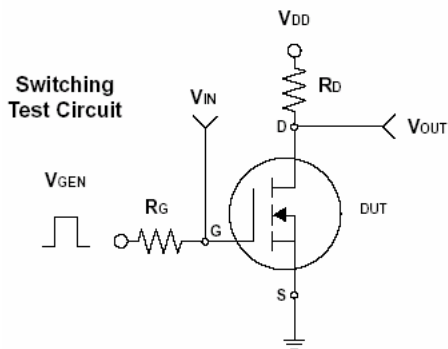
3. Guaranteed by design; not subject to production testing

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ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS} = 0V, I_D = 250\mu A$	20	-	-	V
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 4.5V, I_D = 2.8A$		40	60	mΩ
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 2.5V, I_D = 2.0A$		50	115	
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	0.60	0.95	1.20	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 9.6V, V_{GS} = 0V$			-1	μA
Gate Body Leakage	I_{GSS}	$V_{GS} = \pm 8V, V_{DS} = 0V$			±100	nA
Gate Resistance	R_g					Ω
Forward Transconductance	g_{fs}	$V_{DS} = 5V, I_D = 4.0A$		6.5		S
Dynamic ³⁾						
Total Gate Charge	Q_g	$V_{DS} = 6V, I_D = 2.8A$ $V_{GS} = 4.5V$		3.69		nC
Gate-Source Charge	Q_{gs}			0.70		
Gate-Drain Charge	Q_{gd}			1.06		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 6V, R_L = 6\Omega$ $I_D = 1A, V_{GEN} = 4.5V$ $R_G = 6\Omega$		6.16		ns
Turn-On Rise Time	t_r			7.56		
Turn-Off Delay Time	$t_{d(off)}$			16.61		
Turn-Off Fall Time	t_f			4.07		
Input Capacitance	C_{iss}	$V_{DS} = 6V, V_{GS} = 0V$ $f = 1.0\text{ MHz}$		427.12		pF
Output Capacitance	C_{oss}			80.56		
Reverse Transfer Capacitance	C_{rss}			57.00		
Source-Drain Diode						
Max. Diode Forward Current	I_S				1.6	A
Diode Forward Voltage	V_{SD}	$I_S = -1.6A, V_{GS} = 0V$			1.2	V

Note: Pulse test: pulse width ≤ 300μs, duty cycle ≤ 2%



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TYPICAL ELECTRICAL CHARACTERISTICS

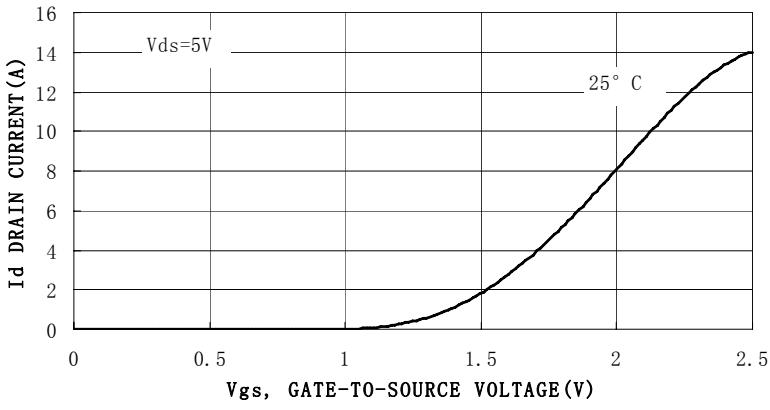


Figure 1. Transfer Characteristics

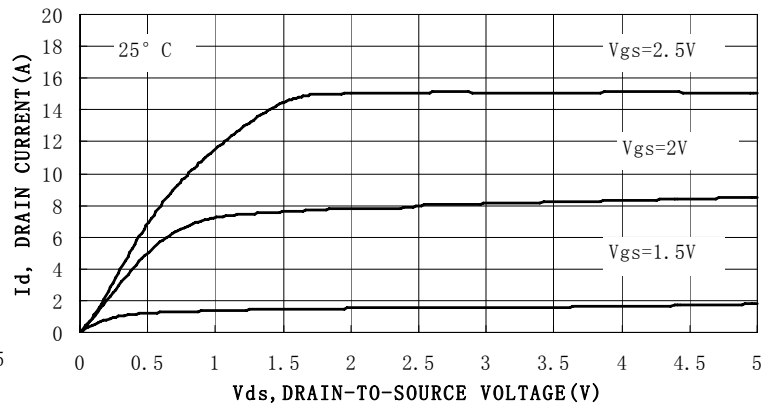


Figure 2. On-Region Characteristics

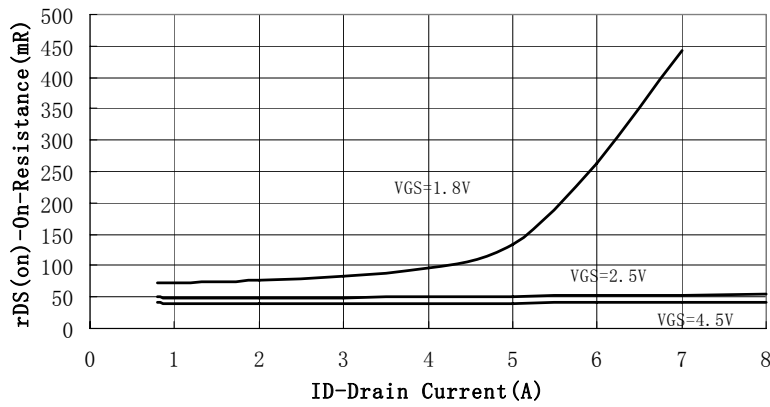


Figure 3. On-Resistance versus Drain Current

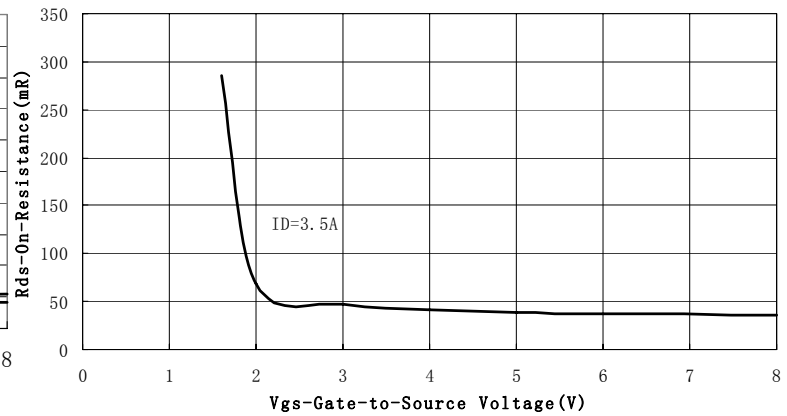


Figure 4. On-Resistance vs. Gate-to-Source Voltage

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TYPICAL ELECTRICAL CHARACTERISTICS

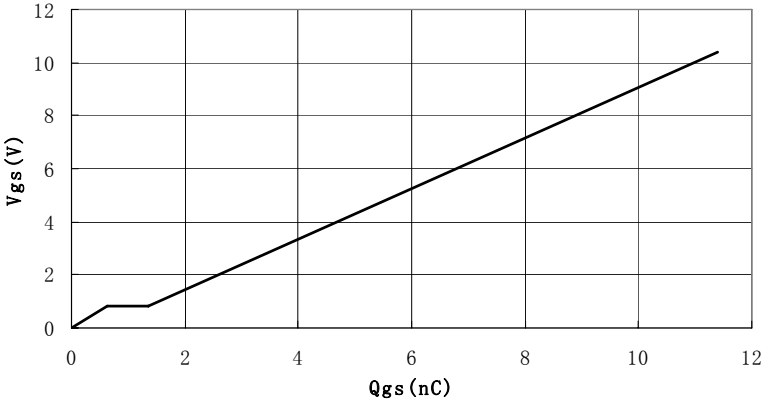


Figure 5. Gate Charge

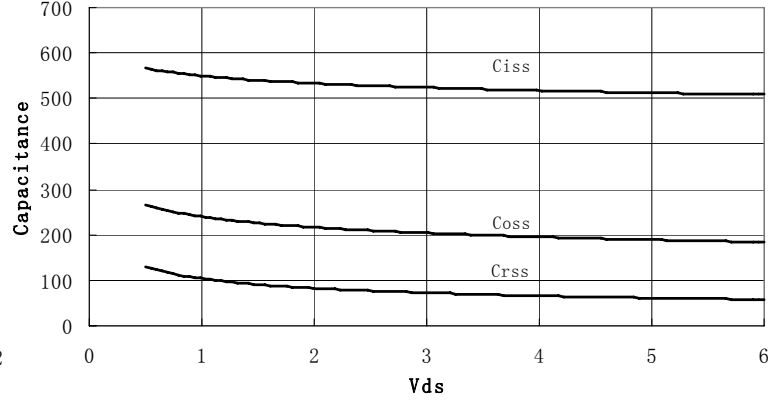


Figure 6. Capacitance

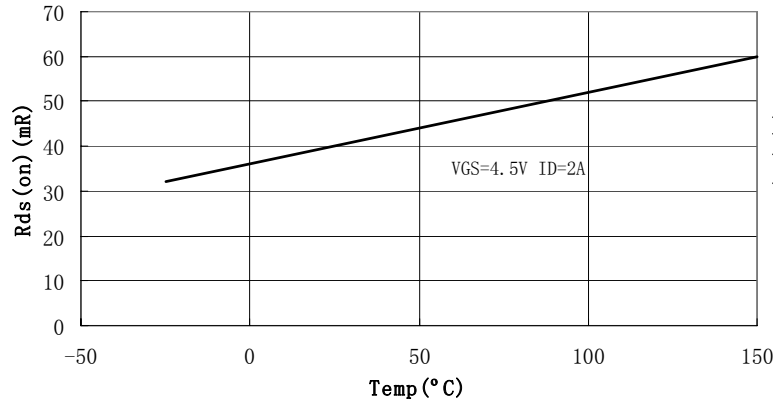


Figure 7. On-Resistance Vs. Junction Temperature

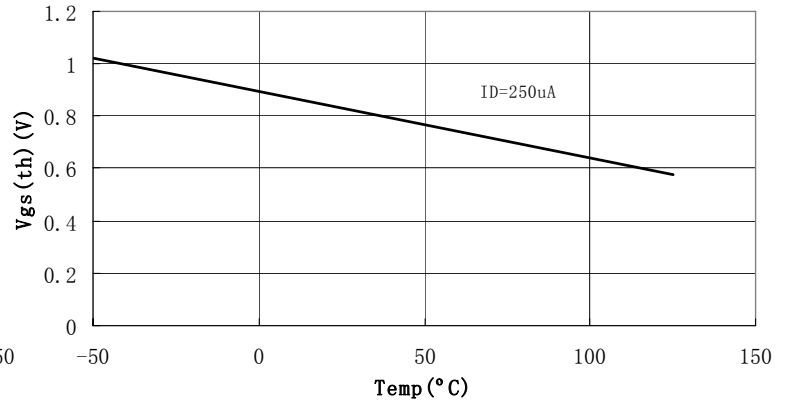


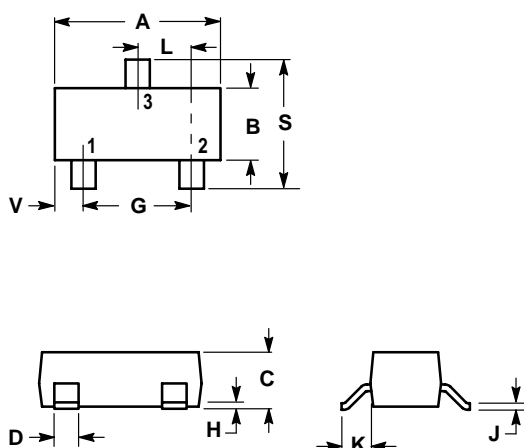
Figure 8. Vth Vs. Junction Temperature

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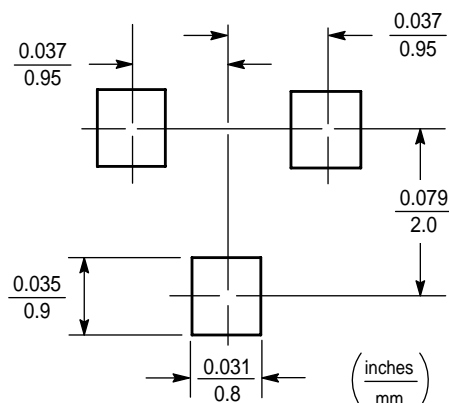
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NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M,1982
2. CONTROLLING DIMENSION: INCH.



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.1102	0.1197	2.80	3.04
B	0.0472	0.0551	1.20	1.40
C	0.0350	0.0440	0.89	1.11
D	0.0150	0.0200	0.37	0.50
G	0.0701	0.0807	1.78	2.04
H	0.0005	0.0040	0.013	0.100
J	0.0034	0.0070	0.085	0.177
K	0.0140	0.0285	0.35	0.69
L	0.0350	0.0401	0.89	1.02
S	0.0830	0.1039	2.10	2.64
V	0.0177	0.0236	0.45	0.60



单击下面可查看定价，库存，交付和生命周期等信息

[>>LRC\(乐山无线电\)](#)