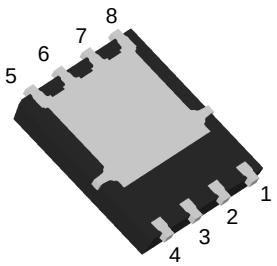
S-LN74095HCDT3WG

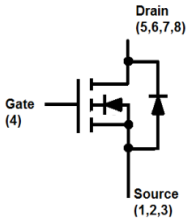
40V N-Channel Power MOSFET



CDFN5060-8H

1. FEATURES

- RDS(on)≤0.95mΩ@VGS=10V.
- Low thermal impedance.
- Fast switching speed.
- We declare that the material of product compliance with RoHS requirements and Halogen Free.
- S-prefix for automotive and other applications requiring unique site and control change requirements; AEC-Q101 qualified and PPAP capable.



2. APPLICATIONS

- Power Tools
- UPS
- Motor Control

3. DEVICE MARKING AND RESISTOR VALUES

Device	Marking	Shipping
S-LN74095HCDT3WG	LN74095HC	5000/Tape&Reel

4. MAXIMUM RATINGS

Parameter		Symbol	Limits	Unit
Drain−to−Source Voltage		VDS	40	V
Gate−to−Source Voltage		VGS	± 20	V
Continuous Drain Current(Note 1)	TA =25°C	ID	40	A
	TA =100°C		25	
Pulsed Drain Current(Note 2)	TA =25°C	IDM	160	
Continuous Drain Current	TC =25°C	ID	200	A
	TC =100°C		120	
Pulsed Drain Current	TC =25°C	IDM	800	
Avalanche Current		IAS	51	A
Avalanche energy(L=0.1mH)		EAS	130	mJ
Power Dissipation(Note 1)	TA =25°C	PD	3.3	W
	TA =100°C		1.7	
Power Dissipation	TC =25°C		100	
	TC =100°C		50	
Operating Junction and Storage Temperature Range		TJ , TSTG	-55~+175	℃

5. THERMAL CHARACTERISTICS

Parameter	Symbol	Max	Unit
Junction-to-Ambient(Note 1)	RθJA	45	℃/W
Junction-to-Case	RθJC	1.5	

Note:1.Surface mounted on "1.5in x 1.5in" FR4 board using 1*1 in pad, 2 oz Cu.

2.Pulse width limited by maximum junction temperature.

6. ELECTRICAL CHARACTERISTICS(TJ=25℃ unless otherwise specified)

Characteristic		Symbol	Min.	Typ.	Max.	Unit
Static						
Drain to Source Breakdown Voltage (VGS = 0 V, ID = 250 μA)		BVDSS	40	-	-	V
Gate-Source Threshold Voltage (VDS = VGS , ID = 250 uA)		VGS(th)	2.1	2.5	3.1	V
Gate-Body Leakage (VDS = 0 V, VGS = ±20 V)		IGSS	-	-	±100	nA
Zero Gate Voltage Drain Current (VDS = 40 V, VGS = 0 V)		IDSS	-	-	1	μA
Drain-Source On-Resistance(Note 3) (VGS = 10 V, ID = 30 A) (VGS = 7 V, ID = 30 A)		RDS(on)	- -	0.85 -	0.95 2	mΩ
Dynamic						
Input Capacitance	(VDS = 20 V, VGS = 0 V, f = 100kHz)	Ciss	-	3612	-	pF
Output Capacitance		Coss	-	1408	-	
Reverse Transfer Capacitance		Crss	-	205	-	
Total Gate Charge	(VDS = 20 V, VGS = 10 V,ID = 30 A)	Qg	-	69	-	nC
Gate-Source Charge		Qgs	-	17.2	-	
Gate-Drain Charge		Qgd	-	23	-	
Turn-On Delay Time	(VDS = 20 V, ID = 30 A, VGS = 10 V, RG = 6 Ω)	td(on)	-	28	-	ns
Rise Time		tr	-	37	-	
Turn-Off Delay Time		td(off)	-	64	-	
Fall Time		tf	-	45	-	
Gate Resistance (VDS = 0 V,VGS = 0 V,f = 1.0MHz)		Rg	-	1	-	Ω
Diode characteristics						
Diode Continuous Current TC =25° C		IS	-	-	100	A
Diode Plused Current TC =25° C		ISM	-	-	400	A
Diode Forward Voltage (IS = 20 A,VGS = 0 V)		VSD	-	0.75	1.3	V
Reverse Recovery Time (VR=20V,IF=20A,dIF/dt=100A/us)		trr	-	96	-	ns
Reverse Recovery Charge (VR=20V,IF=20A,dIF/dt=100A/us)		Qrr	-	144	-	nC
Reverse Recovery Current (VR=20V,IF=20A,dIF/dt=100A/us)		IRRM	-	3.05	-	A

3.Pulse test: PW ⩽ 300us duty cycle ⩽ 2%.

7. ELECTRICAL CHARACTERISTICS CURVES

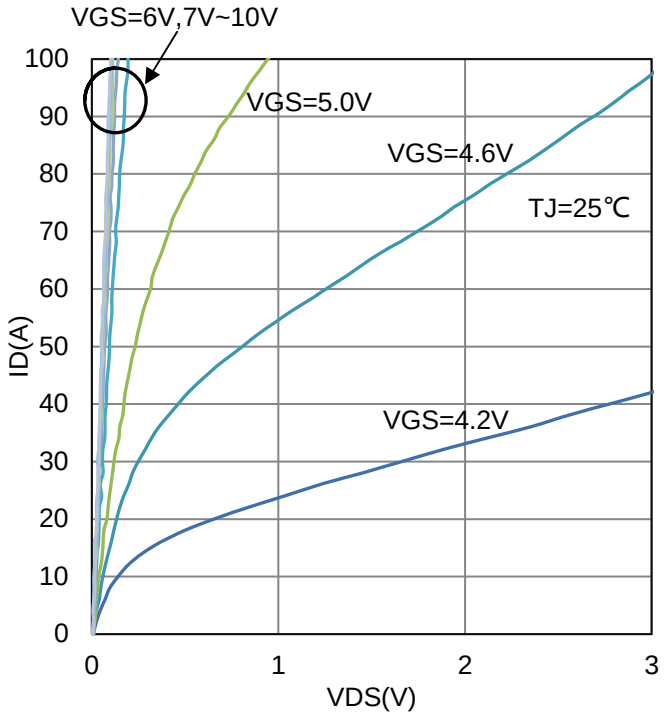


Figure 1.ID vs. VDS

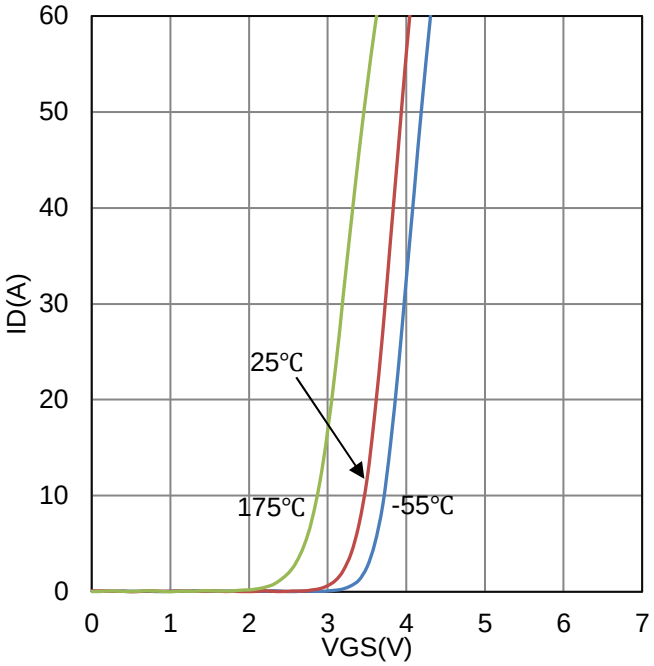


Figure 2.ID vs. VGS

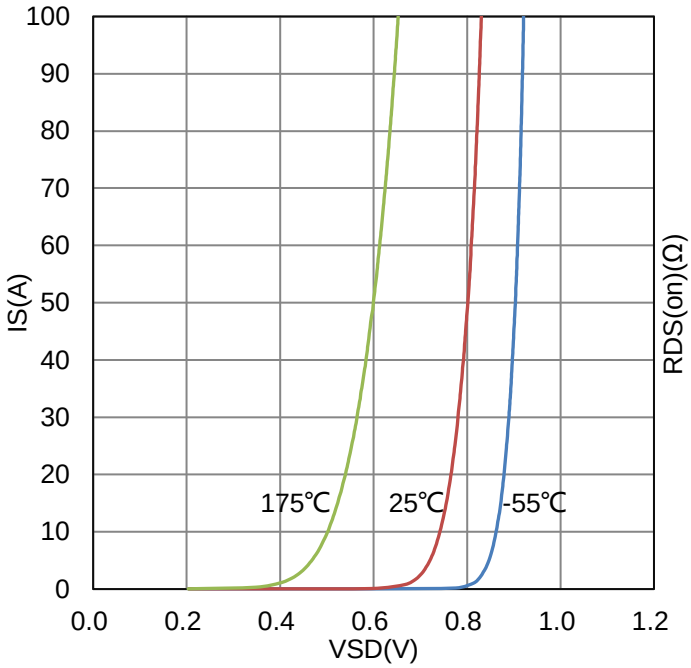


Figure 3.IS vs. VSD

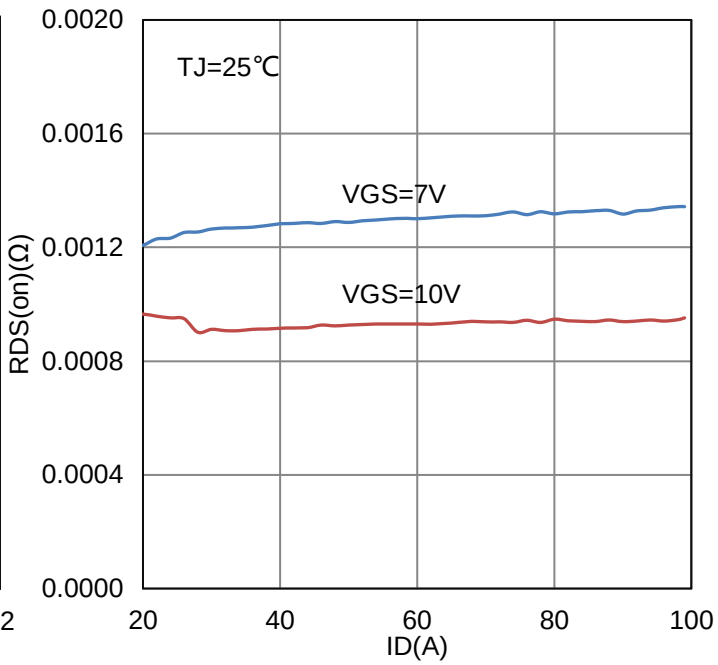


Figure 4.RDS(on) vs. ID

7. ELECTRICAL CHARACTERISTICS CURVES(Con.)

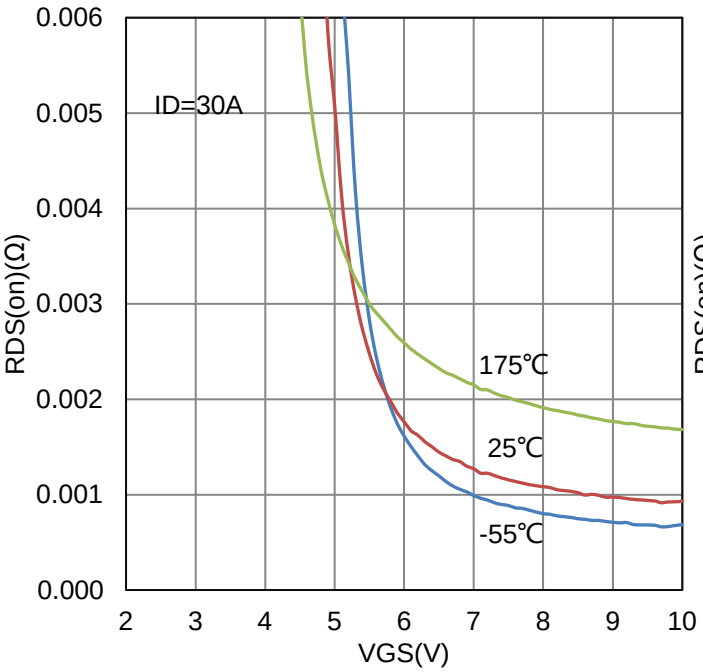


Figure 5.RDS(on) vs. VGS

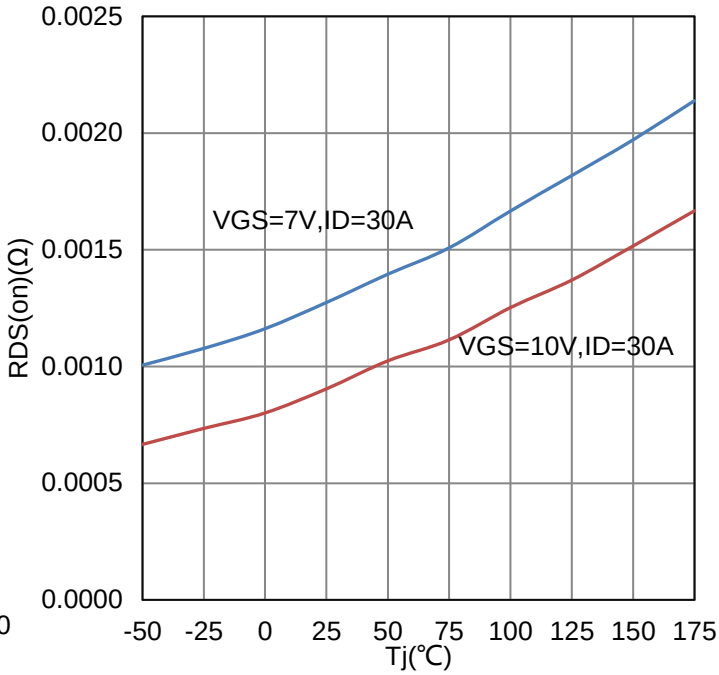


Figure 6.RDS(on) vs. Tj

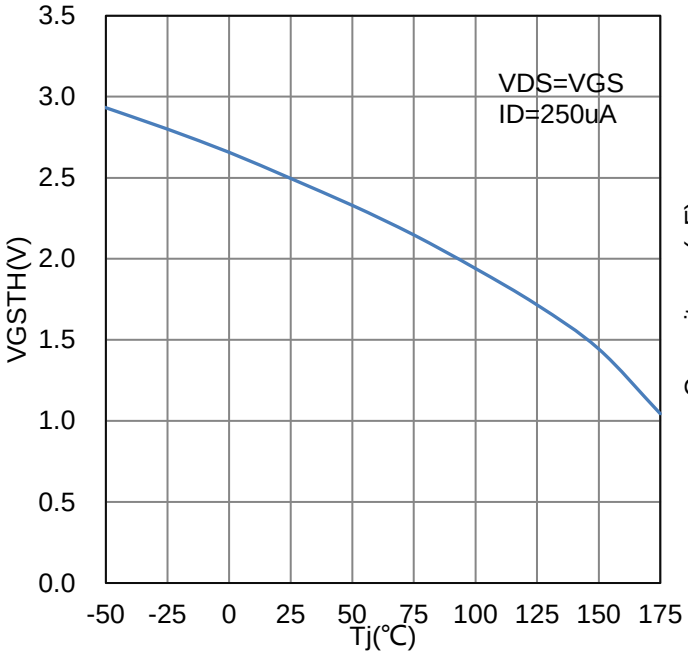


Figure 7.VGSth vs. Tj

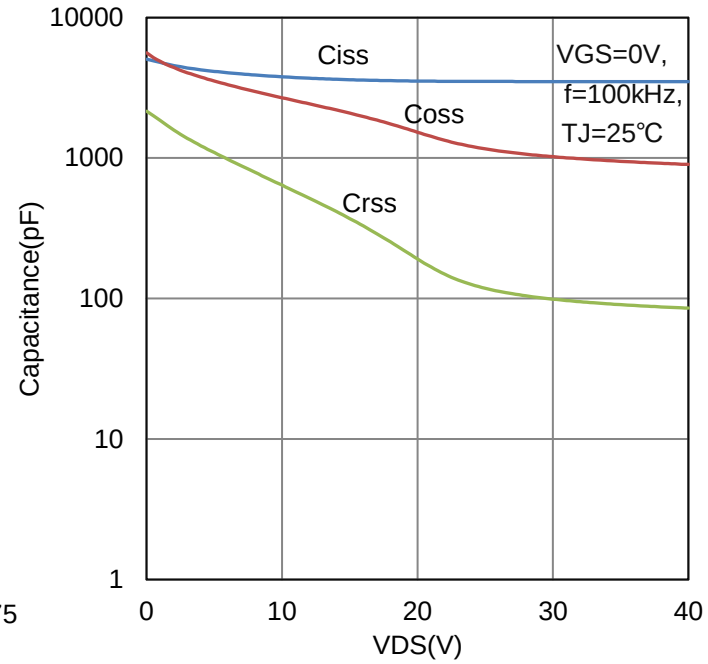


Figure 8.Capacitance

7. ELECTRICAL CHARACTERISTICS CURVES(Con.)

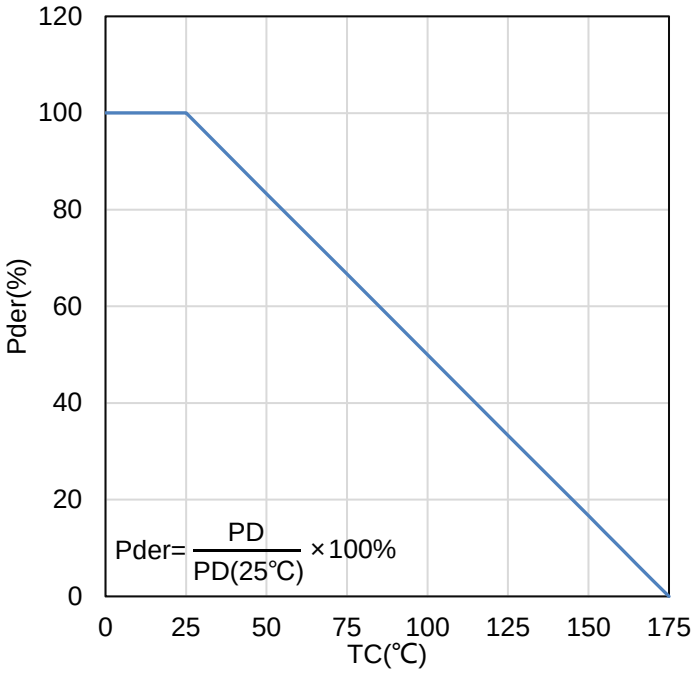


Figure 9.Normalized Derating Curve

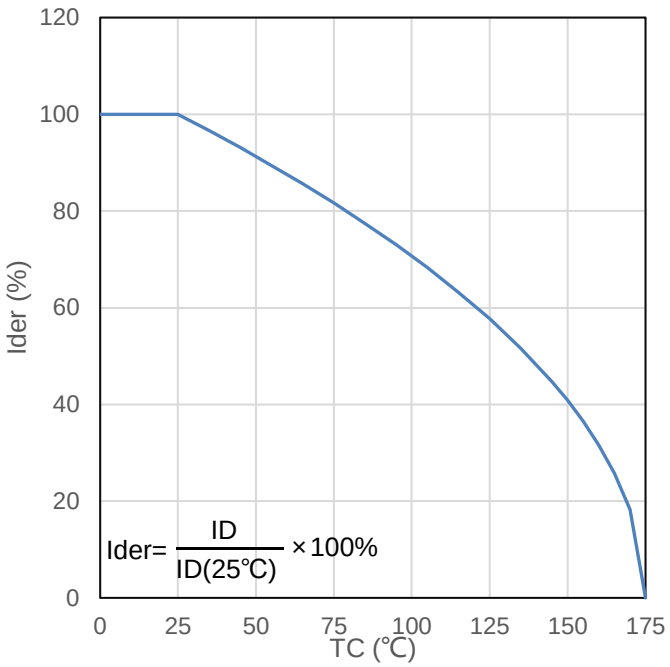


Figure 10.Normalized drain Current

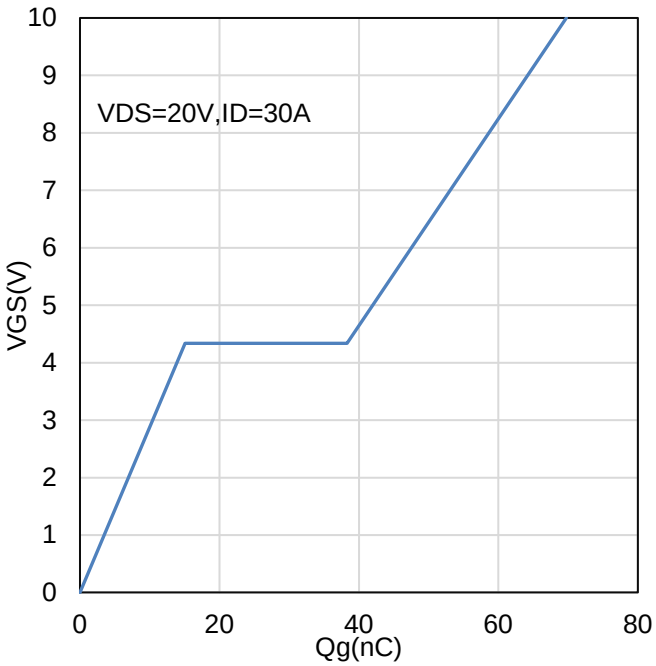


Figure 11.VGS vs. Qg

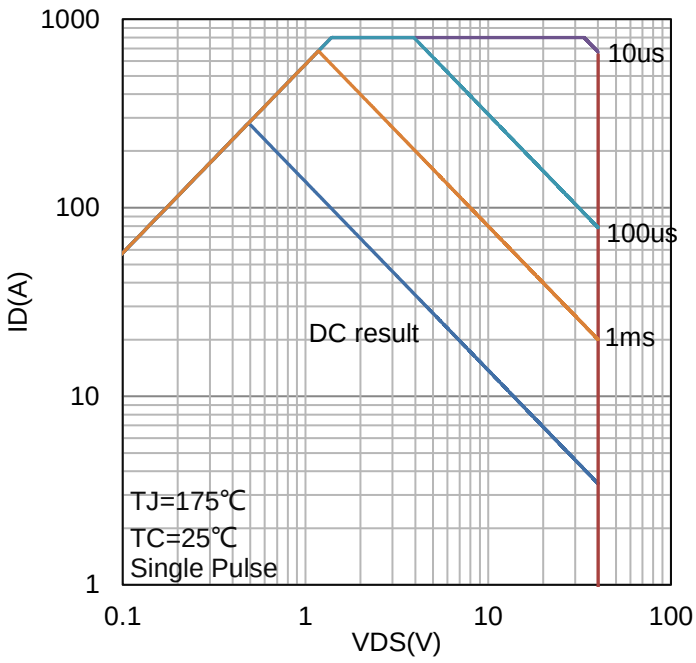


Figure 12.Safe Operating Area

7. ELECTRICAL CHARACTERISTICS CURVES(Con.)

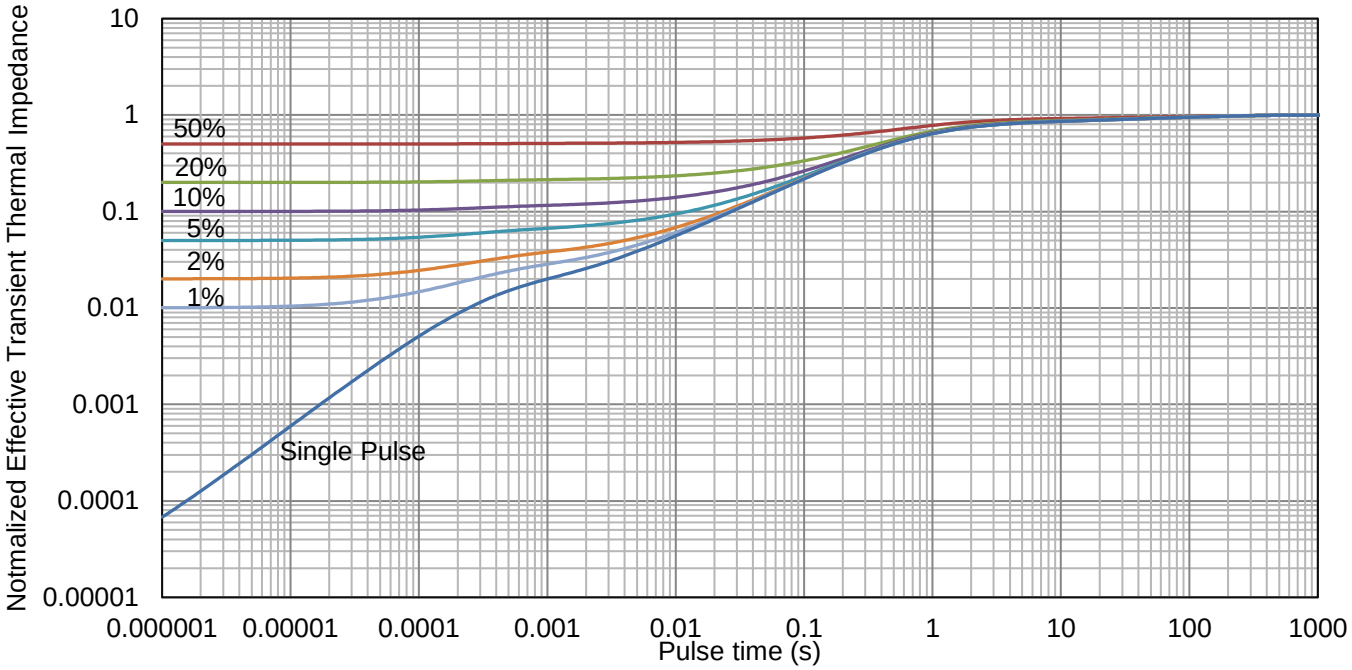
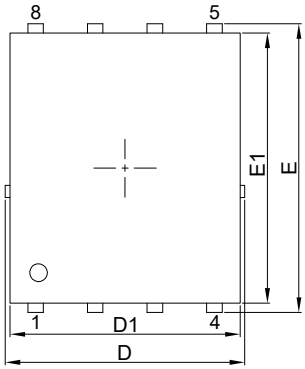


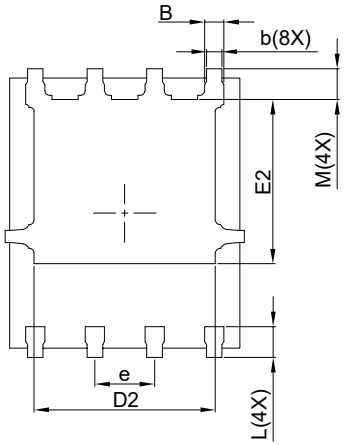
Figure 13.Thermal Response

8.OUTLINE AND DIMENSIONS

CDFN5060-8H(T1.00)

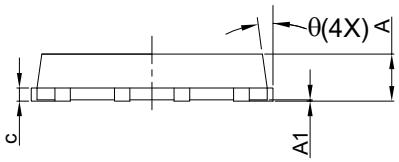


TOP VIEW



BOTTOM VIEW

CDFN5060-8H			
DIM	MIN	NOR	MAX
A	0.90	1.00	1.10
A1	0.00	0.02	0.05
E	6.00	6.15	6.30
E1	5.66	5.76	5.86
E2	3.40	3.50	3.60
D	4.95	5.10	5.25
D1	4.80	4.90	5.00
D2	3.76	3.86	3.96
b	0.30	0.35	0.40
B	0.36	0.41	0.46
L	0.56	0.66	0.76
M	0.56	0.66	0.76
e	1.27BSC		
c	0.254REF.		
θ	0 °	-	12°

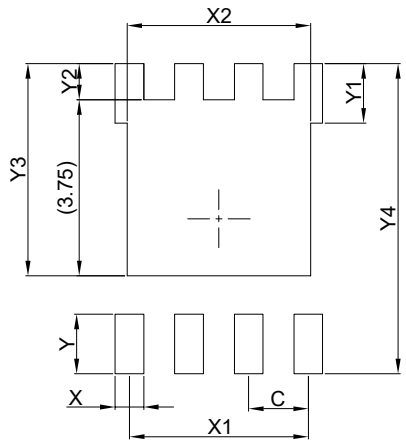


SIDE VIEW

GENERAL NOTES

1. Top package surface finish Ra Max0.4um
2. Bottom package surface finish Ra Max0.4um
3. Side package surface finish Ra Max0.4um
4. Protrusion or Gate Burrs shall not exceed 0.05mm per side
5. Offcenter Max0.038mm; Mismatch Max 0.038mm.

9.SOLDERING FOOTPRINT



CDFN5060-8H	
DIM	(mm)
C	1.27
X	0.61
X1	3.81
X2	3.91
Y	1.27
Y1	1.27
Y2	0.77
Y3	4.52
Y4	6.61

DISCLAIMER

- Curve guarantee in the specification. The curve of test items with electric parameter is used as quality guarantee. The curve of test items without electric parameter is used as reference only.

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