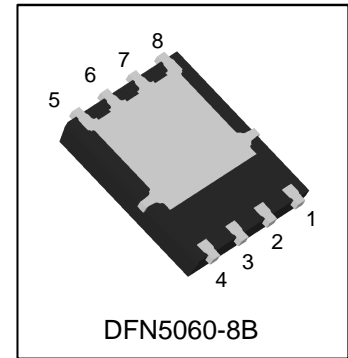


S-LP7411DT3WG

60V P-Channel (D-S) MOSFET

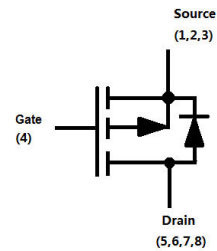


1. FEATURES

- Low RDS(on) trench technology
- Low thermal impedance
- Fast switching speed
- We declare that the material of product compliance with RoHS requirements and Halogen Free.
- S- prefix for automotive and other applications requiring unique site and control change requirements; AEC-Q101 qualified and PPAP capable.

2. APPLICATIONS

- Load Switches
- DC/DC Conversion
- Motor Drives



3. DEVICE MARKING AND ORDERING INFORMATION

Device	Marking	Shipping
S-LP7411DT3WG	LP7411	5000/Tape&Reel

4. MAXIMUM RATINGS(Ta = 25°C)

Parameter	Symbol	Limits	Unit
Drain-Source Voltage	VDS	-60	V
Gate-Source Voltage	VGS	±20	
Continuous Drain Current (Note1)	ID	TA = 25°C	-13
		TA = 100°C	-8
Pulsed Drain Current (Note2)	IDM	-52	A
Continuous Drain Current (Note1)	ID	TC = 25°C	-48
		TC = 100°C	-30
Pulsed Drain Current (Note2)	IDM	-192	A
Avalanche Current	IAS	49	
Avalanche energy(L=0.1mH)	EAS	120.05	mJ
Power Dissipation (Note1)	PD	TA = 25°C	3
		TC = 25°C	41.6
Operating Junction and Storage Temperature Range	TJ,Tstg	-55~+150	°C

5. THERMAL CHARACTERISTICS

Parameter	Symbol	Limits	Unit
Maximum Junction-to-Ambient (Note1)	RθJA	42	°C/W
Maximum Junction-to-Ambient	RθJC	3	

1.Surface mounted on "1.5 x 1.5" FR4 board using 1 sq in pad, 2 oz Cu.

2.Pulse width limited by maximum junction temperature

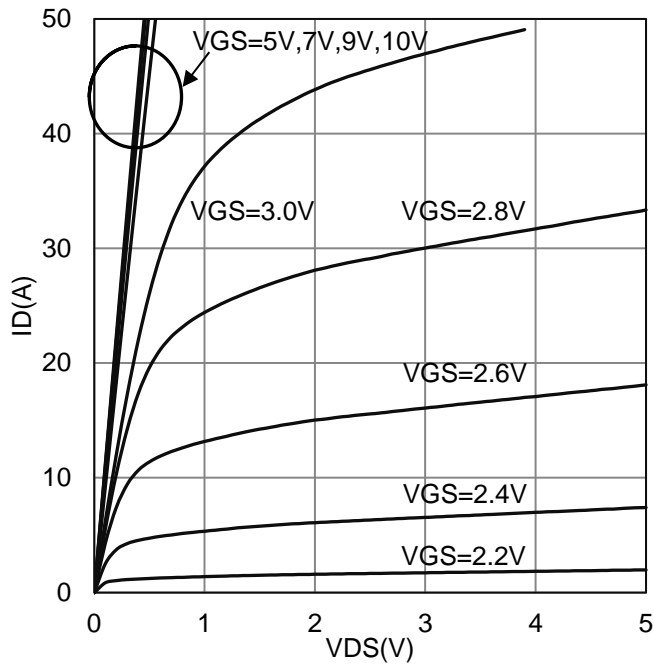
6. ELECTRICAL CHARACTERISTICS (Ta= 25°C)

Characteristic	Symbol	Min.	Typ.	Max.	Unit	
Static						
Drain–Source Breakdown Voltage (VGS = 0, ID = -250μA)	VBRDSS	-60	-	-	V	
Gate Threshold Voltage (VDS =VGS , ID =-250μA)	VGS(th)	-1	-	-3	V	
Gate Leakage Current (VDS =0V, VGS =±20V)	IGSS	-	-	±100	nA	
Zero Gate Voltage Drain Current (VDS = -48 V, VGS = 0 V)	IDSS	-	-	-1	μA	
Drain-Source On-Resistance(Note 3) (VGS = -10 V, ID = -9 A) (VGS = -4.5 V, ID = -8 A)	RDS(ON)	-	-	9.8 11.2	mΩ	
Diode Forward Voltage (Note 3) (IS = -3.6 A, VGS = 0 V)	VSD	-	-0.72	-1.2	V	
Dynamic(Note 4)						
Total Gate Charge	(VDS=-30V,VGS=-4.5V,ID=-9A)	Qg	-	66	-	nC
Gate-Source Charge		Qgs	-	17	-	
Gate-Drain Charge		Qgd	-	26	-	
Turn-On Delay Time	(VDS = -30 V, RL = 3.3 Ω, ID = -9 A, VGEN = -10 V, RGEN = 6 Ω)	td(on)	-	15	-	ns
Rise Time		tr	-	21	-	
Turn-Off Delay Time		td(off)	-	255	-	
Fall Time		tf	-	90	-	
Input Capacitance	(VDS = -30 V, VGS = 0 V, f = 1 MHz)	Ciss	-	7044	-	pF
Output Capacitance		Coss	-	382	-	
Reverse Transfer Capacitance		Crss	-	321	-	

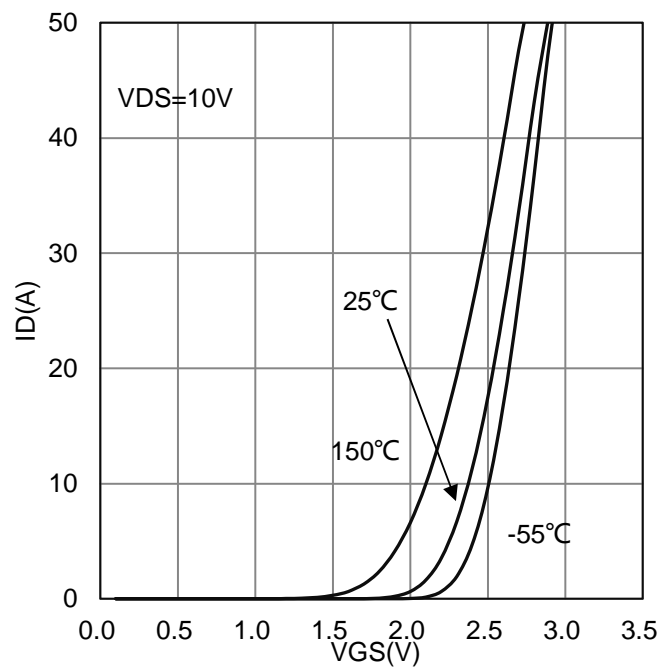
3.Pulse test: PW ≤ 300us duty cycle ≤ 2%.

4.Guaranteed by design, not subject to production testing.

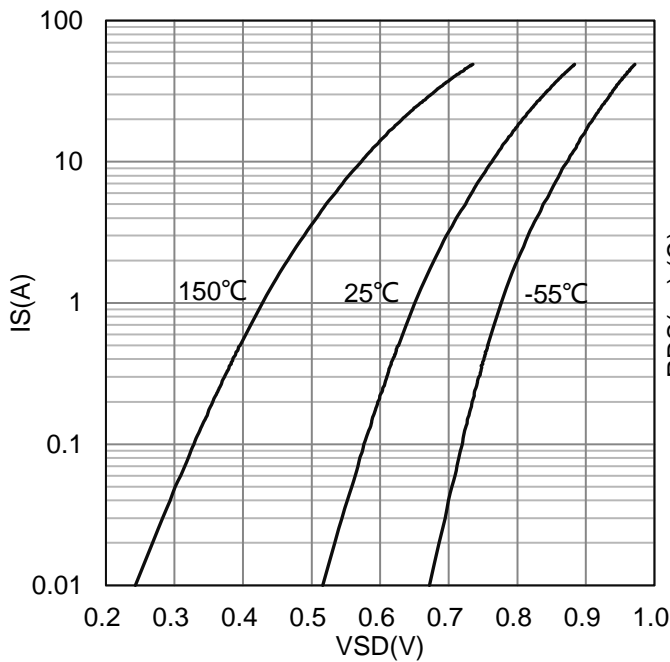
7. ELECTRICAL CHARACTERISTICS CURVES



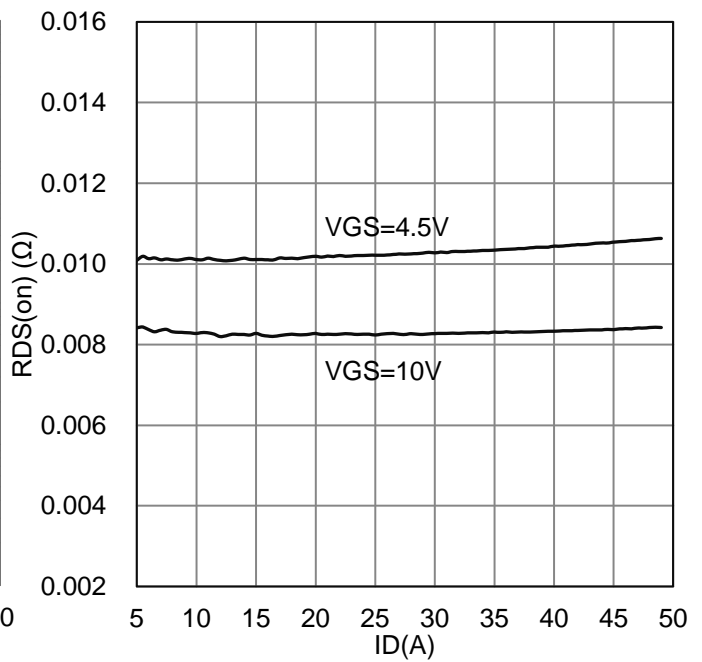
ID vs. VDS



ID vs. VGS

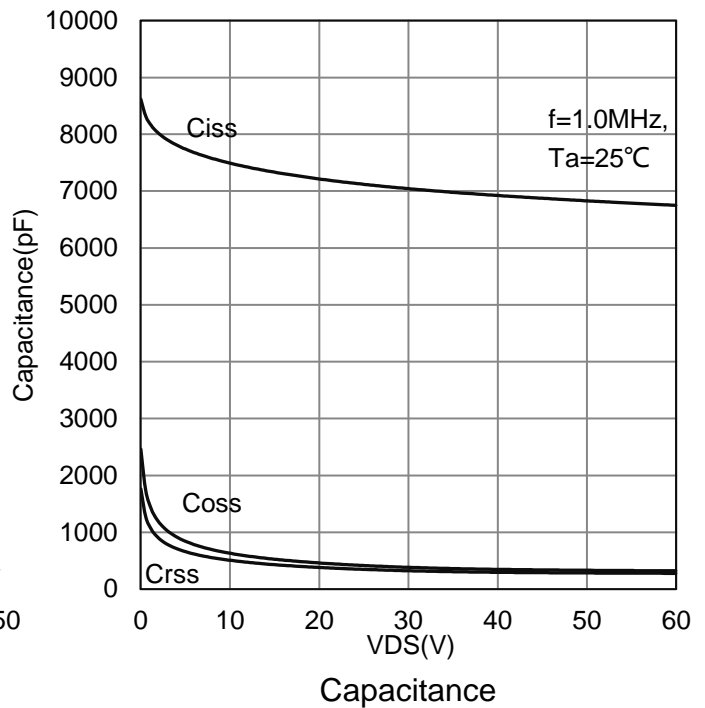
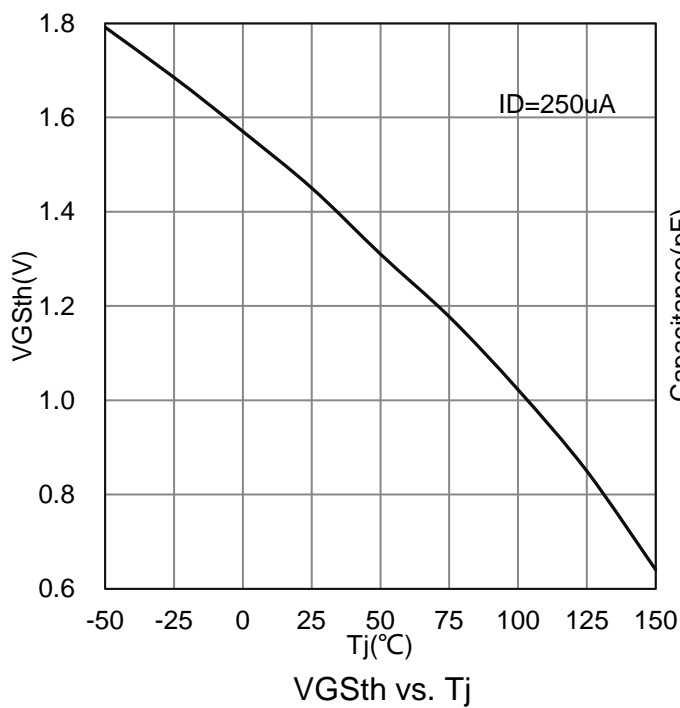
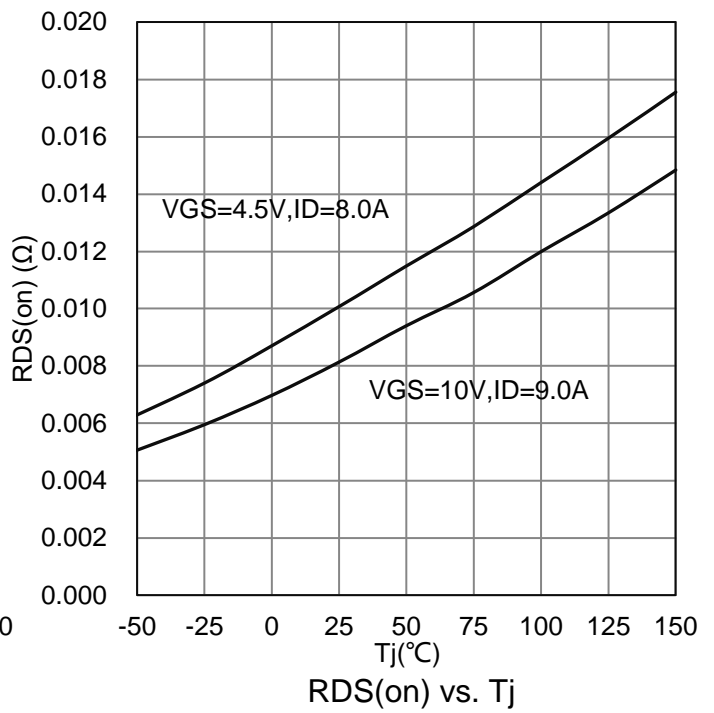
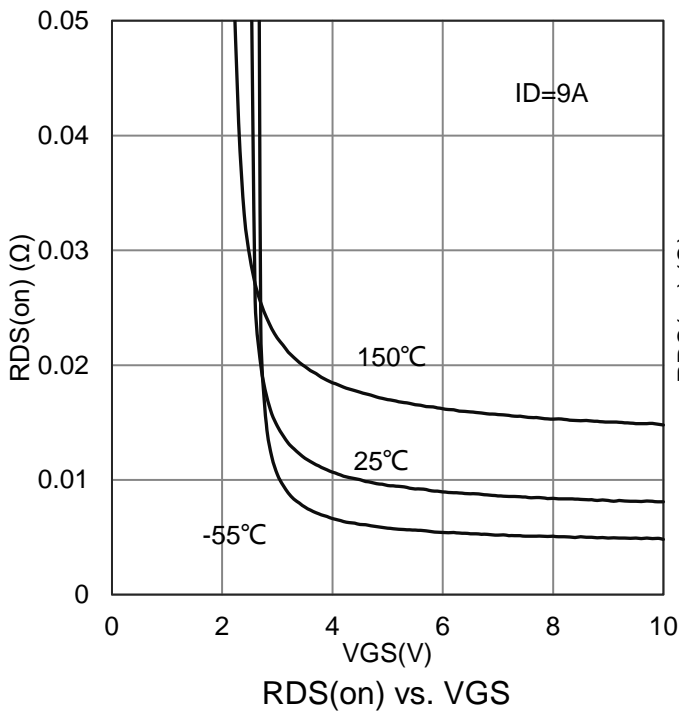


IS vs. VSD

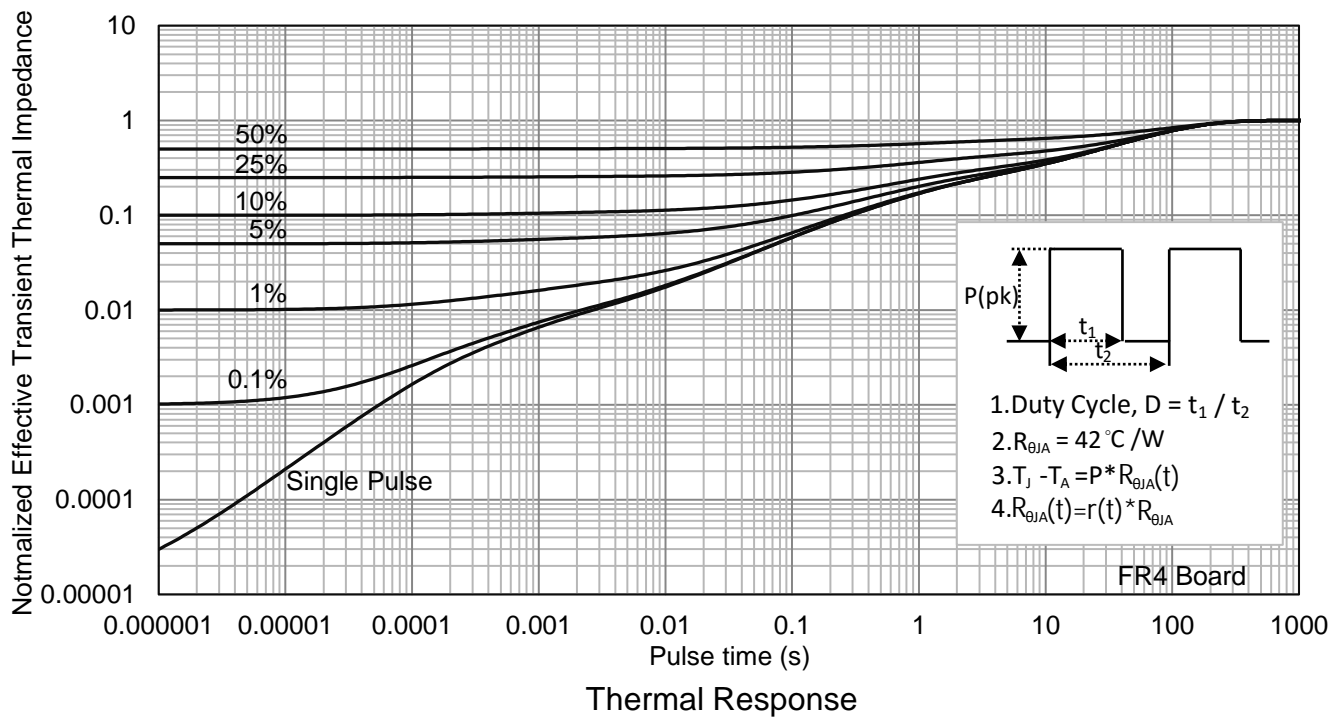
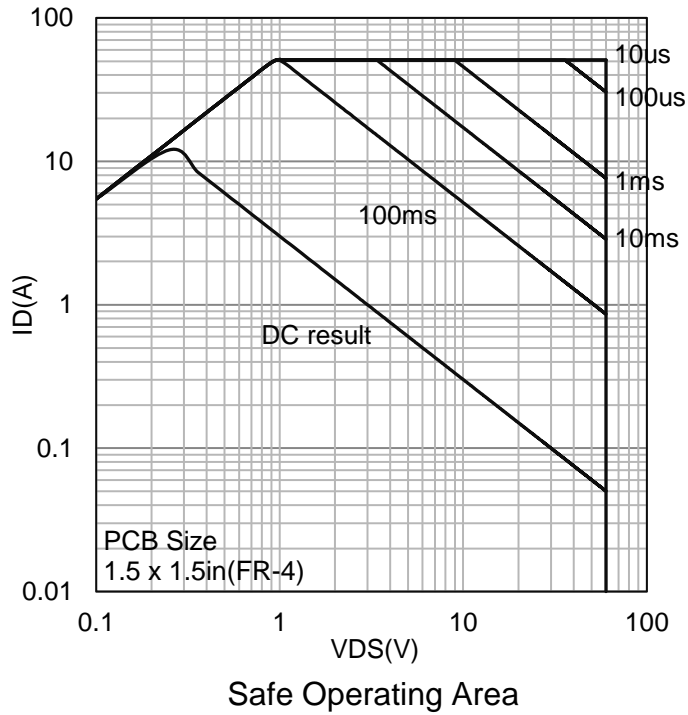


RDS(on) vs. ID

7. ELECTRICAL CHARACTERISTICS CURVES(Con.)

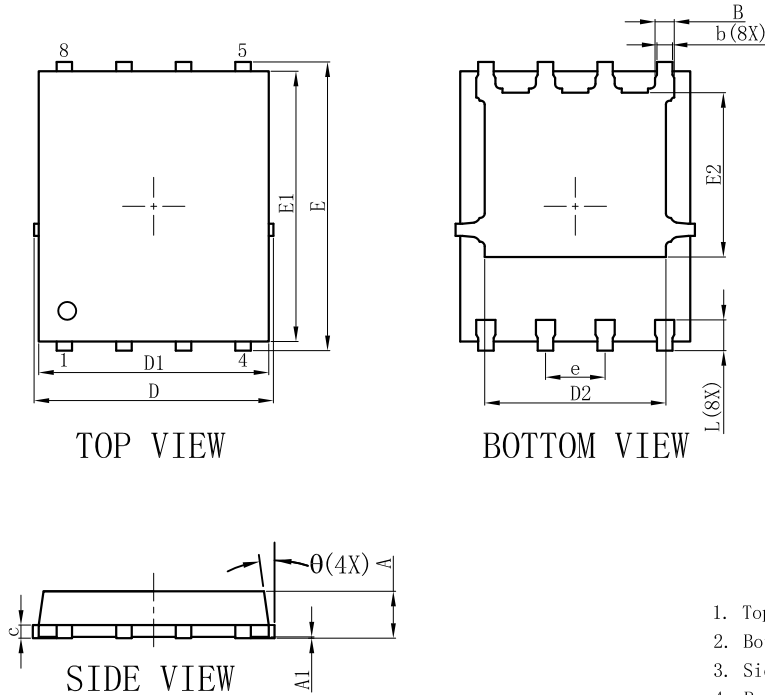


7. ELECTRICAL CHARACTERISTICS CURVES(Con.)



8. OUTLINE AND DIMENSIONS

DFN5060-8B

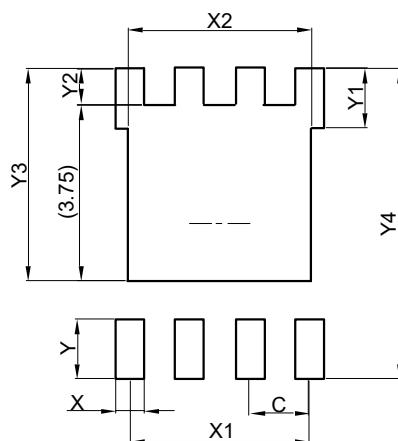


DFN5060-8B			
DIM	MIN	NOR	MAX
A	0.90	1.00	1.10
A1	0.00	0.02	0.05
E	6.00	6.15	6.30
E1	5.66	5.76	5.86
E2	3.40	3.50	3.60
D	4.95	5.10	5.25
D1	4.80	4.90	5.00
D2	3.76	3.86	3.96
b	0.30	0.35	0.40
B	0.36	0.41	0.46
L	0.56	0.66	0.76
e	1.27BSC		
c	0.254REF.		
θ	0°	-	12°
All Dimensions in mm			

GENERAL NOTES

1. Top package surface finish Ra0.4±0.2um
2. Bottom package surface finish Ra0.7±0.2um
3. Side package surface finish Ra0.4±0.2um
4. Protrusion or Gate Burrs shall not exceed 0.05mm per side.
5. Offcenter Max0.038mm; Mismatch Max 0.038mm.

9. SOLDERING FOOTPRINT



DFN5060-8B	
DIM	(mm)
C	1.27
X	0.61
X1	3.81
X2	3.91
Y	1.27
Y1	1.27
Y2	0.77
Y3	4.52
Y4	6.61

DISCLAIMER

- Curve guarantee in the specification. The curve of test items with electric parameter is used as quality guarantee. The curve of test items without electric parameter is used as reference only.
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