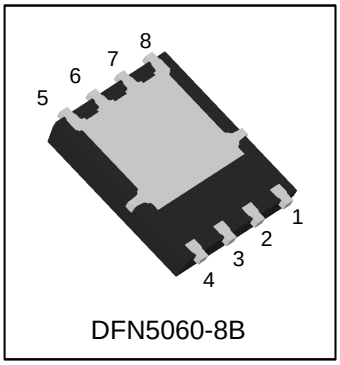
S-LN7266DT1WG

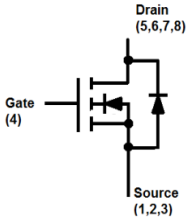
N-Channel 60-V (D-S) MOSFET



DFN5060-8B

1. FEATURES

- Low RDS(on) trench technology
- Low thermal impedance
- Fast switching speed
- We declare that the material of product compliance with RoHS requirements and Halogen Free.
- S- prefix for automotive and other applications requiring unique site and control change requirements; AEC-Q101 qualified and PPAP capable.



2. APPLICATIONS

- White LED boost converters
- Automotive Systems
- Industrial DC/DC Conversion Circuits

3. DEVICE MARKING AND RESISTOR VALUES

Device	Marking	Shipping
S-LN7266DT1WG	LN7266	3000/Tape&Reel

4. MAXIMUM RATINGS(Ta = 25ºC)

Parameter		Symbol	Limits	Unit
Drain-to-Source Voltage		VDS	60	V
Gate-to-Source Voltage		VGS	±20	V
Continuous Drain Current	TA=25℃	ID	13	A
	TA=70℃		11	
Pulsed Drain Current(Note 2)	TA=25℃	IDM	50	
Continuous Drain Current	TC=25℃	ID	37	A
	TC=100℃		23	
Pulsed Drain Current(Note 2)	TC=25℃	IDM	148	
Avalanche Current		IAS	15	A
Avalanche energy (L=0.1mH)		EAS	11.25	mJ
Power Dissipation(Note 1)	TA=25℃	PD	5	W
	TA=70℃		3.2	
	TC=25℃		41	
	TC=100℃		16	
Operating Junction and Storage Temperature Range		Tj/Tstg	-55~+175	℃

5. THERMAL CHARACTERISTICS

Parameter	Symbol	Value	Unit
Junction−to−Ambient(Note 1)	RθJA	50	℃/W
Junction−to−Case	RθJC	3	℃/W

1.Surface mounted on "1.5 x 1.5" FR4 board using 1 sq in pad, 2 oz Cu.

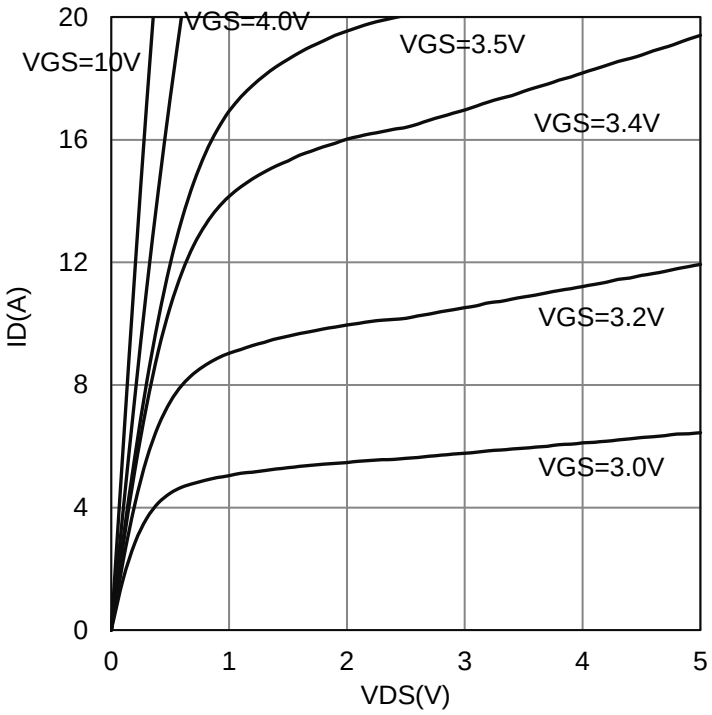
2.Pulse width limited by maximum junction temperature.

6. ELECTRICAL CHARACTERISTICS (Ta= 25°C)

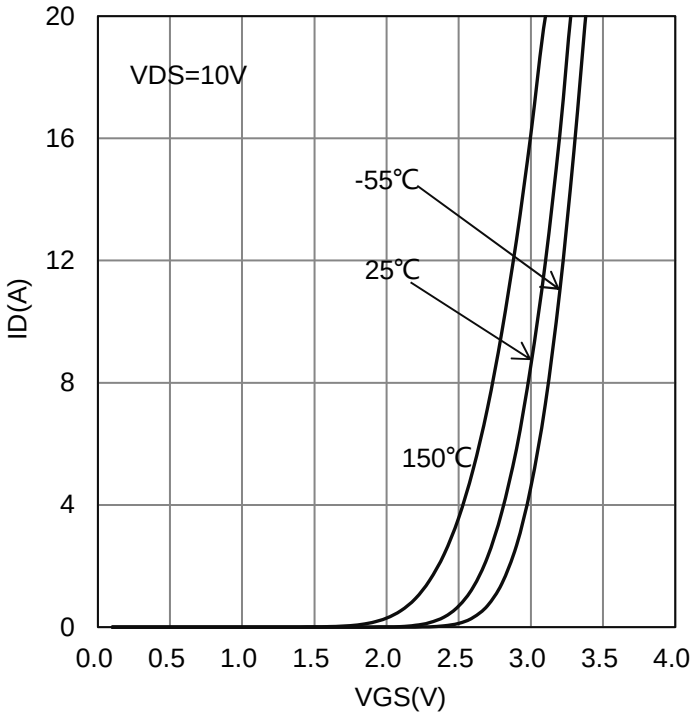
Characteristic		Symbol	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage (VGS = 0 V, ID = 250 uA)		V(BR)DSS	60	-	-	V
Gate-Source Threshold Voltage (VDS = VGS , ID = 250 μA)		VGS(th)	1	-	3	V
Gate-Body leakage current (VDS = 0 V, VGS = ±20 V)		IGSS	-	-	±10	μA
Zero Gate Voltage Drain Current (VDS = 48 V, VGS = 0 V)		IDSS	-	-	1	μA
Drain-to-Source On-Resistance(Note 3) (VGS = 10 V, ID = 11 A) (VGS = 4.5 V, ID = 7 A)		RDS(ON)	- -	16.5 20.5	18 24	mΩ
Diode Forward Voltage (IS = 2.3 A, VGS = 0 V)		VSD	-	0.7	1.2	V
Dynamic						
Total Gate Charge	(VDS = 30 V, VGS = 4.5 V,ID = 10.4 A)	Qg	-	12.4	-	nC
Gate to Source Charge		Qgs	-	5.3	-	
Gate to Drain Charge		Qgd	-	3.9	-	
Turn-on Delay Time	(VDS=30 V,RL=2.9 Ω,ID=10.4A,VGEN=10 V,RGEN=6Ω)	td(on)	-	10	-	nS
Rise Time		tr	-	24	-	
Turn-Off Delay Time		td(off)	-	67	-	
Fall Time		tf	-	37	-	
Input Capacitance	(VDS = 15 V, VGS = 0 V, f = 1 MHz)	Ciss	-	1669	-	pF
Output Capacitance		Coss	-	89	-	
Reverse Transfer Capacitance		Crss	-	72	-	
Gate-Resistance (VDS= 0 V,VGS = 0 V,f = 710.938kHz)		Rg	-	1.7	-	Ω

3.Pulse test: PW≤300μs duty cycle≤2%.

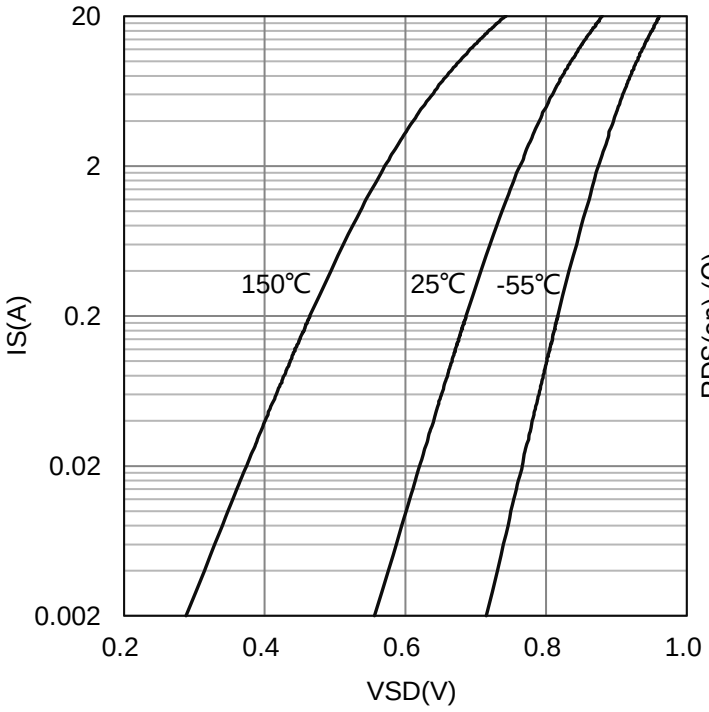
7.ELECTRICAL CHARACTERISTICS CURVES



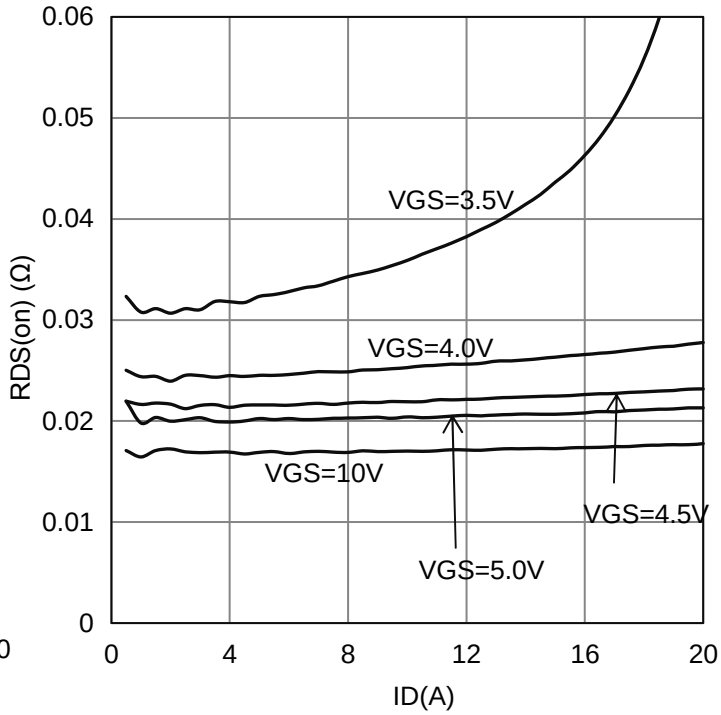
ID vs. VDS



ID vs. VGS

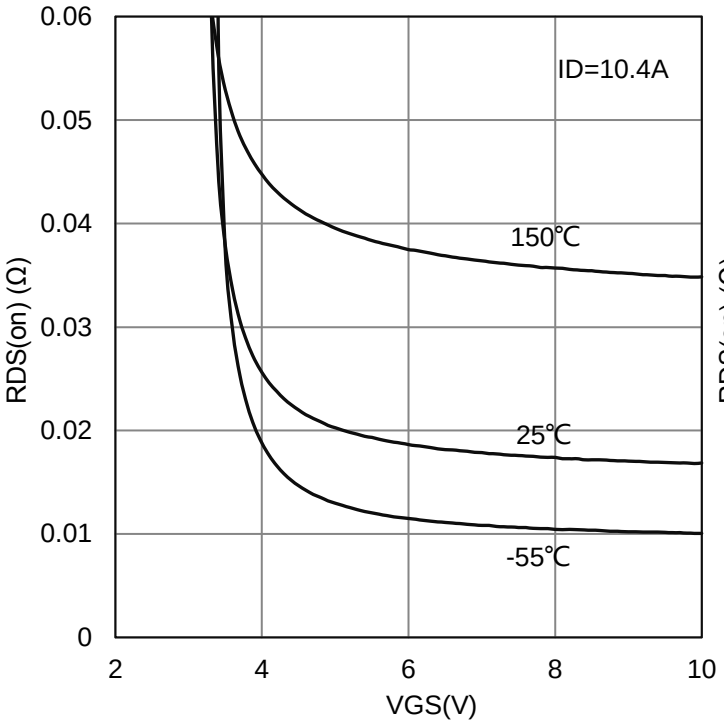


IS vs. VSD

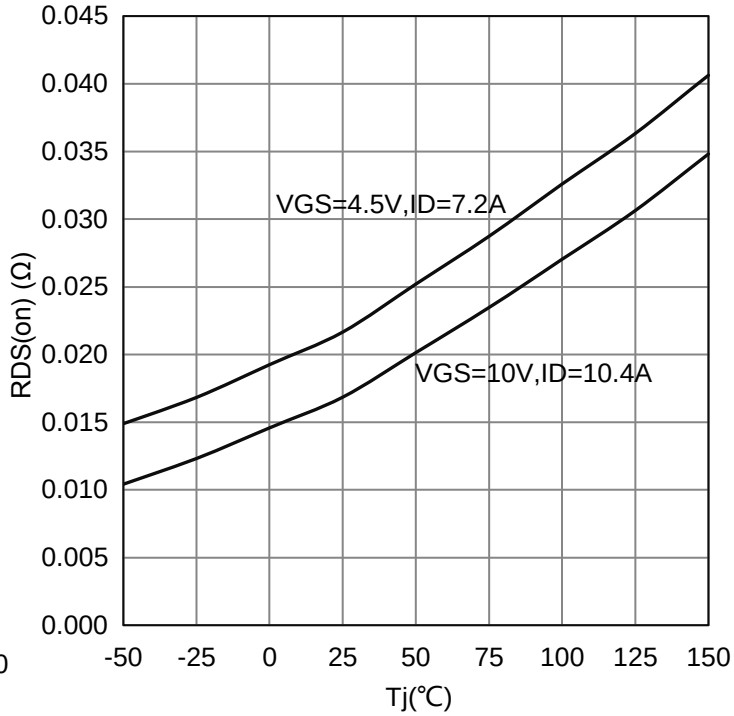


RDS(on) vs. ID

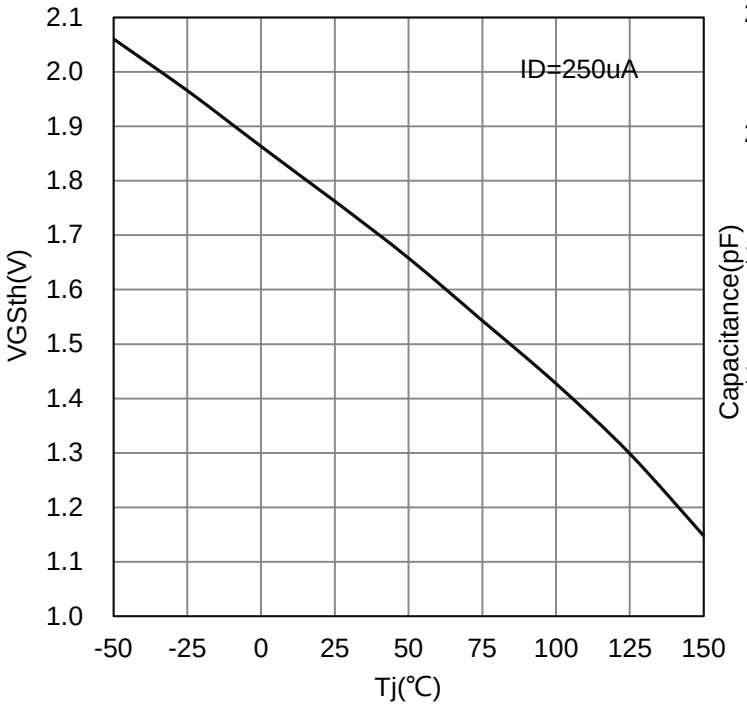
7.ELECTRICAL CHARACTERISTICS CURVES(Con.)



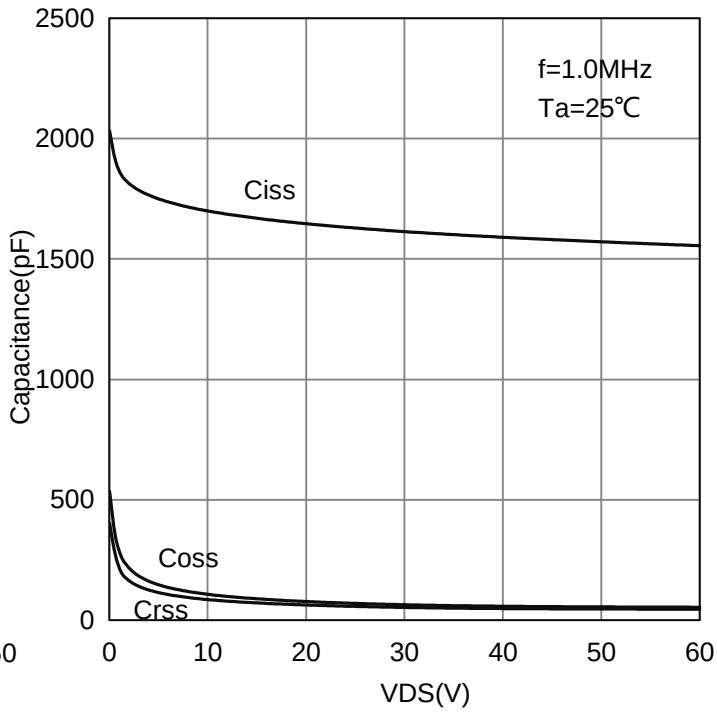
RDS(on) vs. VGS



RDS(on) vs. Tj

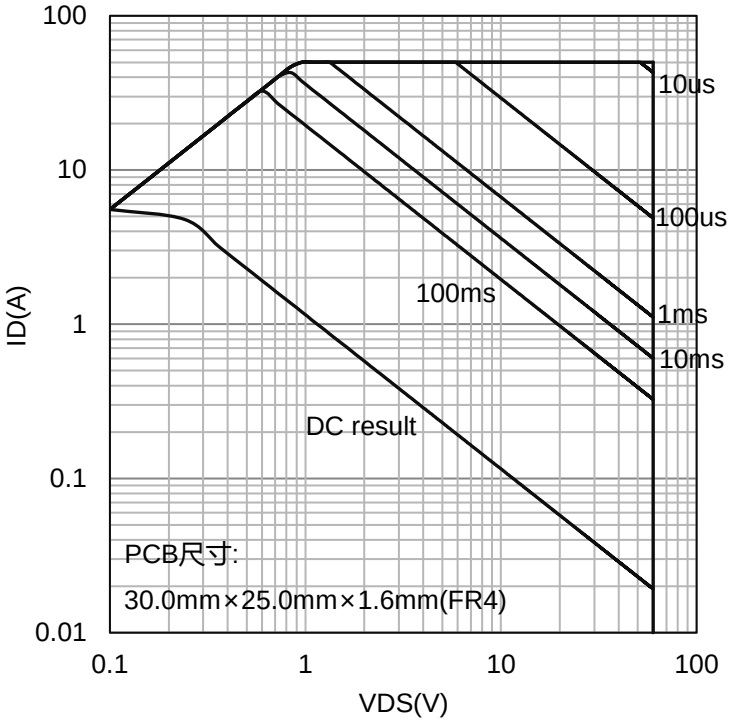


VGSth vs. Tj



Capacitance

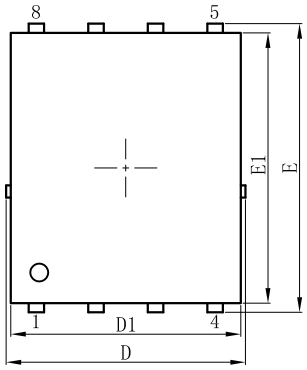
7.ELECTRICAL CHARACTERISTICS CURVES(Con.)



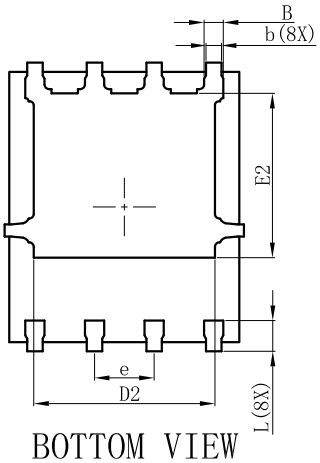
Safe Opearting Area

8.OUTLINE AND DIMENSIONS

DFN5060-8B

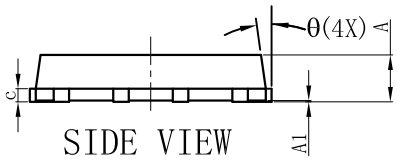


TOP VIEW



BOTTOM VIEW

DFN5060-8B			
DIM	MIN	NOR	MAX
A	0.90	1.00	1.10
A1	0.00	0.02	0.05
E	6.00	6.15	6.30
E1	5.66	5.76	5.86
E2	3.40	3.50	3.60
D	4.95	5.10	5.25
D1	4.80	4.90	5.00
D2	3.76	3.86	3.96
b	0.30	0.35	0.40
B	0.36	0.41	0.46
L	0.56	0.66	0.76
e	1.27BSC		
c	0.254REF.		
θ	0°	-	12°
All Dimensions in mm			

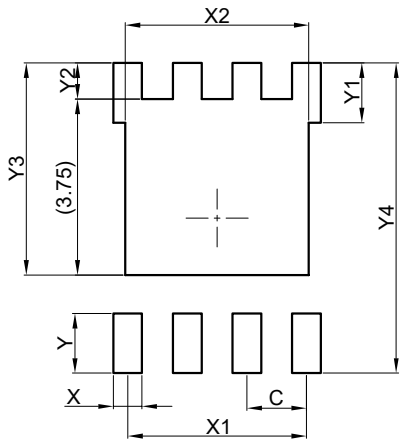


SIDE VIEW

GENERAL NOTES

1. Top package surface finish Ra0.4±0.2um
2. Bottom package surface finish Ra0.7±0.2um
3. Side package surface finish Ra0.4±0.2um
4. Protrusion or Gate Burrs shall not exceed 0.05mm per side.
5. Offcenter Max0.038mm; Mismatch Max 0.038mm.

9.SOLDERING FOOTPRINT



DFN5060-8B	
DIM	(mm)
C	1.27
X	0.61
X1	3.81
X2	3.91
Y	1.27
Y1	1.27
Y2	0.77
Y3	4.52
Y4	6.61

DISCLAIMER

- Curve guarantee in the specification. The curve of test items with electric parameter is used as quality guarantee. The curve of test items without electric parameter is used as reference only.

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