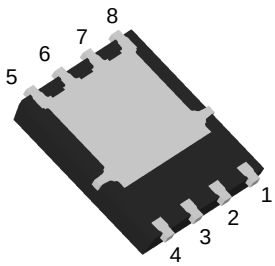
S-LN74025DT3WG

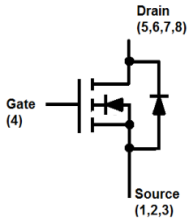
40V N-Channel Power MOSFET



DFN5060-8B

1. FEATURES

- Low thermal impedance.
- Fast switching.
- We declare that the material of product compliance with RoHS requirements and Halogen Free.
- S-prefix for automotive and other applications requiring unique site and control change requirements; AEC-Q101 qualified and PPAP capable.



2. APPLICATIONS

- Power Tools
- DC/DC conversion
- Motor Control

3. DEVICE MARKING AND RESISTOR VALUES

Device	Marking	Shipping
S-LN74025DT3WG	LN74025	5000/Tape&Reel

4. MAXIMUM RATINGS(Ta = 25ºC)

Parameter		Symbol	Limits	Unit
Drain-to-Source Voltage		VDS	40	V
Gate-to-Source Voltage		VGS	±20	V
Continuous Drain Current(Note 1)	TA=25℃	ID	34	A
	TA=70℃		27.4	
	TA=100℃		21.4	
Pulsed Drain Current (Note 2)	TA=25℃	IDM	136	
Continuous Drain Current	TC=25℃	ID	161.4	A
	TC=70℃		129.1	
	TC=100℃		102.1	
Pulsed Drain Current	TC=25℃	IDM	645	
Avalanche Current		IAS	42.6	A
Avalanche Energy(L=0.1mH)		EAS	90.7	mJ
Power Dissipation(Note 1)	TA=25℃	PD	2.8	W
	TC=25℃		62.5	
Operating Junction and Storage Temperature Range		Tj/Tstg	-55~+150	℃

5. THERMAL CHARACTERISTICS

Parameter	Symbol	Max	Unit
Thermal Resistance,Junction-to-Ambient(Note 1)	RθJA	45	℃/W
Thermal Resistance,Junction-to-Case	RθJC	2	

1.Surface mounted on 1.5 x 1.5 FR4 board using 1 sq in pad, 2 oz Cu.

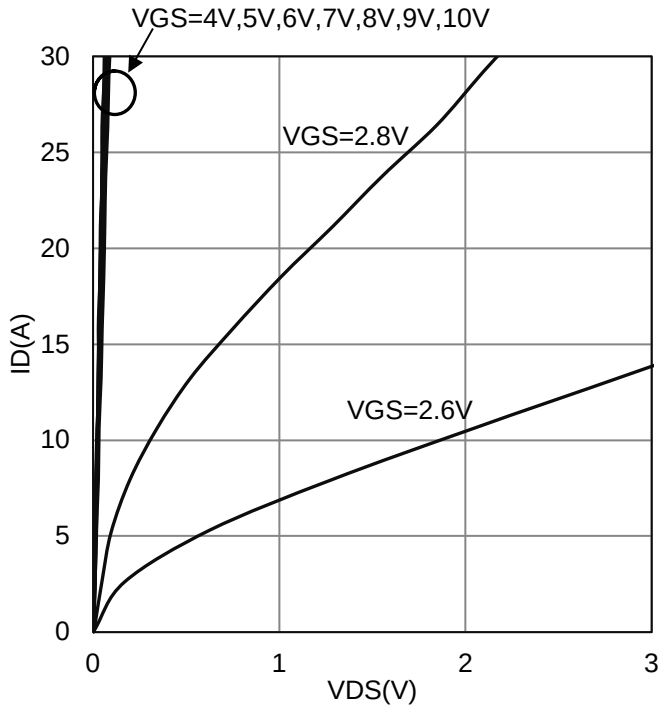
2.Pulse width limited by maximum junction temperature

6. ELECTRICAL CHARACTERISTICS (Ta= 25°C)

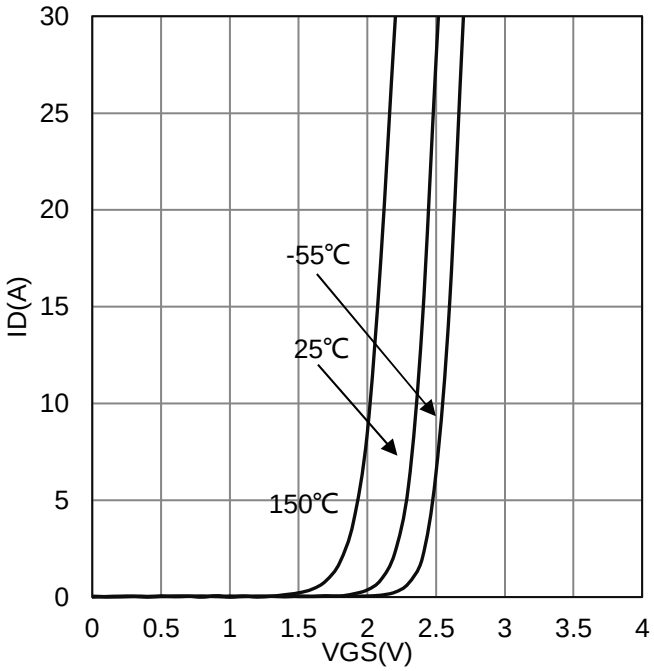
Characteristic		Symbol	Min.	Typ.	Max.	Unit
STATIC						
Drain–Source Breakdown Voltage (VGS = 0 V, ID = 250 μA)		VBRDSS	40	-	-	V
Gate Threshold Voltage (VDS = VGS , ID = 250 μA)		VGS(th)	1.2	1.8	2.5	V
Gate-Body leakage current (VDS = 0 V, VGS = ±20 V)		IGSS	-	-	±100	nA
Zero Gate Voltage Drain Current (VDS = 32 V, VGS = 0 V)		IDSS	-	-	1	μA
Drain-to-Source On-Resistance (Note 3) (VGS = 10 V, ID = 20 A) (VGS = 4.5 V, ID = 15 A)		RDS(on)	- -	2.1 2.6	2.5 3	mΩ
Diode Forward Voltage (IS = 20 A, VGS = 0 V)		VSD	-	0.9	1.2	V
DYNAMIC						
Total Gate Charge	(VDS = 20 V, VGS = 10 V,ID =20 A)	Qg	-	46	69	nC
Gate to Source Charge		Qgs	-	8.5	-	
Gate to Drain Charge		Qgd	-	7.6	-	
Turn-on Delay Time	(VDD = 20 V,ID = 20 A,VGS = 10 V,RG = 6 Ω)	td(on)	-	17	-	nS
Rise Time		tr	-	12	-	
Turn-Off Delay Time		td(off)	-	76	-	
Fall Time		tf	-	19	-	
Input Capacitance	(VDS = 20 V, VGS = 0 V, f = 1MHz)	Ciss	-	2825	-	pF
Output Capacitance		Coss	-	605	-	
Reverse Transfer Capacitance		Crss	-	22	-	

3.Pulse test: PW ⩽ 300μs duty cycle ⩽ 2%.

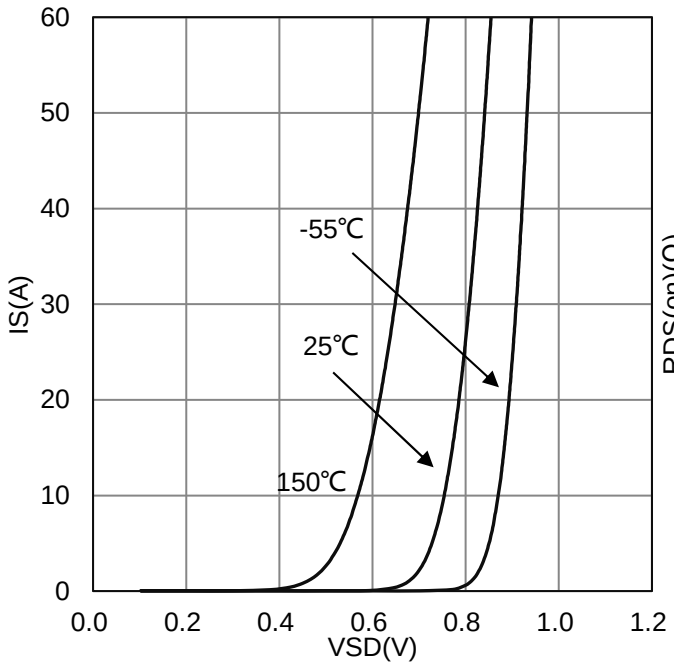
7. ELECTRICAL CHARACTERISTICS CURVES



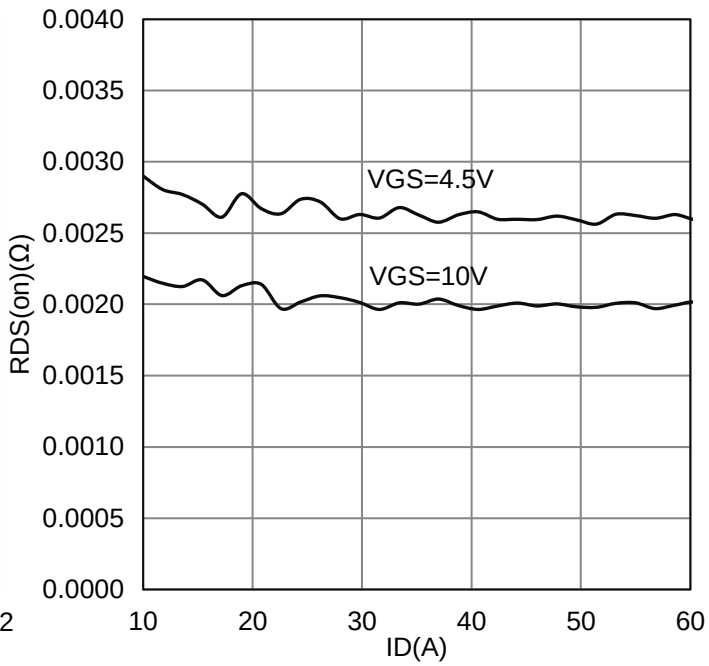
ID vs. VDS



ID vs. VGS

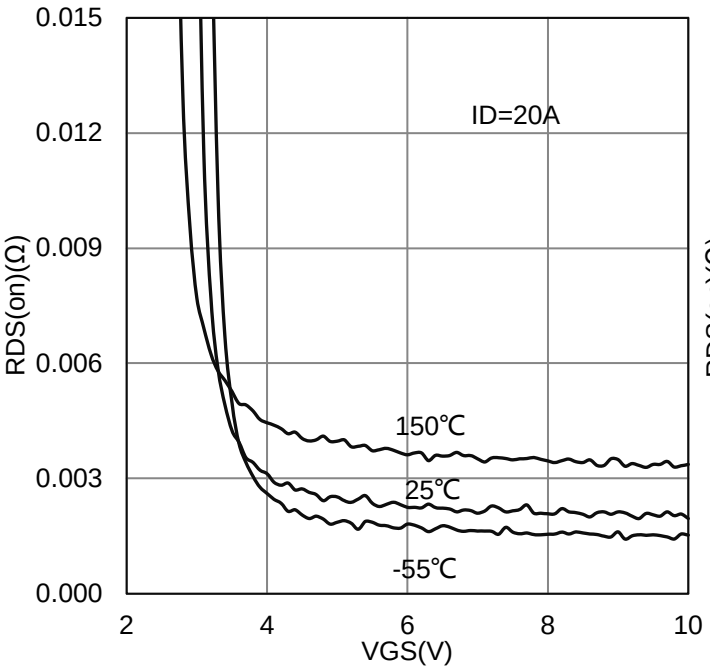


IS vs. VSD

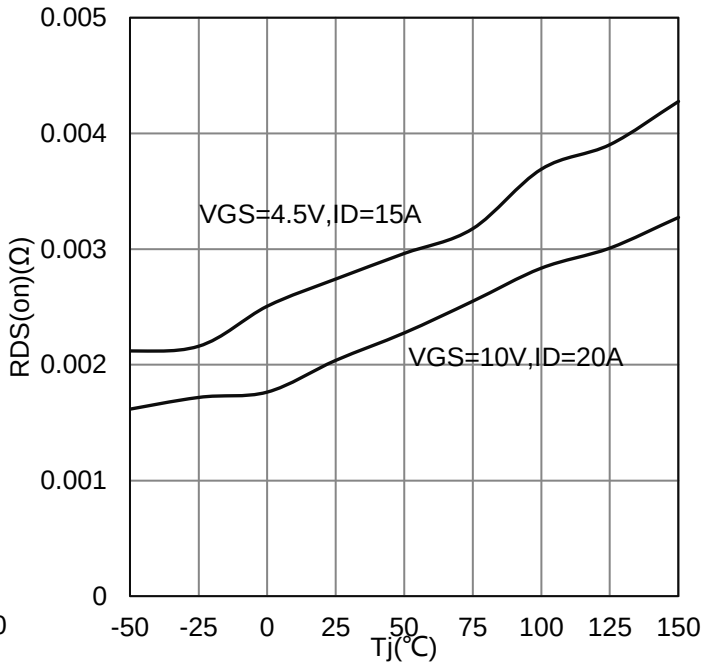


RDS(on) vs. ID

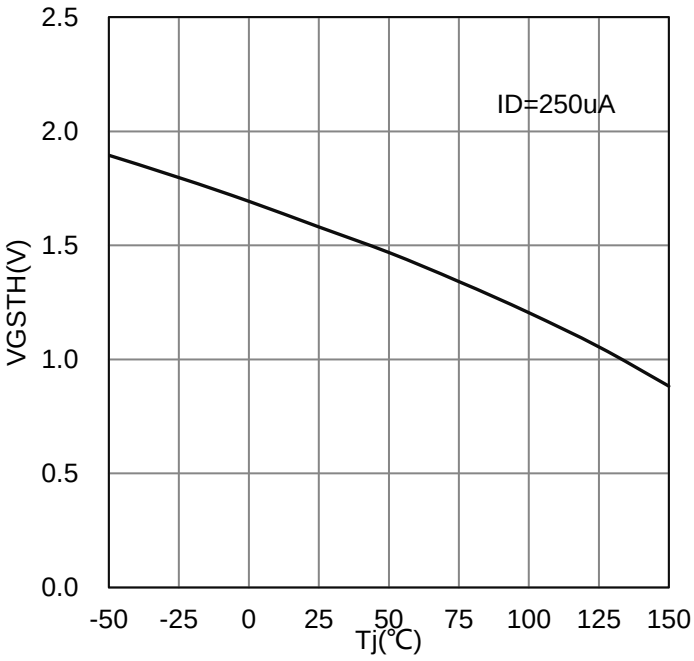
7. ELECTRICAL CHARACTERISTICS CURVES(Con.)



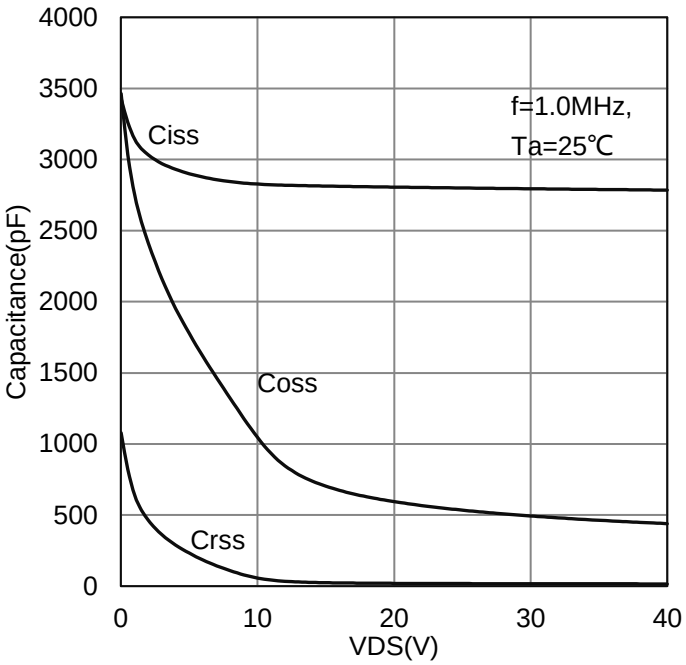
RDS(on) vs. VGS



RDS(on) vs. Tj

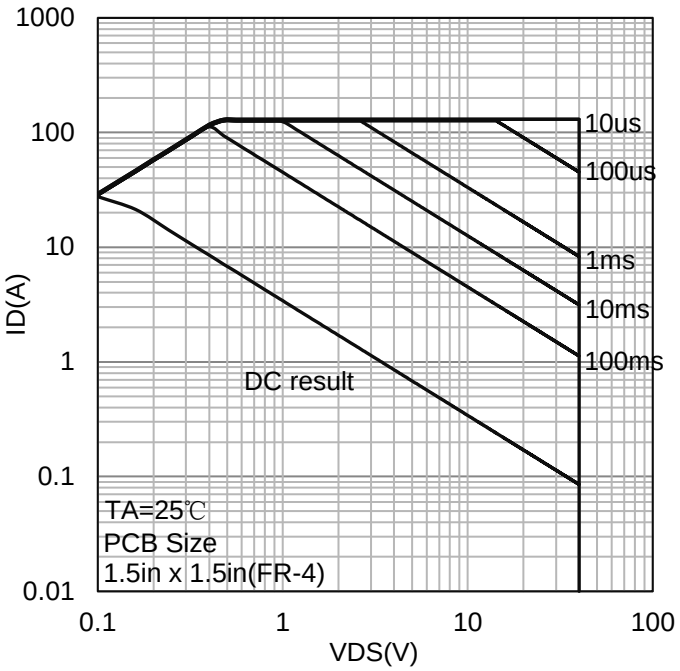


VGSth vs. Tj

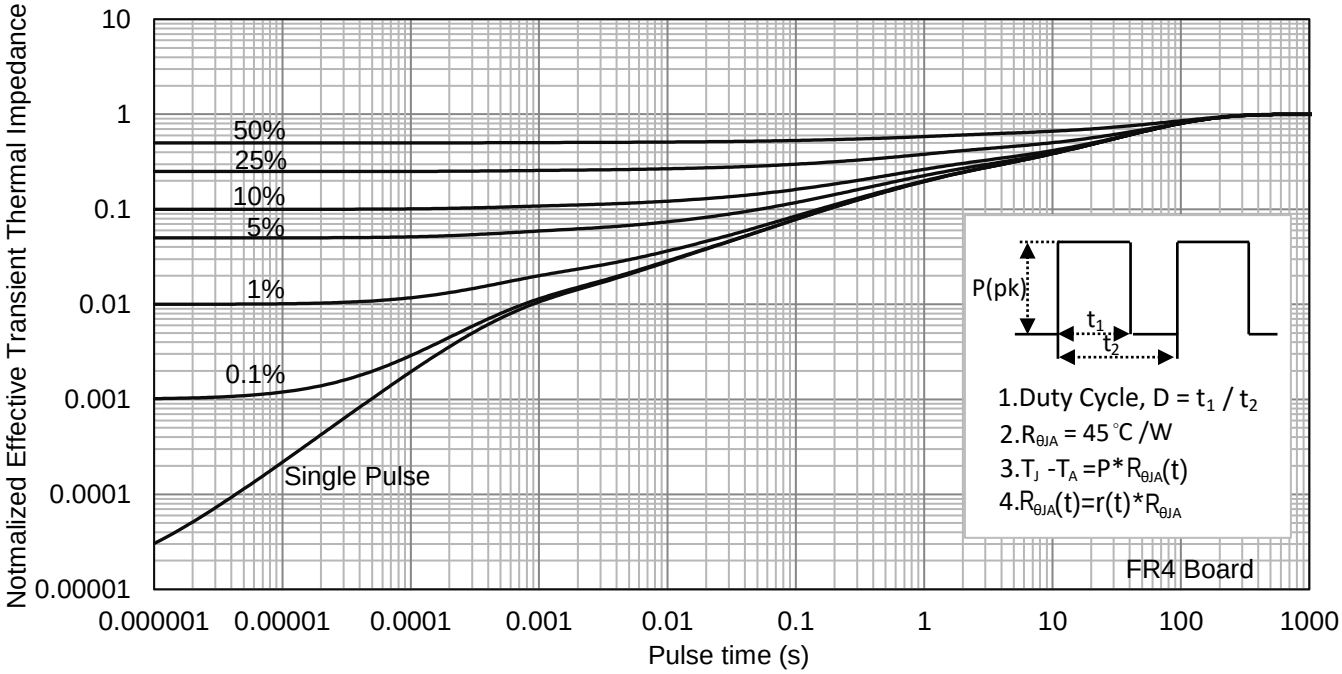


Capacitance

7. ELECTRICAL CHARACTERISTICS CURVES(Con.)

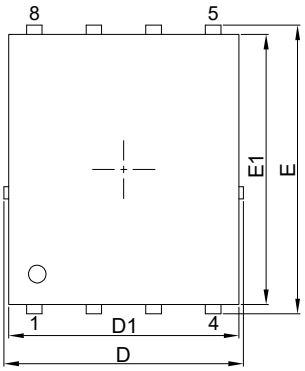


Safe Operating Area

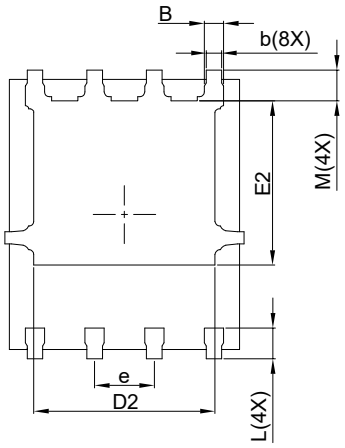


Thermal Response

8.OUTLINE AND DIMENSIONS

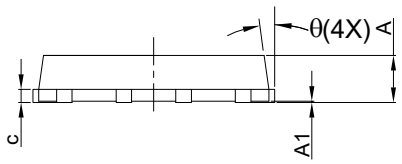


TOP VIEW



BOTTOM VIEW

DFN5060-8B			
DIM	MIN	NOR	MAX
A	0.90	1.00	1.10
A1	0.00	0.02	0.05
E	6.00	6.15	6.30
E1	5.66	5.76	5.86
E2	3.40	3.50	3.60
D	4.95	5.10	5.25
D1	4.80	4.90	5.00
D2	3.76	3.86	3.96
b	0.30	0.35	0.40
B	0.36	0.41	0.46
L	0.56	0.66	0.76
M	0.56	0.66	0.76
e	1.27BSC		
c	0.254REF.		
θ	0 °	-	12°

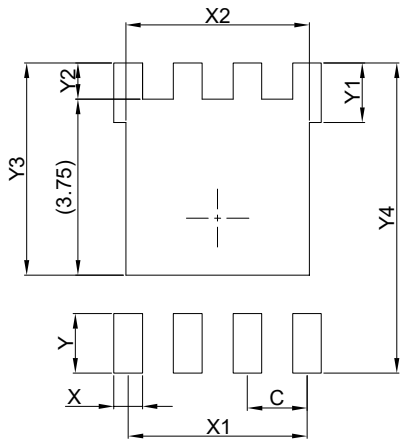


SIDE VIEW

GENERAL NOTES

1. Top package surface finish Ra Max0.4um
2. Bottom package surface finish Ra Max0.4um
3. Side package surface finish Ra Max0.4um
4. Protrusion or Gate Burrs shall not exceed 0.05mm per side
5. Offcenter Max0.038mm; Mismatch Max 0.038mm.

9.SOLDERING FOOTPRINT



DFN5060-8B	
DIM	(mm)
C	1.27
X	0.61
X1	3.81
X2	3.91
Y	1.27
Y1	1.27
Y2	0.77
Y3	4.52
Y4	6.61

DISCLAIMER

- Curve guarantee in the specification. The curve of test items with electric parameter is used as quality guarantee. The curve of test items without electric parameter is used as reference only.

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