

LP2301ELT1G

S-LP2301ELT1G

20V P-Channel Enhancement-Mode MOSFET

1. FEATURES

- $V_{DS} = -20V$
- $R_{DS(ON)}, V_{GS@-2.5V}, I_{DS@-2.0A} \leq 156m\Omega$
- $R_{DS(ON)}, V_{GS@-4.5V}, I_{DS@-2.8A} \leq 110m\Omega$
- We declare that the material of product compliance with RoHS requirements and Halogen Free.
- S- prefix for automotive and other applications requiring unique site and control change requirements; AEC-Q101 qualified and PPAP capable.
- Advanced trench process technology
- High density cell design for ultra low on-resistance
- Fully characterized avalanche voltage and current improved shoot-through FOM
- ESD protected, ESD > 1kV HBM

2. APPLICATIONS

- Simple drive requirement
- Small package outline
- Surface mount device

3. DEVICE MARKING AND ORDERING INFORMATION

Device	Marking	Shipping
LP2301ELT1G	YES	3000/Tape&Reel
LP2301ELT3G	YES	10000/Tape&Reel

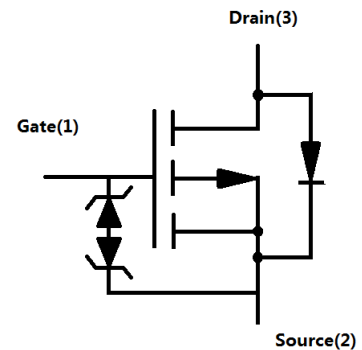
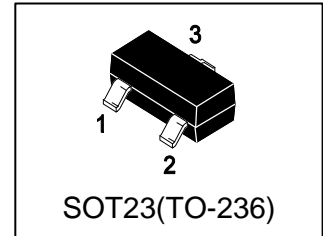
4. MAXIMUM RATINGS($T_a = 25^\circ C$)

Parameter	Symbol	Limits	Unit
Drain-Source Voltage	V_{DSS}	-20	V
Gate-to-Source Voltage – Continuous	V_{GS}	± 8	V
Drain Current			A
– Continuous $T_A = 25^\circ C$	I_D	-2.8	
– Pulsed(Note 1)	I_{DM}	-11	

5. THERMAL CHARACTERISTICS

Parameter	Symbol	Limits	Unit
Maximum Power Dissipation	PD	0.9	W
Thermal Resistance, Junction-to-Ambient(Note 2)	$R_{\theta JA}$	140	$^\circ C/W$
Junction and Storage temperature	T_J, T_{stg}	$-55 \sim +150$	$^\circ C$

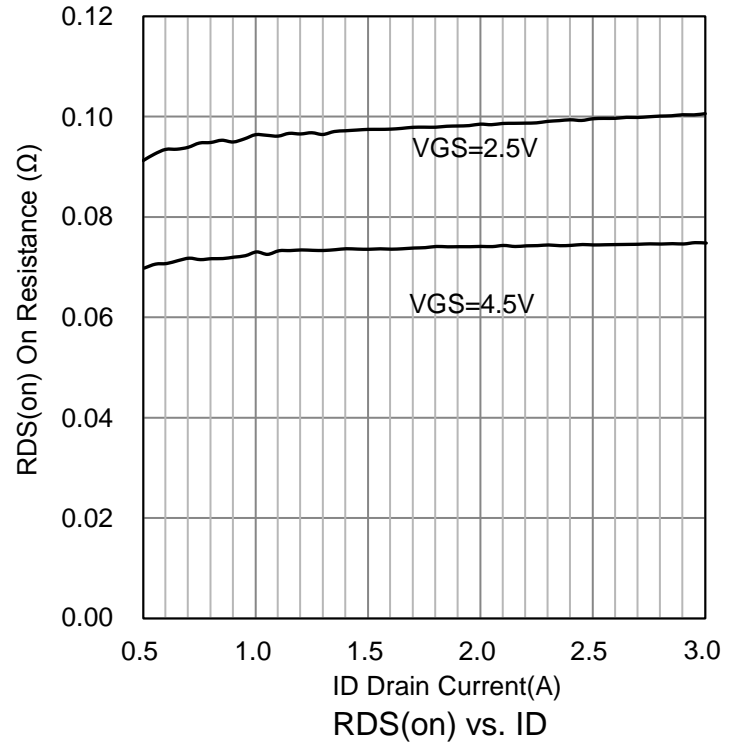
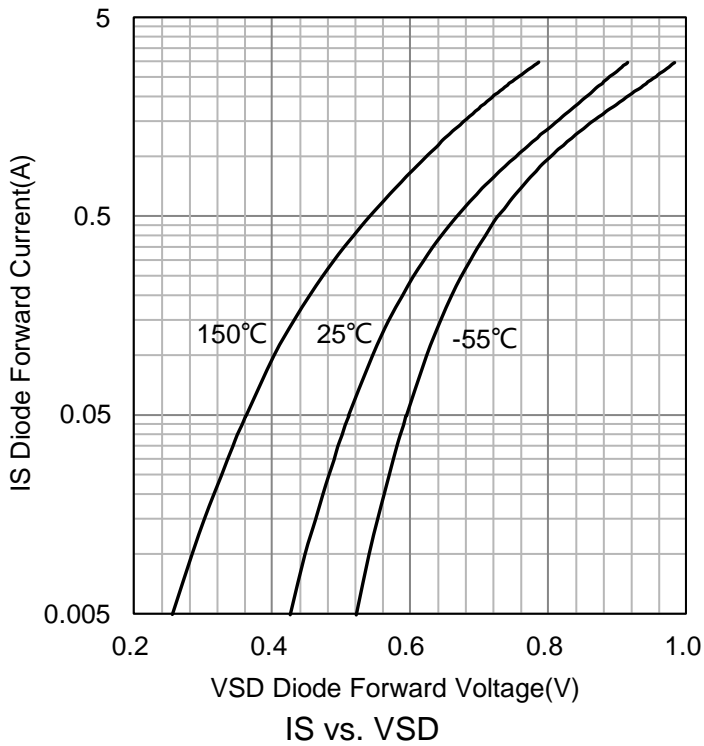
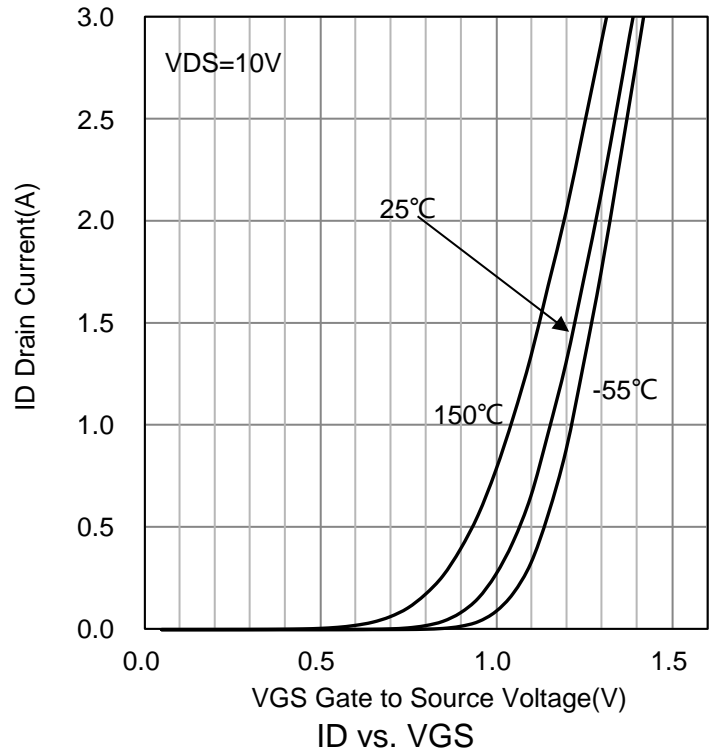
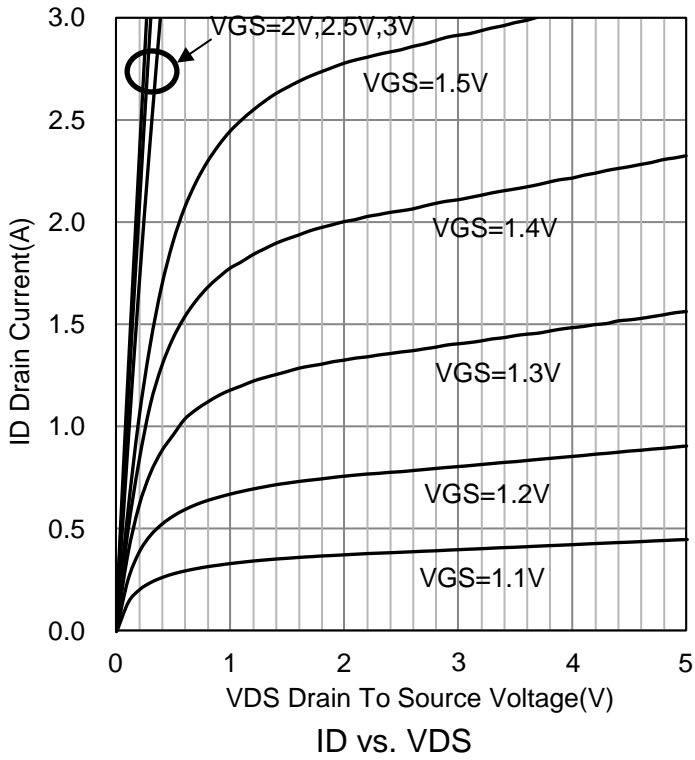
1. Repetitive Rating: Pulse width limited by the Maximum junction temperature.
2. 1-in² 2oz Cu PCB board.



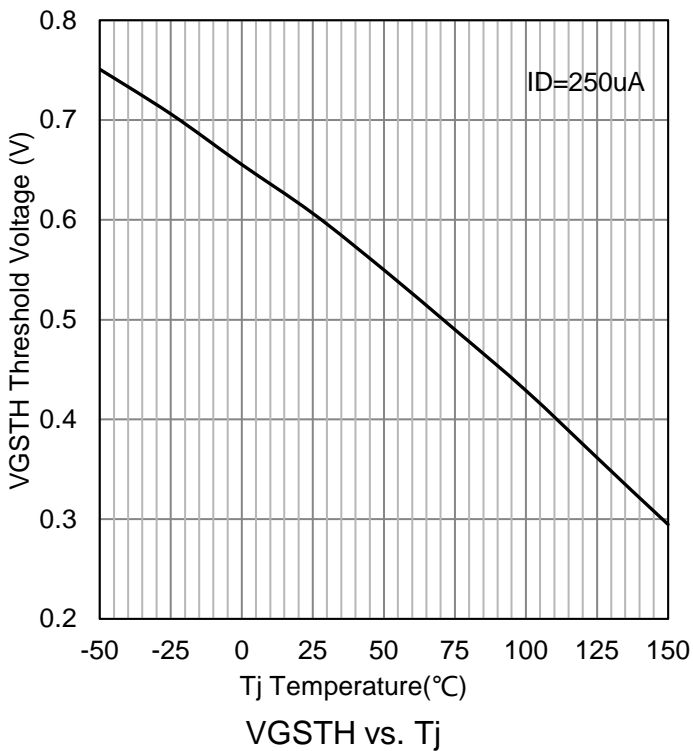
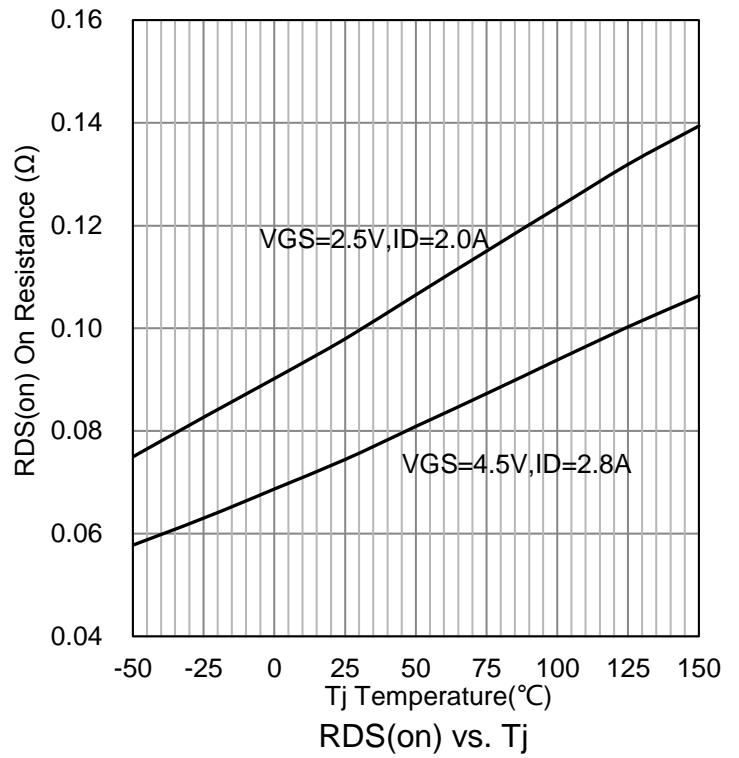
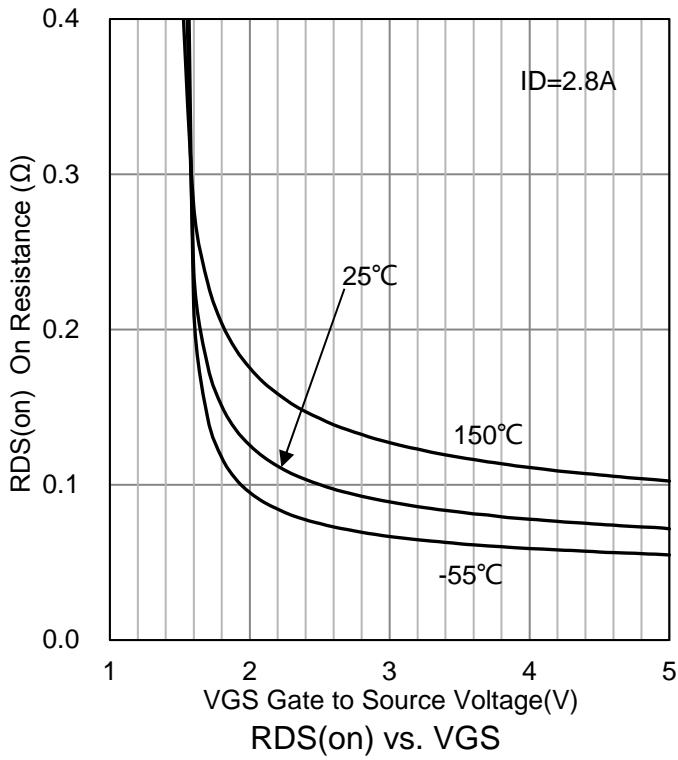
6. ELECTRICAL CHARACTERISTICS (Ta= 25°C)

Characteristic	Symbol	Min.	Typ.	Max.	Unit	
STATIC						
Drain–Source Breakdown Voltage (VGS = 0, ID = -250μA)	VBRDSS	-20	-	-	V	
Zero Gate Voltage Drain Current (VGS = 0, VDS = -9.6 V)	IDSS	-	-	-1	μA	
Gate–Body Leakage Current, Forward (VGS = ± 8 V)	IGSS	-	-	± 10	μA	
Gate Threshold Voltage (VDS = VGS, ID = -250μA)	VGS(th)	-0.4	-0.65	-0.9	V	
Static Drain–Source On–State Resistance (VGS = -4.5 V, ID = -2.8 A) (VGS = -2.5 V, ID = -2 A)	RDS(on)	-	90 110	110 156	mΩ	
DYNAMIC						
Total Gate Charge	(VDS = -10V, VGS = -10V, ID = -1.6A)	Qg(-10V)	-	7.8	-	nC
Total Gate Charge		Qg(-4.5V)	-	3.5	-	
Gate–Source Charge		Qgs	-	0.5	-	
Gate–Drain Charge		Qgd	-	1.2	-	
Input Capacitance (VGS = 0 V, f = 1.0MHz, VDS= -6 V)	Ciss	-	520	-	pF	
Output Capacitance (VGS = 0 V, f = 1.0MHz, VDS= -6 V)	Coss	-	55	-	pF	
Reverse Transfer Capacitance (VGS = 0 V, f = 1.0MHz, VDS= -6 V)	Crss	-	17	-	pF	
Turn-On Delay Time	(VDD = -6V, RL = 6Ω ID = -1A, VGEN = -4.5V RG = 6Ω)	td(on)	-	1350	-	ns
Rise Time		tr	-	830	-	
Turn-Off Delay Time		td(off)	-	5500	-	
Fall Time		tf	-	1550	-	
Forward Voltage (VGS = 0 V, ISD = -0.75 A)	VSD	-	-0.8	-1.2	V	

7. ELECTRICAL CHARACTERISTICS CURVES



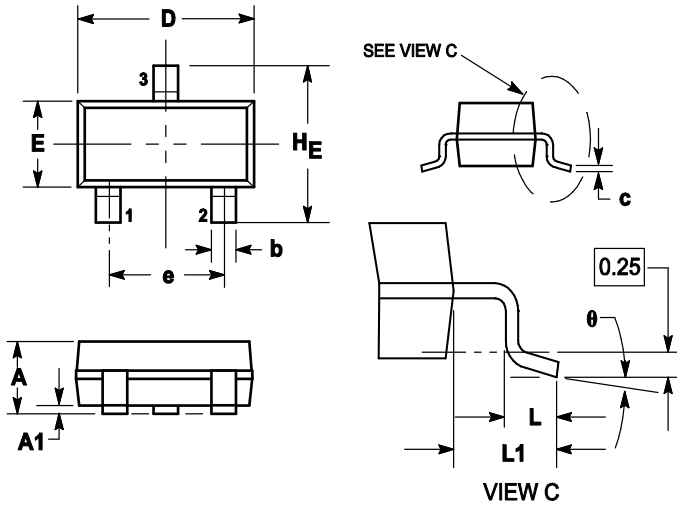
7. ELECTRICAL CHARACTERISTICS CURVES(Con.)



8. OUTLINE AND DIMENSIONS

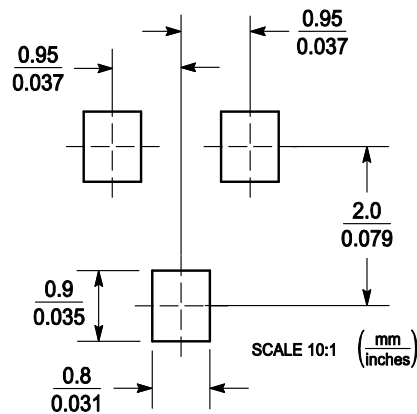
Notes:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.



DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.89	1	1.11	0.035	0.04	0.044
A1	0.01	0.06	0.1	0.001	0.002	0.004
b	0.37	0.44	0.5	0.015	0.018	0.02
c	0.09	0.13	0.18	0.003	0.005	0.007
D	2.80	2.9	3.04	0.11	0.114	0.12
E	1.20	1.3	1.4	0.047	0.051	0.055
e	1.78	1.9	2.04	0.07	0.075	0.081
L	0.10	0.2	0.3	0.004	0.008	0.012
L1	0.35	0.54	0.69	0.014	0.021	0.029
HE	2.10	2.4	2.64	0.083	0.094	0.104
theta	0°	---	10°	0°	---	10°

9. SOLDERING FOOTPRINT



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