

# LN2336ELT1G

N-Channel 30V (D-S) MOSFET , ESD Protected

## 1. FEATURES

- Gate to Source ESD Protected.
- Super high density cell design for extremely low RDS(ON).
- Exceptional on-resistance and maximum DC current capability.
- We declare that the material of product compliance with RoHS requirements and Halogen Free.

## 2. APPLICATIONS

- Power Management in Note book
- Portable Equipment
- Load Switch

## 3. DEVICE MARKING AND ORDERING INFORMATION

Device	Marking	Shipping
LN2336ELT1G	3ED	3000/Tape&Reel

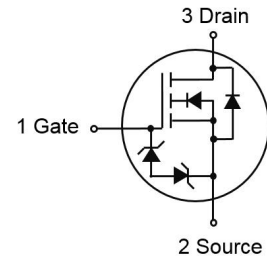
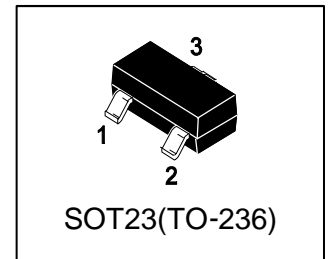
## 4. MAXIMUM RATINGS(Ta = 25°C)

Parameter	Symbol	Limits	Unit
Drain–Source Voltage	VDS	30	V
Gate–to–Source Voltage	VGSS	±20	V
Continuous Drain	ID	TA =25°C	4
		TA =70°C	3.2
Pulsed Drain Current	IDM	16	A
Avalanche Current(L=0.1mH)	IAS	9	A
Avalanche energy(L=0.1mH)	EAS	4.05	mJ

## 5. THERMAL CHARACTERISTICS

Parameter	Symbol	Limits	Unit
Maximum Power Dissipation	PD	0.9	W
Thermal Resistance, Junction–to–Ambient(Note 1)	RθJA	140	°C/W
Junction and Storage temperature	TJ,Tstg	-55~+150	°C

1. 1-in<sup>2</sup> 2oz Cu PCB board.

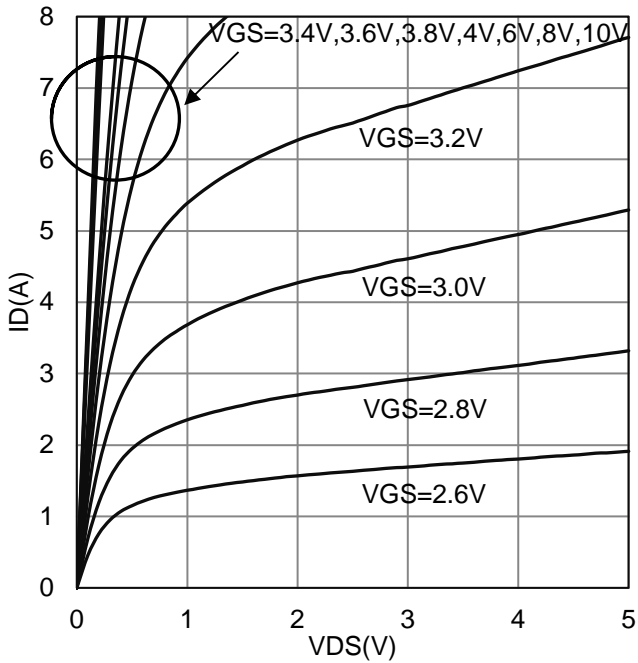


**6 ELECTRICAL CHARACTERISTICS (Ta= 25 °C)**

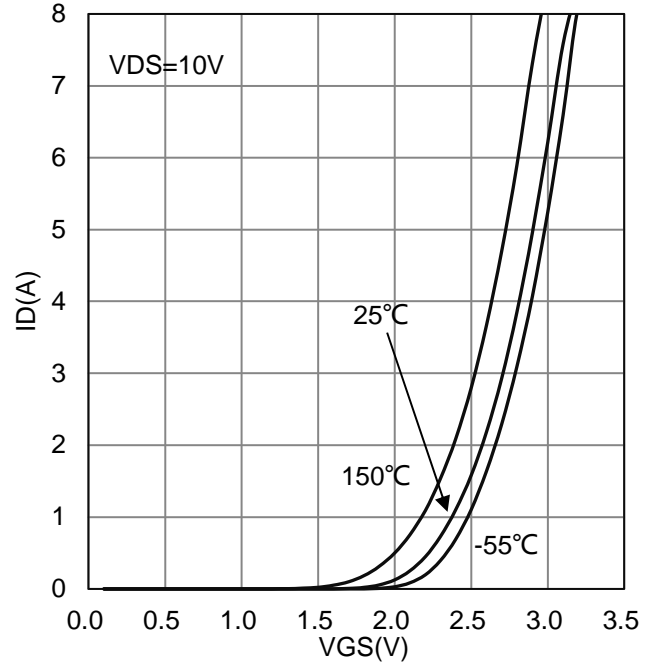
Characteristic	Symbol	Min.	Typ.	Max.	Unit
Static					
Drain-Source Breakdown Voltage (VGS =0V, ID =250μA)	V(BR)DSS	30	-	-	V
Gate Threshold Voltage (VDS =VGS , ID =250μA)	VGS(th)	1	1.5	3	V
Gate Leakage Current (VDS =0V, VGS =±16V)	IGSS	-	-	±10	μA
Zero Gate Voltage Drain Current (VDS =30V, VGS =0V)	IDSS	-	-	1	
Drain-Source On-Resistance(Note 2) (VGS =10V, ID = 3A) (VGS =4.5V, ID = 3A)	RDS(ON)	- -	35 48	40 60	mΩ
Diode Forward Voltage (IS =1.7A, VGS =0V)	VSD	-	0.8	1.2	V
Dynamic					
Input Capacitance	(VDS =15V, VGS =0V, f=1MHz)	Ciss	-	360	pF
Output Capacitance		Coss	-	52	
Reverse Transfer Capacitance		Crss	-	37	
Total Gate Charge(0~10V)	(VDS =15V , ID =3A)	Qg	-	6.1	nC
Total Gate Charge(0~4.5V)		Qg	-	3.2	
Gate-Source Charge		Qgs	-	1.1	
Gate-Drain Charge		Qgd	-	1.3	
Turn-On Delay Time	(VDD =15V, RL =15Ω, ID =1A, VGEN =10V, RG =6Ω)	td(on)	-	TBD	ns
Turn-On Rise Time		tr	-	TBD	
Turn-Off Delay Time		td(off)	-	TBD	
Turn-Off Fall Time		tf	-	TBD	

2. Pulse test: pulse width ≤ 300μs, duty cycle ≤ 2%.

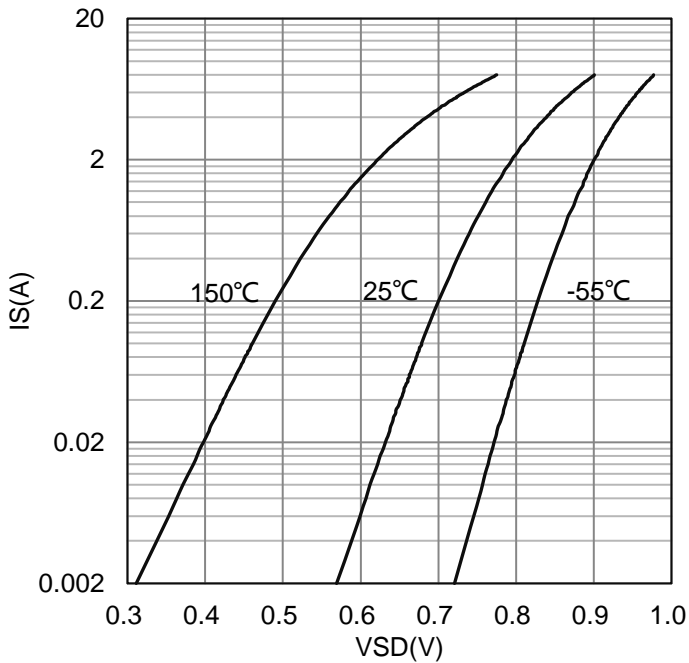
**7. ELECTRICAL CHARACTERISTICS CURVES**



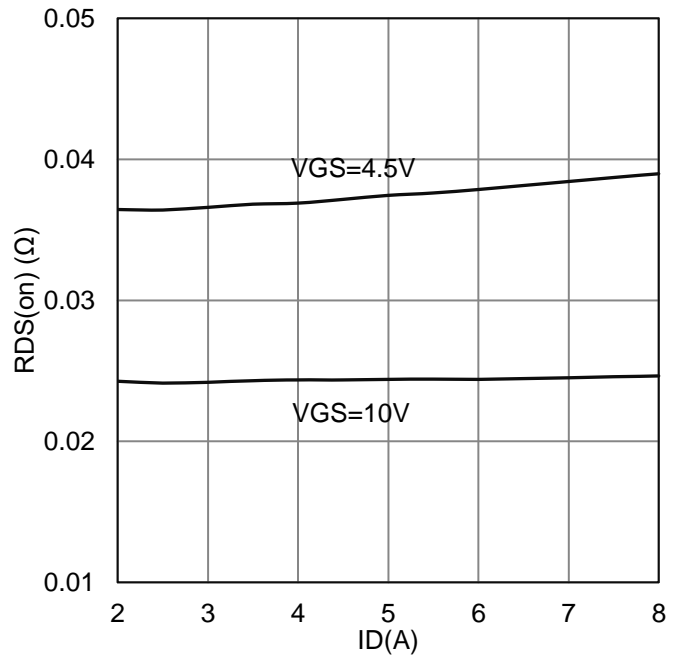
ID vs. VDS



ID vs. VGS

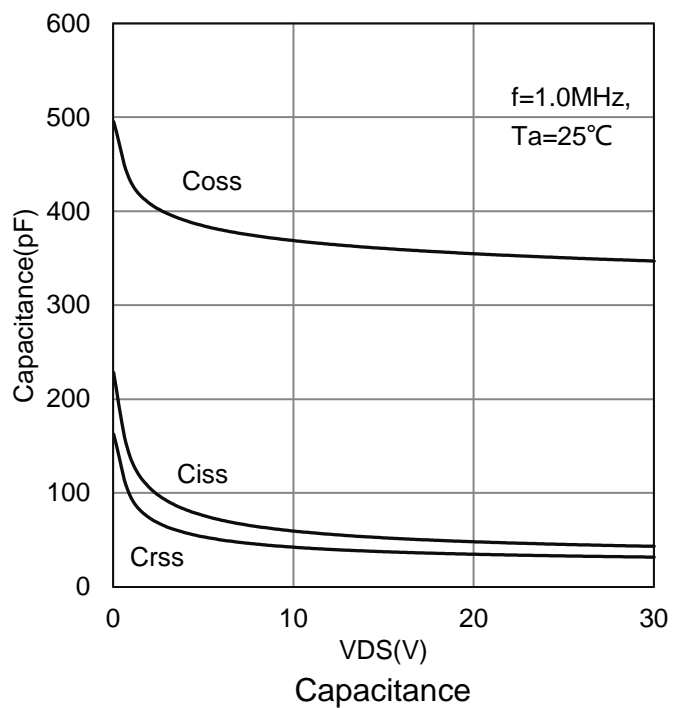
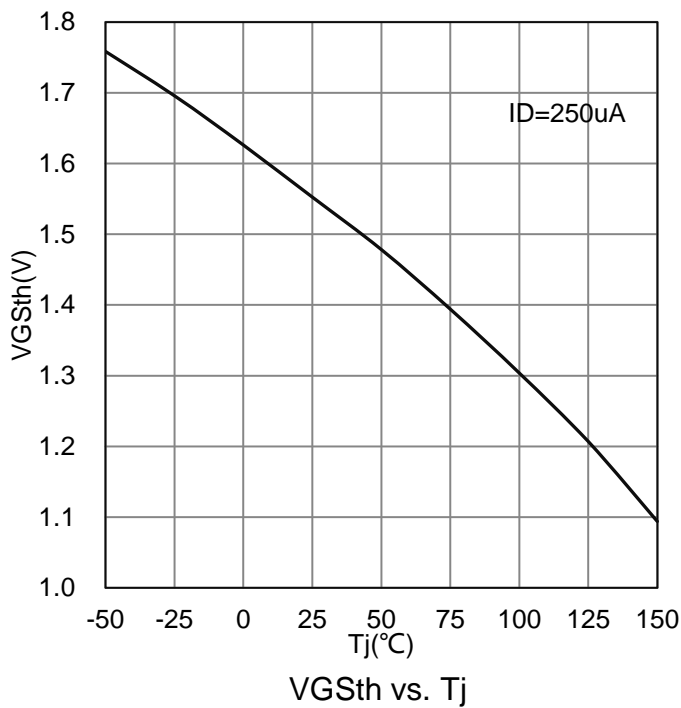
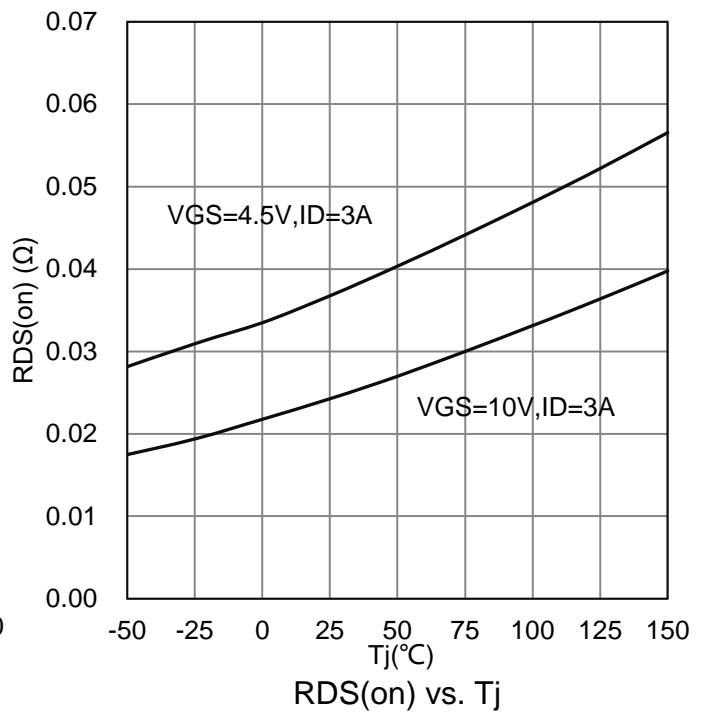
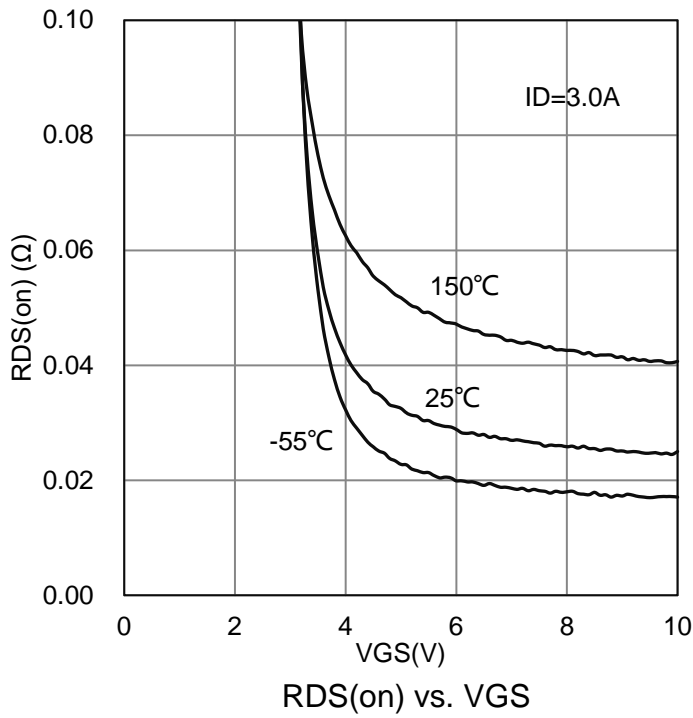


IS vs. VSD



RDS(on) vs. ID

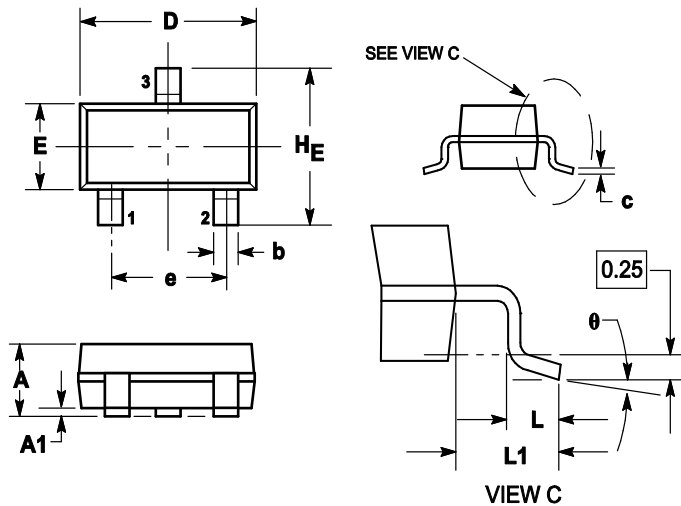
### 7. ELECTRICAL CHARACTERISTICS CURVES(Con.)



### 8. OUTLINE AND DIMENSIONS

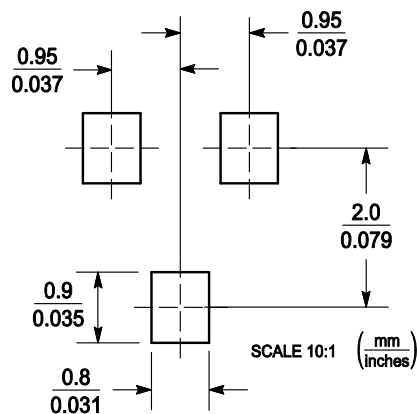
Notes:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.



DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.89	1	1.11	0.035	0.04	0.044
A1	0.01	0.06	0.1	0.001	0.002	0.004
b	0.37	0.44	0.5	0.015	0.018	0.02
c	0.09	0.13	0.18	0.003	0.005	0.007
D	2.80	2.9	3.04	0.11	0.114	0.12
E	1.20	1.3	1.4	0.047	0.051	0.055
e	1.78	1.9	2.04	0.07	0.075	0.081
L	0.10	0.2	0.3	0.004	0.008	0.012
L1	0.35	0.54	0.69	0.014	0.021	0.029
HE	2.10	2.4	2.64	0.083	0.094	0.104
theta	0°	---	10°	0°	---	10°

### 9. SOLDERING FOOTPRINT



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