

LP2301SLT1G

20V P-Channel Enhancement-Mode MOSFET

1. FEATURES

- $V_{DS} = -20V$
- $R_{DS(ON)}, V_{GS@-2.5V}, I_{D@-1.8A} \leq 130m\Omega$
- $R_{DS(ON)}, V_{GS@-4.5V}, I_{D@-2A} \leq 100m\Omega$
- We declare that the material of product compliance with RoHS requirements and Halogen Free.
- Advanced trench process technology
- High density cell design for ultra low on-resistance

2. APPLICATIONS

- Simple drive requirement
- Small package outline
- Surface mount device

3. DEVICE MARKING AND ORDERING INFORMATION

Device	Marking	Shipping
LP2301SLT1G	01S	3000/Tape&Reel

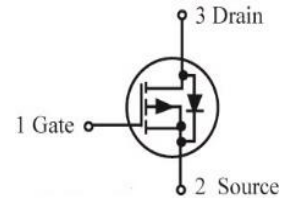
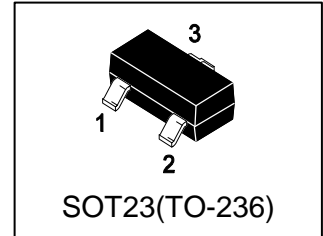
4. MAXIMUM RATINGS($T_a = 25^\circ C$)

Parameter	Symbol	Limits	Unit
Drain–Source Voltage	V_{DSS}	-20	V
Gate–to–Source Voltage – Continuous	V_{GS}	± 12	V
Drain Current			
– Continuous $T_a = 25^\circ C$	I_D	-2.4	A
– Pulsed(Note 1)	I_{DM}	-10	
– Continuous $T_a = 25^\circ C$	I_D	-1.8	A
– Pulsed(Note 3)	I_{DM}	-7	

5. THERMAL CHARACTERISTICS

Parameter	Symbol	Limits	Unit
Maximum Power Dissipation	PD	0.9	W
Maximum Power Dissipation(Note 3)	PD	0.5	W
Thermal Resistance, Junction–to–Ambient(Note 2)	$R_{\theta JA}$	140	$^\circ C/W$
Junction–to–Ambient(Note 3)	$R_{\theta JA}$	250	
Junction and Storage temperature	T_J, T_{stg}	$-55 \sim +150$	$^\circ C$

- 1.Repetitive Rating: Pulse width limited by the Maximum junction temperature.
- 2.1-in² 2oz Cu PCB board.
- 3.Surface mounted on FR4 board using the minimum recommended pad size.

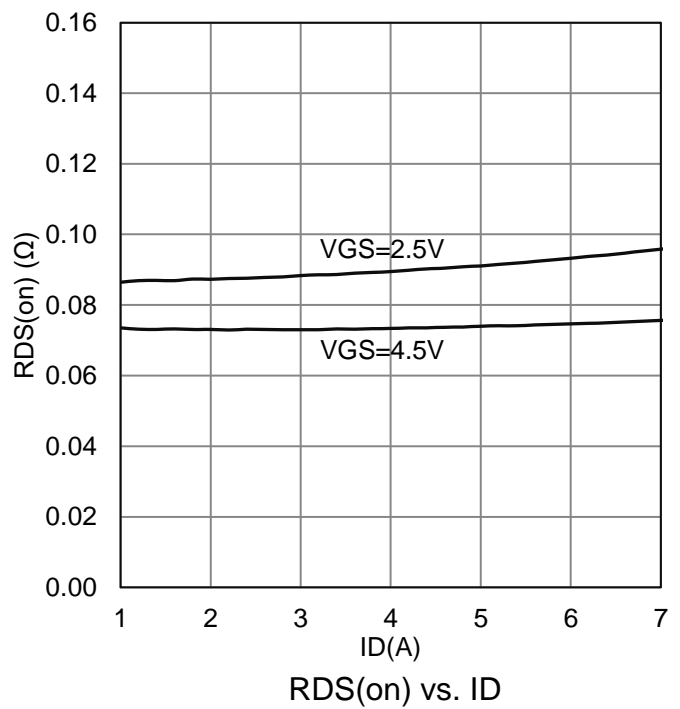
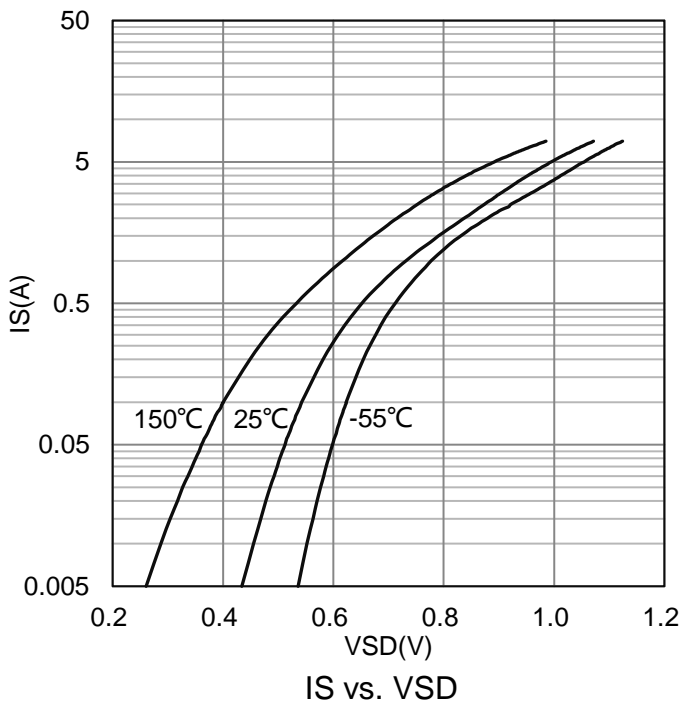
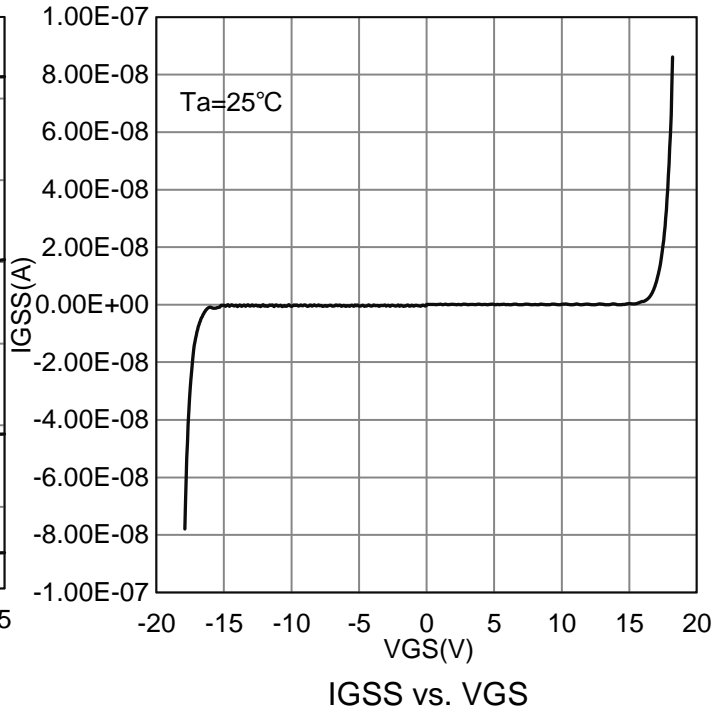
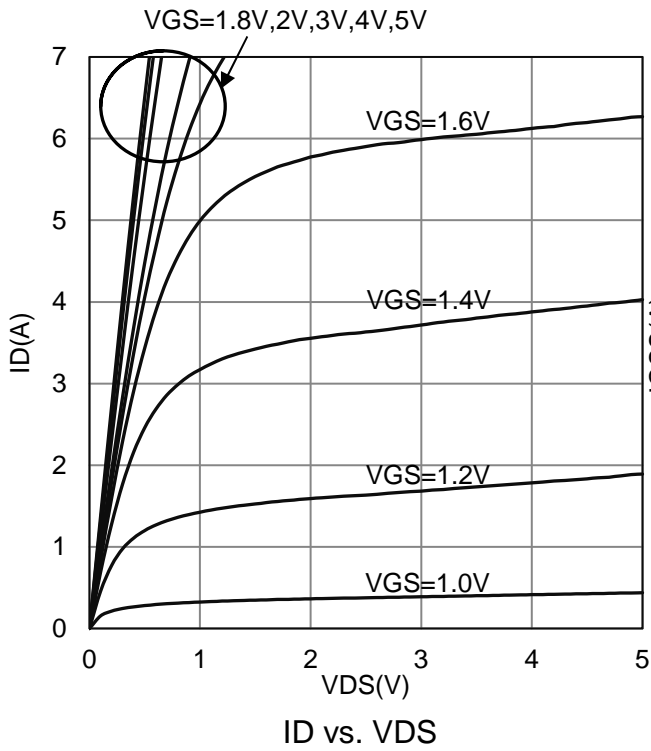


6. ELECTRICAL CHARACTERISTICS (Ta= 25°C)

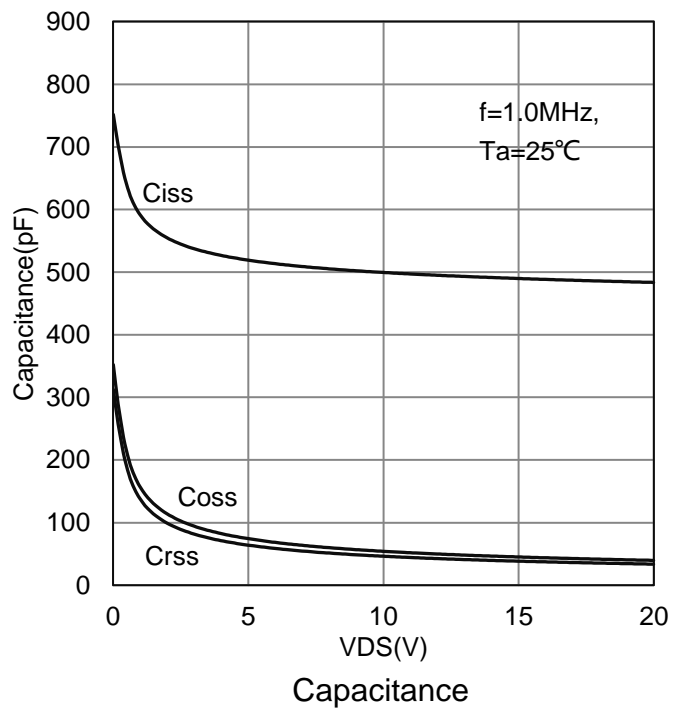
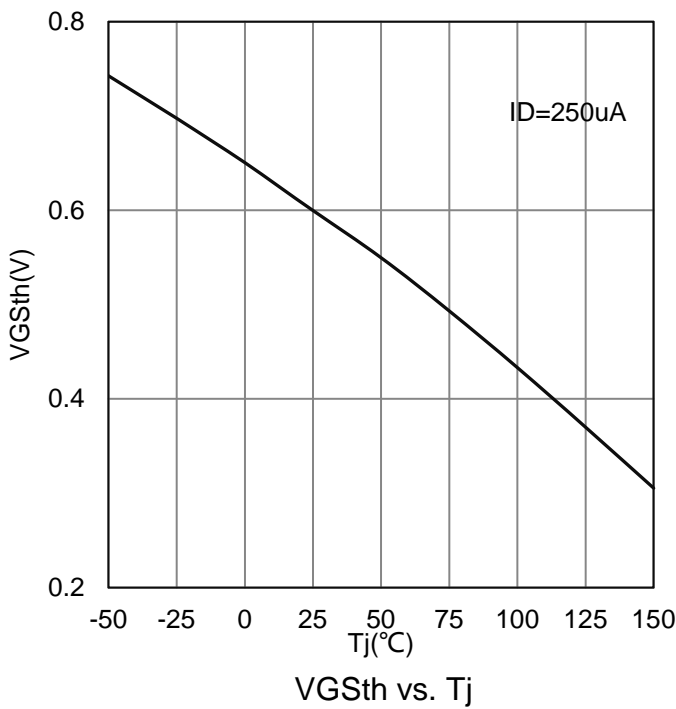
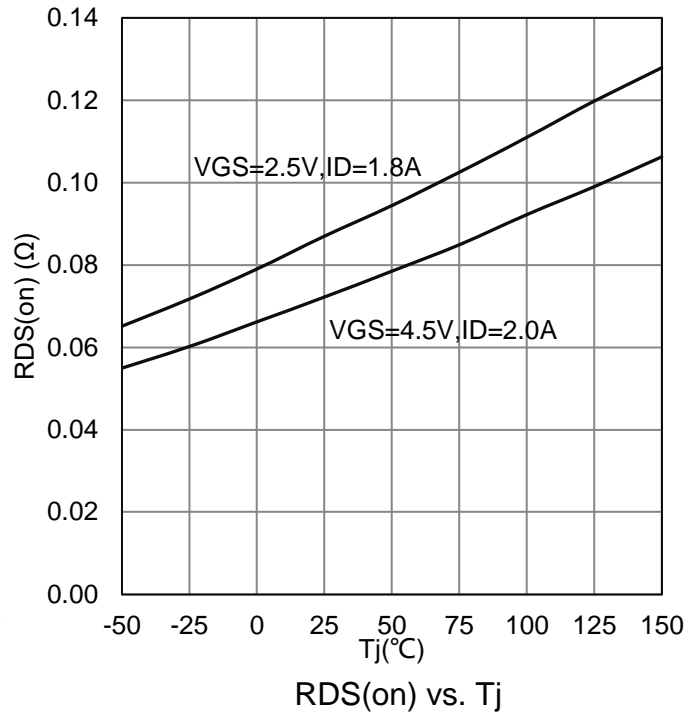
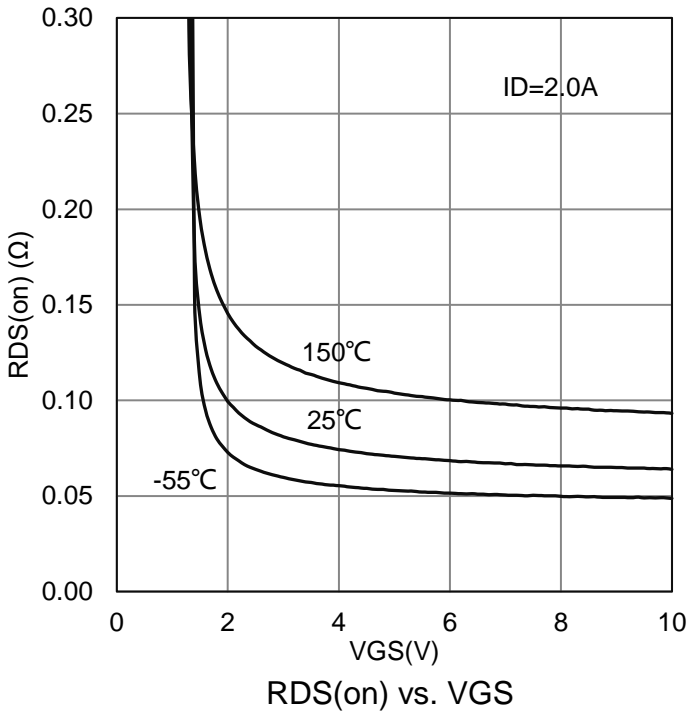
Characteristic	Symbol	Min.	Typ.	Max.	Unit	
Static						
Drain–Source Breakdown Voltage (VGS = 0 V, ID = -250 μA)	VBRDSS	-20	-	-	V	
Gate-Source Threshold Voltage (VDS = VGS, ID = -250 μA)	VGS(th)	-0.4	-	-0.9	V	
Gate-Body Leakage Current (VDS = 0 V, VGS = ± 12 V)	IGSS	-	-	± 100	nA	
Zero Gate Voltage Drain Current (VDS = -16 V, VGS = 0 V)	IDSS	-	-	-500	nA	
Drain-Source On-Resistance(Note 4) (VGS = -4.5 V, ID = -2 A) (VGS = -2.5 V, ID = -1.8 A)	RDS(ON)	-	-	100 130	mΩ	
Diode Forward Voltage (IS = -1 A, VGS = 0 V)	VSD	-0.4	-0.8	-1.2	V	
Dynamic						
Total Gate Charge	(VDS = -10 V, VGS = -4.5 V, ID = -2 A)	Qg	-	5	-	nC
Gate-Source Charge		Qgs	-	0.6	-	
Gate-Drain Charge		Qgd	-	1.4	-	
Turn-On Delay Time	(VDS = -6 V, VGEN = -4.5 V, ID = -1 A, RG = 6Ω, RL = 6Ω)	td(on)	-	4	-	ns
Rise Time		tr	-	11	-	
Turn-Off Delay Time		td(off)	-	84	-	
Fall Time		tf	-	45	-	
Input Capacitance	(VDS = -10 V, VGS = 0 V, f = 1 MHz)	Ciss	-	495	-	pF
Output Capacitance		Coss	-	46	-	
Reverse Transfer Capacitance		Crss	-	35	-	

4. Pulse test; pulse width ≤ 300μs, duty cycle ≤ 2%

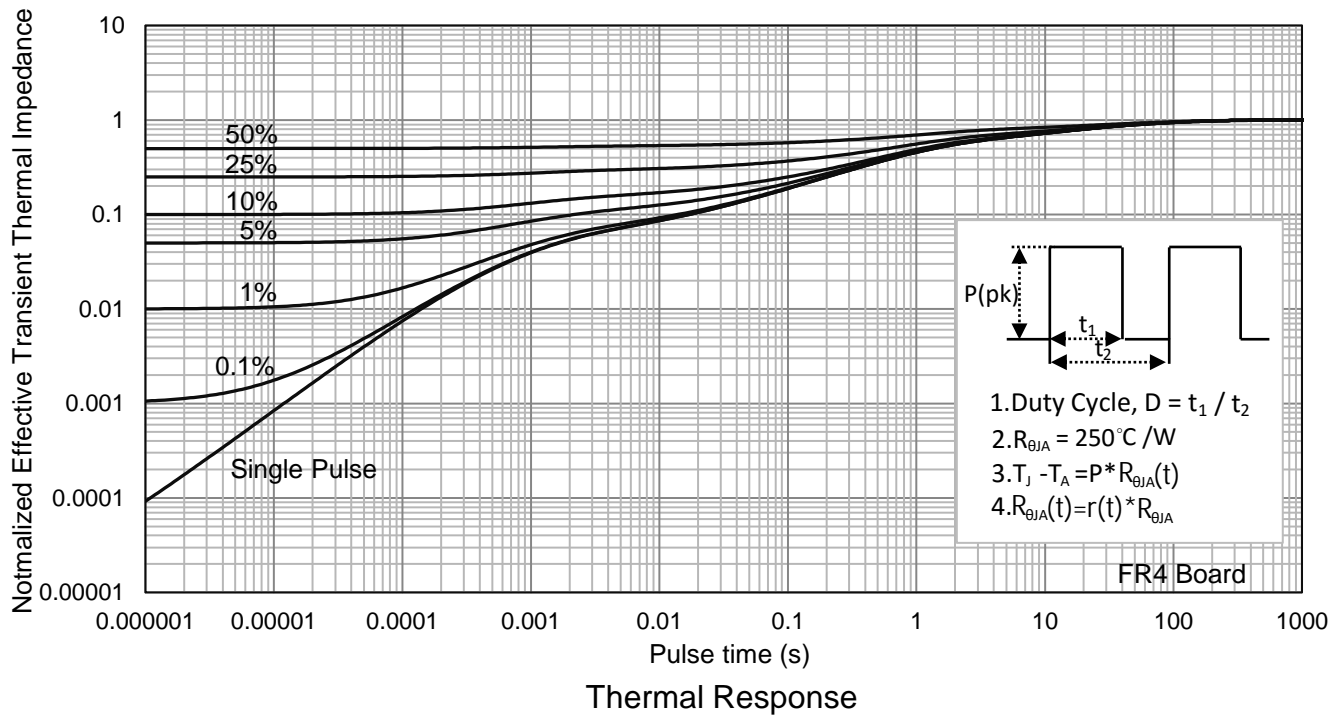
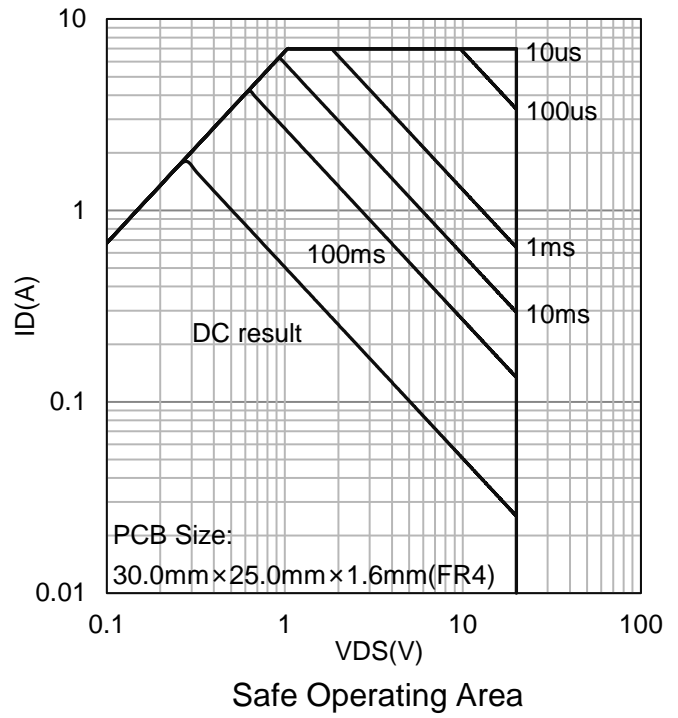
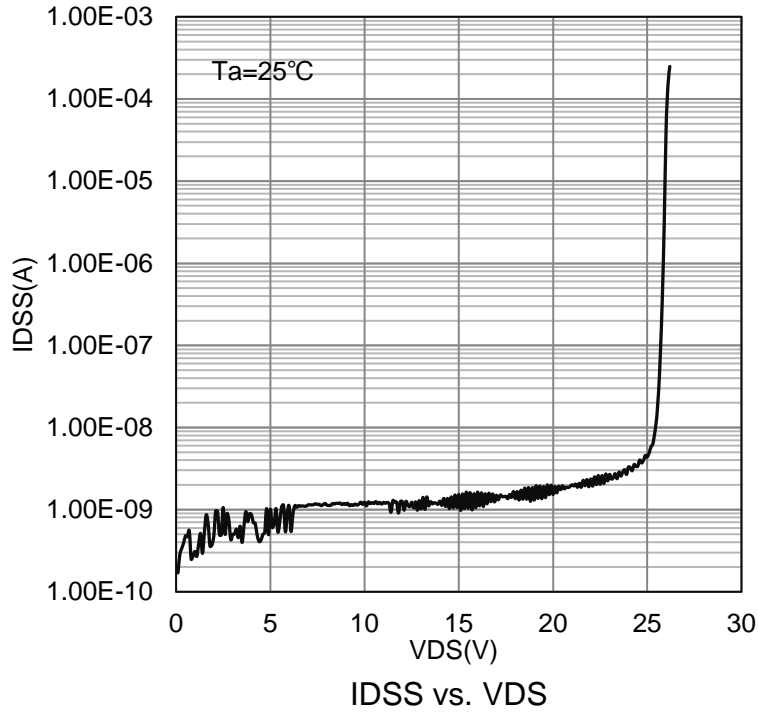
7. ELECTRICAL CHARACTERISTICS CURVES



7. ELECTRICAL CHARACTERISTICS CURVES(Con.)



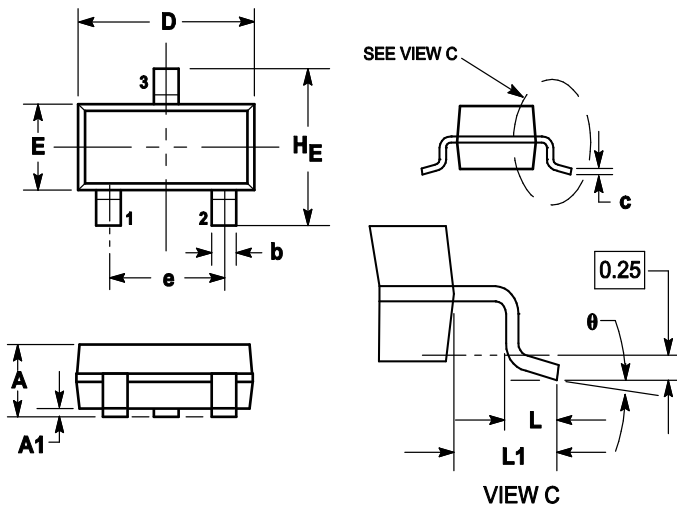
7. ELECTRICAL CHARACTERISTICS CURVES(Con.)



8. OUTLINE AND DIMENSIONS

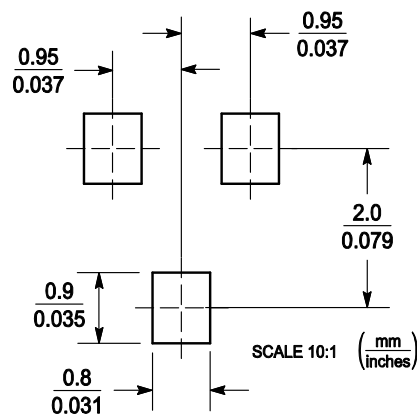
Notes:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.



DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.89	1	1.11	0.035	0.04	0.044
A1	0.01	0.06	0.1	0.001	0.002	0.004
b	0.37	0.44	0.5	0.015	0.018	0.02
c	0.09	0.13	0.18	0.003	0.005	0.007
D	2.80	2.9	3.04	0.11	0.114	0.12
E	1.20	1.3	1.4	0.047	0.051	0.055
e	1.78	1.9	2.04	0.07	0.075	0.081
L	0.10	0.2	0.3	0.004	0.008	0.012
L1	0.35	0.54	0.69	0.014	0.021	0.029
H _E	2.10	2.4	2.64	0.083	0.094	0.104
θ	0°	---	10°	0°	---	10°

9. SOLDERING FOOTPRINT



DISCLAIMER

- Curve guarantee in the specification. The curve of test items with electric parameter is used as quality guarantee. The curve of test items without electric parameter is used as reference only.
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