Ultra Low Current Consumption
300mA CMOS Voltage Regulator

LR6232 Series

■ INTRODUCTION

The LR6232 series are a group of positive voltage regulators manufactured by CMOS technologies with ultra low power consumption and low dropout voltage, which provide large output currents even when the difference of the input-output voltage is small. The LR6232 series can deliver 300mA output current and allow an input voltage as high as 8V. The series are very suitable for the battery-powered equipments, such as RF applications and other systems requiring a quiet voltage source.

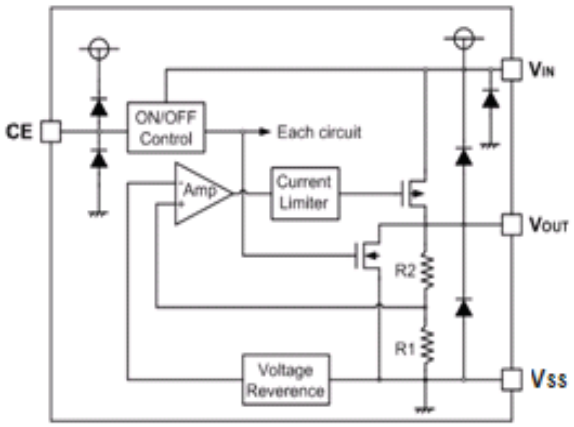
■ FEATURES

- Low Quiescent Current: 0.8μA
- Operating Voltage Range: 1.8V～8V
- Output Current: 300mA
- Low Dropout Voltage：
  110mV@100mA(V_{OUT}=3.3V)
- Output Voltage: 1.0~ 5.0V
- High Accuracy: ±2%/±1%（Typ.）
- High Power Supply Rejection Ratio:
  50dB@1kHz
- Low Output Noise:
  27xV_{OUT} μV_{RMS} (10Hz~100kHz)
- Excellent Line and Load Transient Response
- Built-in Current Limiter, Short-Circuit Protection

■ APPLICATIONS

- Portable consumer equipments
- Radio control systems
- Laptop, Palmtops and PDAs
- Wireless Communication Equipments
- Portable Audio Video Equipments
- Ultra Low Power Microcontroller

■ BLOCK DIAGRAM



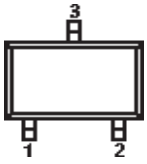
■ ORDER INFORMATION

LR6232①②③④⑤

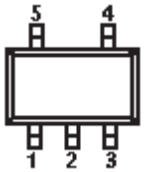
DESIGNATOR	SYMBOL	DESCRIPTION
①	A	**Standard**
	B	**High Active, pull-down resistor built in, with C_{OUT} discharge resistor**
②	Integer	**Output Voltage e.g.1.8V=18 2.8V=28**
③	M/MC/MY	Package:SOT-23-3
	M	Package:SOT-23-5
	P/PT/PL	Package:SOT-89-3
	F	Package:DFN1X1-4
④	T5AG	Tape information—With pin1 in quadrant 1 (DFN1X1-4)
	-	Tape information—With pin1 in quadrant 3 (DFN1X1-4)
⑤	-	Vout tolerance: ±2%
	1	Vout tolerance: ±1%

■ PIN CONFIGURATION

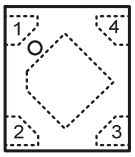
SOT-23-3



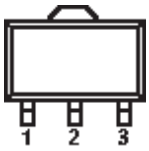
SOT-23-5



DFN1×1-4



SOT-89-3



PIN NUMBER						PIN NAME	FUNCTION
SOT-23-3			SOT-89-3				
M	MC	MY	P	PT	PL		
1	3	3	1	2	2	V_{SS}	Ground
2	2	1	3	1	3	V_{OUT}	Output
3	1	2	2	3	1	V_{IN}	Power input

SOT-23-5

PIN NUMBER	SYMBOL	FUNCTION
1	V_{IN}	Power Input Pin
2	V_{SS}	Ground
3	CE	Chip Enable Pin
4	NC	No Connection
5	V_{OUT}	Output Pin

DFN1X1-4

PIN NUMBER	SYMBOL	FUNCTION
F		
1	V_{OUT}	Output Pin
2	V_{SS}	Ground
3	CE	Chip Enable Pin
4	V_{IN}	Power Input Pin

■ ABSOLUTE MAXIMUM RATINGS(1)

(Unless otherwise specified, T_A=25°C)

PARAMETER		SYMBOL	RATINGS	UNITS
Input Voltage(2)		V_{IN}	-0.3~9	V
Output Voltage(2)		V_{OUT}	-0.3~V_{IN}+0.3	V
Output Current		I_{OUT}	600	mA
Power Dissipation	SOT-23	P_D	0.3	W
	DFN1X1-4		0.4	W
	SOT-89		0.5	W
Operating Junction Temperature Range		T_j	-40~125	°C
Storage Temperature		T_{stg}	-40~125	°C
Lead Temperature(Soldering, 10 sec)		T_{solder}	260	°C

Note:

(1) Stresses beyond those listed under *absolute maximum ratings may* cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods my affect device reliability.

(2) All voltages are with respect to network ground terminal.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	MIN.	NOM.	MAX.	UNITS
Supply voltage at V_{IN}	1.8		8	V
Operating junction temperature range, T_j	-40		125	°C
Operating free air temperature range, T_A	-40		85	°C

■ ELECTRICAL CHARACTERISTICS

LR6232 Series **(V_{IN}=V_{OUT}+1V, C_{IN}=C_{OUT}=1μF, T_A=25℃,unless otherwise specified)**

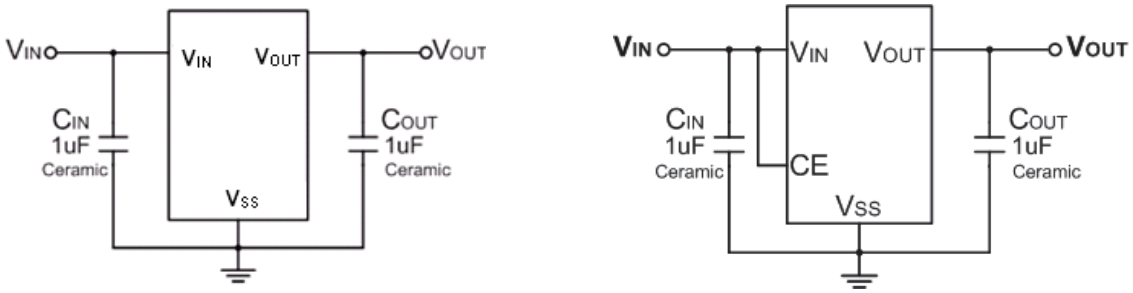
PARAMETER	SYMBOL	CONDITIONS		MIN.	TYP.(3)	MAX.	UNITS
Input Voltage	V_{IN}			1.8	—	8	V
Output Voltage Range	V_{OUT}			1.0	—	5	V
DC Output Accuracy		I_{OUT}=1mA		-2	—	2	%
				-1	—	1	%
Dropout Voltage	V_{dif}(4)	I_{OUT} =100mA,V_{OUT}=3.3V		—	110	—	mV
Supply Current	I_{SS}	I_{OUT} =0	1.2V≤V_{OUT}≤3.3V	—	0.8	1.3	μA
			3.3V<V_{OUT}≤5.0V		1.0	1.5	μA
Standby Current	I_{STBY}	CE=V_{SS}				0.1	μA
Line Regulation	$\frac{\Delta V_{OUT}}{V_{OUT} \times \Delta V_{IN}}$	I_{OUT} =10mA V_{OUT} +1V≤V_{IN}≤8V		—	0.05	0.3	%/V
Load Regulation	ΔV_{OUT}	V_{IN}= V_{OUT} +1V, 1mA≤I_{OUT}≤100mA		—	10	—	mV
Temperature Coefficient	$\frac{\Delta V_{OUT}}{V_{OUT} \times \Delta T_A}$	I_{OUT}=10mA, -40°C<T_A<125°C			100		ppm
Output Current Limit	I_{LIM}	V_{OUT}= 0.5 x $V_{OUT(Normal)}$, V_{IN} = 5V		550	700	850	mA
Short Current	I_{SHORT}	V_{OUT} =V_{SS}		—	20	—	mA
Power Supply Rejection Ratio	PSRR	I_{OUT}=50mA	100Hz		70		dB
			1kHz	—	50	—	
			10kHz	—	40	—	
			100kHz	—	35	—	
Output Noise Voltage	V_{ON}	BW=10Hz to 100kHz		—	27 x V_{OUT}	—	μV_{RMS}
CE "High" Voltage	V_{CE}"H"			1.5		V_{IN}	V
CE "Low" Voltage	V_{CE}"L"					0.3	V
C_{OUT} Auto-Discharge Resistance	$R_{DISCHRG}$	V_{IN}=5V, V_{OUT}=3.0V, V_{CE}=V_{SS}			200		Ω

Note:

(3) Typical numbers are at 25°C and represent the most likely norm.

(4) V_{dif}: The Difference Of Output Voltage And Input Voltage When Input Voltage Is Decreased Gradually Till Output Voltage Equals To 98% Of V_{OUT} (E).

■ TYPICAL APPLICATION CIRCUIT



■ APPLICATION INFORMATION

Selection of Input/ Output Capacitors

In general, all the capacitors need to be low leakage. Any leakage the capacitors have will reduce efficiency, increase the quiescent current.

A recent trend in the design of portable devices has been to use ceramic capacitors to filter DC-DC converter inputs. Ceramic capacitors are often chosen because of their small size, low equivalent series resistance (ESR) and high RMS current capability. Also, recently, designers have been looking to ceramic capacitors due to shortages of tantalum capacitors.

Unfortunately, using ceramic capacitors for input filtering can cause problems. Applying a voltage step to a ceramic capacitor causes a large current surge that stores energy in the inductances of the power leads. A large voltage spike is created when the stored energy is transferred from these inductances into the ceramic capacitor. These voltage spikes can easily be twice the amplitude of the input voltage step.

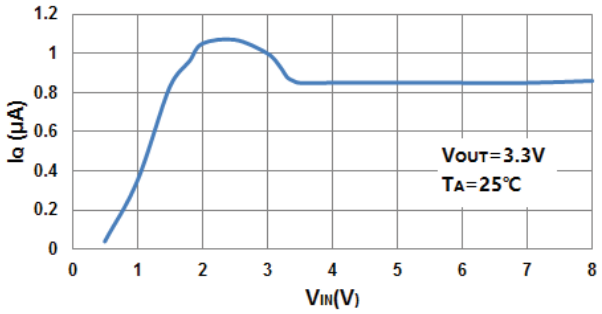
Many types of capacitors can be used for input bypassing, however, caution must be exercised when using multilayer ceramic capacitors (MLCC). Because of the self-resonant and high Q characteristics of some types of ceramic capacitors, high voltage transients can be generated under some start-up conditions, such as connecting the LDO input to a live power source. Adding a 3Ω resistor in series with an X5R ceramic capacitor will minimize start-up voltage transients.

The LDO also requires an output capacitor for loop stability. Connect a 1μF tantalum capacitor from OUT to GND close to the pins. For improved transient response, this output capacitor may be ceramic.

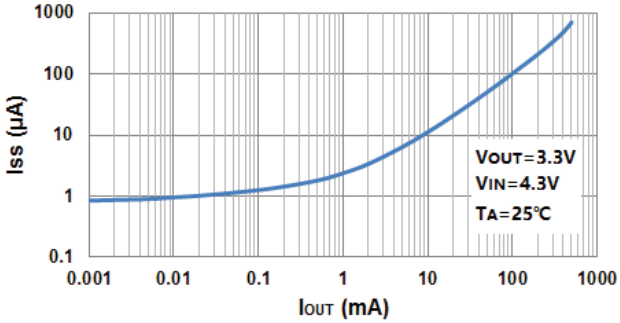
■ YPICAL PERFORMANCE CHARACTERISTICS

(V_{IN}=V_{OUT}+1V, C_{IN}=C_{OUT}=1μF，T_A=25℃,unless otherwise specified)

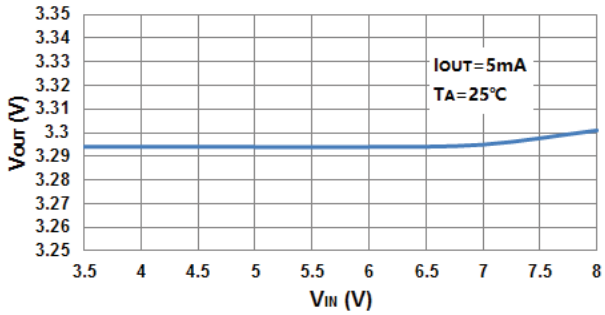
IQ vs. VIN



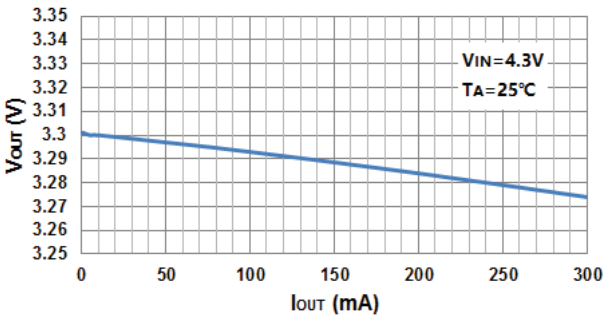
Iss vs. IOUT



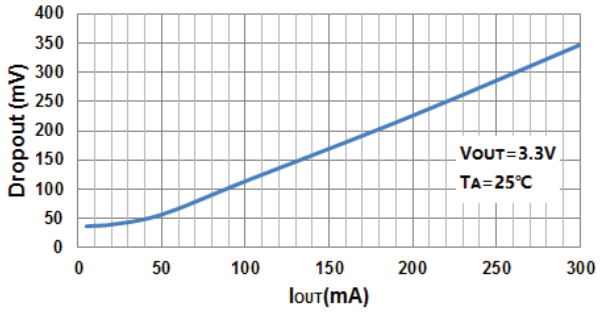
VOUT vs. VIN



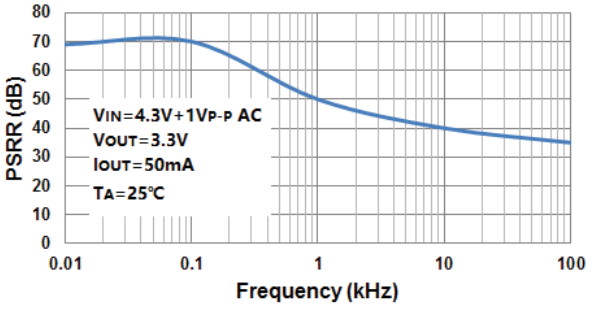
VOUT vs. IOUT

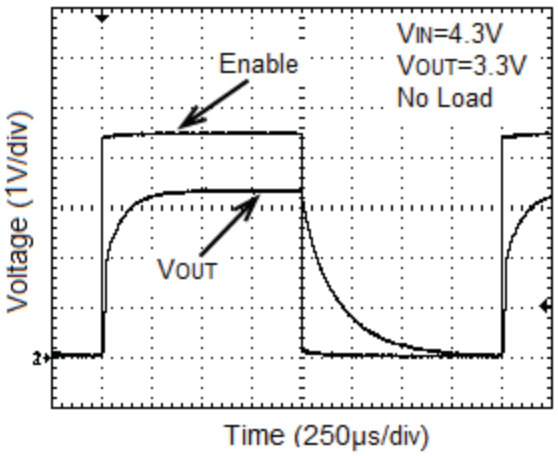


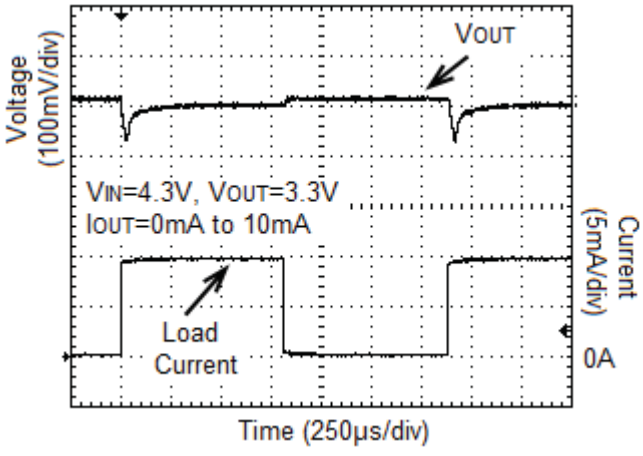
Dropout vs. IOUT



PSRR vs. Frequency

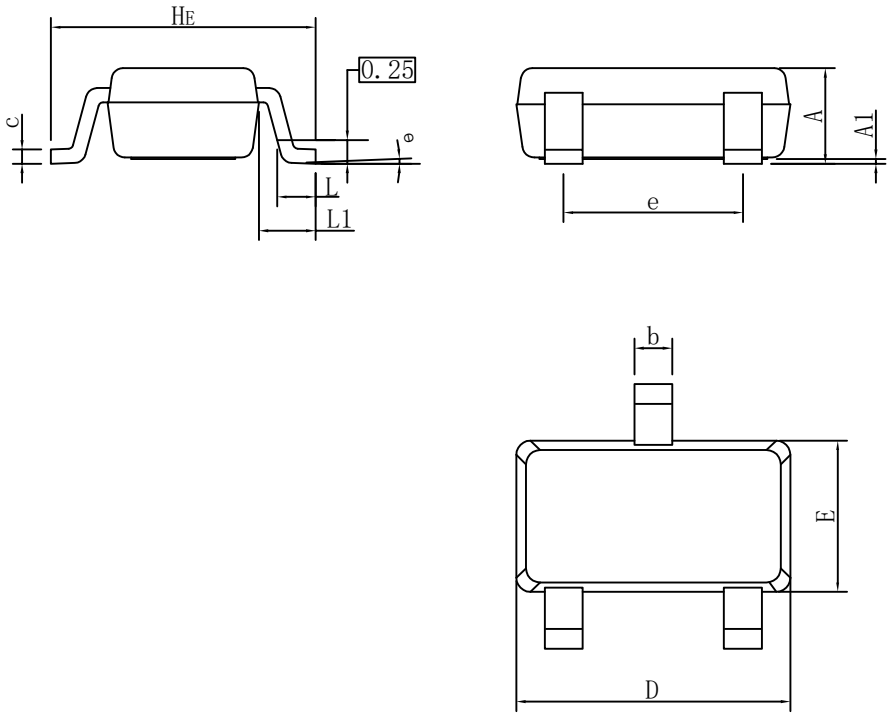






■ PACKAGING INFORMATION

● SOT-23-3 PACKAGE OUTLINE DIMENSIONS

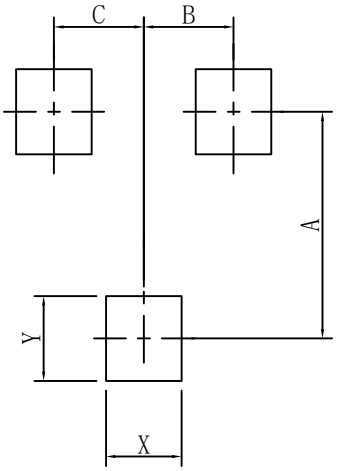


SOT23LC			
DIM	MIN	NOR	MAX
A	0.90	1.00	1.10
A1	0.01	0.06	0.10
b	0.30	0.40	0.50
c	0.10	0.17	0.20
D	2.80	2.90	3.00
E	1.50	1.60	1.70
e	1.80	1.90	2.00
L	0.20	0.40	0.60
L1	0.60REF		
HE	2.60	2.80	3.00
θ	0°	-	10°
All Dimensions in mm			

GENERAL NOTES

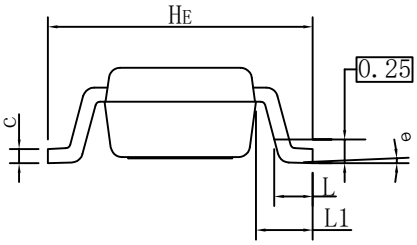
1. Top package surface finish Ra0.4±0.2um
2. Bottom package surface finish Ra0.7±0.2um
3. Side package surface finish Ra0.4±0.2um

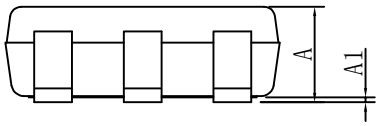
■ RECOMMENDED PAD LAYOUT

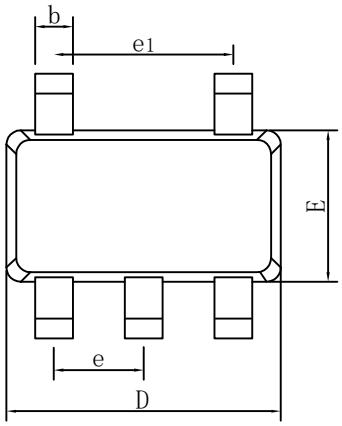


DIM	(mm)
X	0.80
Y	0.90
A	2.40
B	0.95
C	0.95

● SOT-23-5 PACKAGE OUTLINE DIMENSIONS





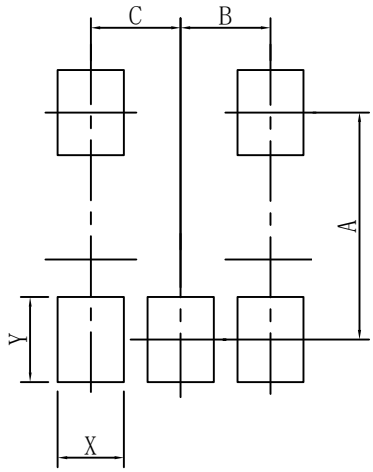


SOT25			
DIM	MIN	NOR	MAX
A	0.90	1.00	1.10
A1	0.01	0.06	0.10
b	0.30	0.40	0.50
c	0.10	0.17	0.20
D	2.80	2.90	3.00
E	1.50	1.60	1.70
e	0.85	0.95	1.05
e1	1.80	1.90	2.00
L	0.20	0.40	0.60
L1	0.60REF		
HE	2.60	2.80	3.00
θ	0°	-	10°

GENERAL NOTES

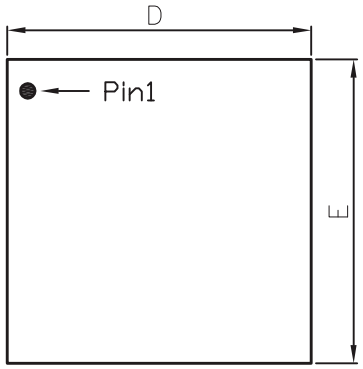
1. Top package surface finish Ra0.4±0.2um
2. Bottom package surface finish Ra0.7±0.2um
3. Side package surface finish Ra0.4±0.2um

■ RECOMMENDED PAD LAYOUT

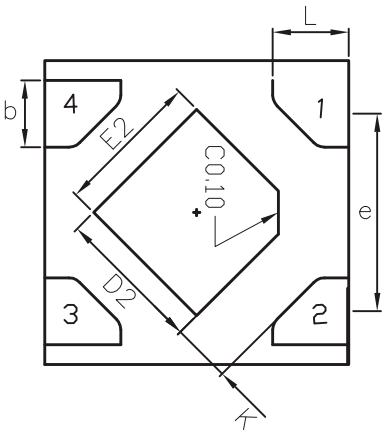


SOT25	
DIM	(mm)
X	0.70
Y	0.90
A	2.40
B	0.95
C	0.95

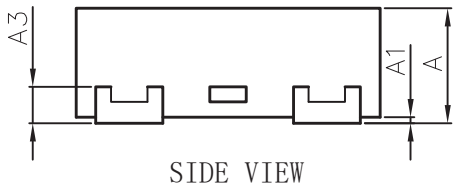
● DFNXX1-4 PACKAGE OUTLINE DIMENSIONS



TOP VIEW



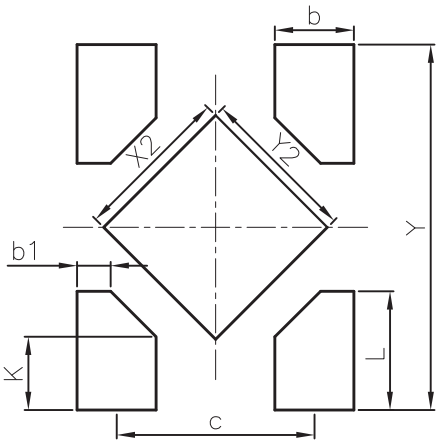
BOTTOM VIEW



SIDE VIEW

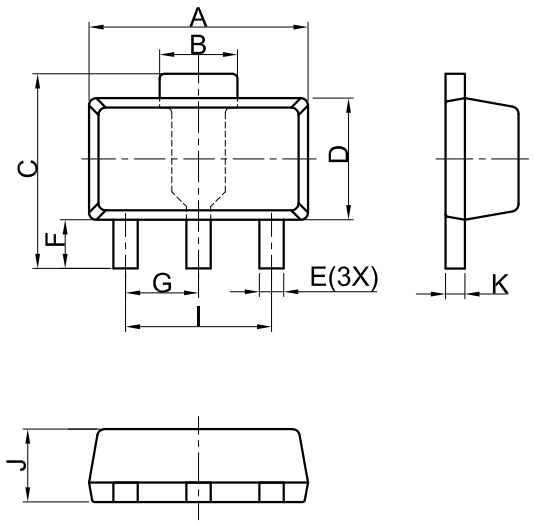
DFN1010			
DIM	MIN	NOR	MAX
A	0.34	0.37	0.40
A1	0.01	0.02	0.05
b	0.17	0.22	0.25
L	0.20	0.25	0.30
D	0.95	1.00	1.05
E	0.95	1.00	1.05
D2	0.43	0.48	0.53
E2	0.43	0.48	0.53
e	0.65		
A3	0.127REF.		
K	0.15	-	-
All Dimensions in mm			

Suggested Pad layout



DFN1010	
DIM	(mm)
X2	0.52
Y2	0.52
L	0.39
Y	1.20
K	0.24
b	0.26
c	0.65
b1	0.11

● SOT-89-3 PACKAGE OUTLINE DIMENSIONS

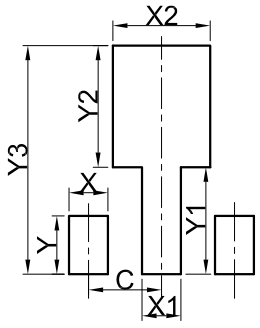


SOT89			
DIM	MIN	NOR	MAX
A	4.30	4.50	4.70
B	1.40	1.60	1.80
C	3.90	4.00	4.25
D	2.30	2.50	2.70
E	0.40	0.50	0.58
F	0.90	1.00	1.20
G	1.50 BSC		
I	3.00 BSC		
J	1.40	1.50	1.60
K	0.34	0.40	0.50
All Dimensions in mm			

GENERAL NOTES

1. Top package surface finish Ra0.4±0.2um
2. Bottom package surface finish Ra0.7±0.2um
3. Side package surface finish Ra0.4±0.2um
4. Protrusion or Gate Burrs shall not exceed 0.10mm per side.

■ RECOMMENDED PAD LAYOUT



SOT89-3	
DIM	(mm)
X	0.80
Y	1.20
X1	0.80
Y1	2.20
X2	2.00
Y2	2.50
C	1.50
Y3	4.70

■ ORDERING INFORMATION APPENDIX

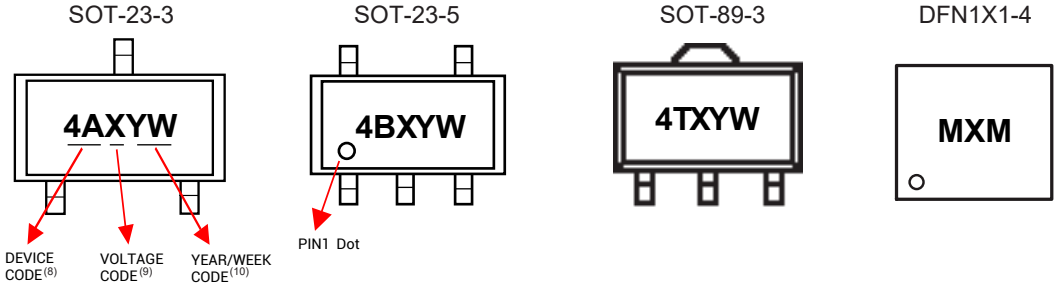
Part Number(5)	Package	Output Voltage(6)	Marking(7)	Shipping
LR6232AxxM	SOT-23-3	1.0V~5.0V(Except3.0V)	4AX	3K/Reel
LR6232A30M	SOT-23-3	3.0V	4RK	3K/Reel
LR6232AxxMC	SOT-23-3	1.0V~5.0V	4CX	3K/Reel
LR6232AxxMY	SOT-23-3	1.0V~5.0V	4YX	3K/Reel
LR6232BxxM	SOT-23-5	1.0V~5.0V	4BX	3K/Reel
LR6232AxxP	SOT-89-3	1.0V~5.0V	4DX	5K/Reel
LR6232AxxPT	SOT-89-3	1.0V~5.0V	4TX	5K/Reel
LR6232AxxPL	SOT-89-3	1.0V~5.0V	4LX	5K/Reel
LR6232BxxF	DFN1X1-4	1.0V~5.0V	MX	10K/Reel
LR6232BxxFT5AG	DFN1X1-4	1.0V~5.0V(Except3.3V)	MX	10K/Reel
LR6232B33FT5AG	DFN1X1-4	3.3V	NL	10K/Reel

(5) The "xx" in part number represents output voltage, eg "18" = 1.8V, "50" = 5.0V.

(6) Output voltage varies from 1.0V to 5.0V, 0.1V an interval.

(7) There are additional marking, which relates to the date code. For detailed information, please refer to MARKING INFORMATION APPENDIX below.

■ MARKING INFORMATION APPENDIX



(8) The first two letters in the Marking represent DEVICE CODE. For DFN1X1-4 package, DEVICE CODE has only one letter.

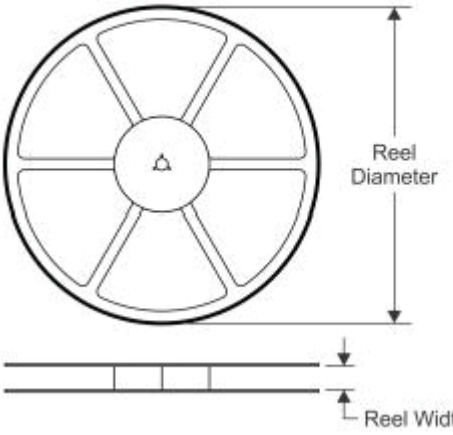
(9) The following letter "X" in the Marking changes along with the output voltage, as the chart shows below.

Voltage(V)	···	1.0	1.2	1.5	1.8	2.5	2.7	2.8	3.0	3.0(1%)	3.3	3.3(1%)	3.6	4.0	5.0	5.0(1%)	···
Symbol	···	D	E	F	G	H	I	J	K	B	L	Q	M	N	P	m	···

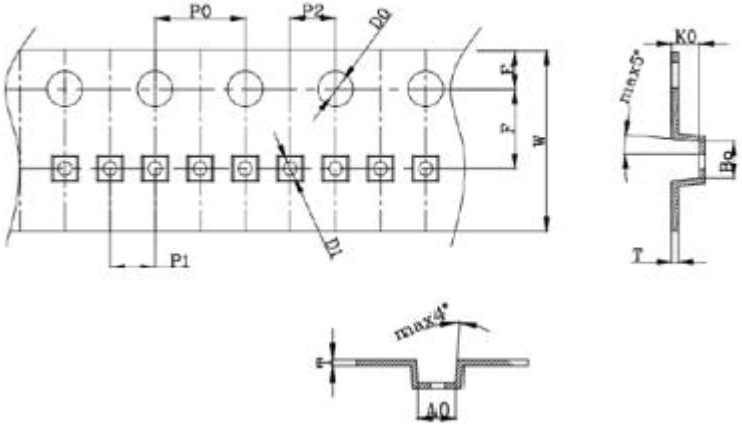
(10) The last two letters in the Marking represent YEAR/WEEK CODE. For DFN1X1-4 package, YEAR/WEEK CODE has only one letter.

■ TAPE AND REEL INFORMATION

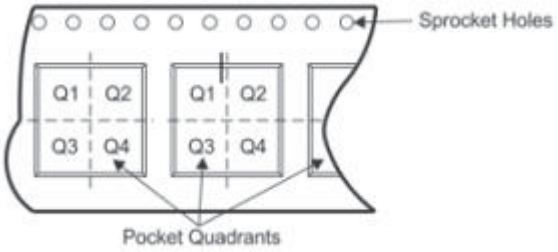
REEL DEMENSIONS



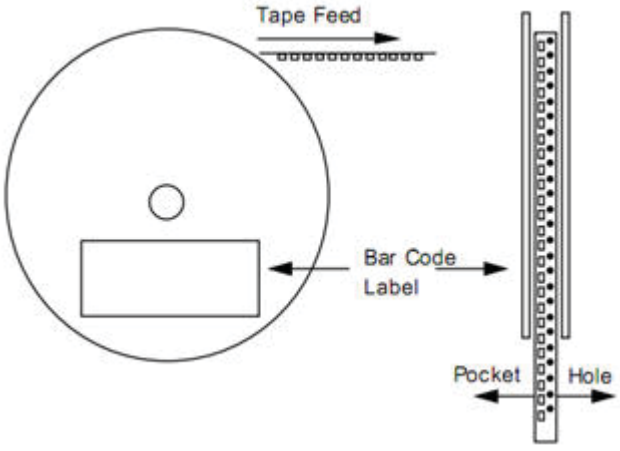
TAPE DEMENSIONS



PIN ORIENTATION



ROLLING ORIENTATION



Device	Package	Reel Diameter (mm)	Reel width (mm)	P0 (mm)	P1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	W (mm)	PIN1
LR6232AxxM	SOT-23-3	178±1	9.6±1.2	4.00±0.1	4.00±0.1	3.1±0.1	3.28±0.1	1.32±0.1	8.0±0.1	NA
LR6232AxxMC	SOT-23-3	178±1	9.6±1.2	4.00±0.1	4.00±0.1	3.1±0.1	3.28±0.1	1.32±0.1	8.0±0.1	NA
LR6232AxxMY	SOT-23-3	178±1	9.6±1.2	4.00±0.1	4.00±0.1	3.1±0.1	3.28±0.1	1.32±0.1	8.0±0.1	NA
LR6232BxxM	SOT-23-5	178±1	9.6±1.2	4.00±0.1	4.00±0.1	3.25±0.05	3.15±0.05	1.5±0.05	8.0±0.1	Q3
LR6232BxxF	DFN1X1-4	178±1	9.6±1.2	4.00±0.1	2.00±0.05	1.16±0.05	1.16±0.05	0.5±0.05	8.0±0.1	Q3
LR6232BxxFT5AG	DFN1X1-4	178±1	9.6±1.2	4.00±0.1	2.00±0.05	1.16±0.05	1.16±0.05	0.5±0.05	8.0±0.1	Q1

■ REVISON HISTORY

Version	Description	Update by	Update Date
0.8	增加产品丝印详细说明。	陈帅	2022-11-29
0.9	增加部分1%精度的电压点marking代码。	陈帅	2024-04-01
1.0	SOT-89包装数量由1000每卷改为5000每卷.	陈帅	2024-04-01

DISCLAIMER

- Curve guarantee in the specification. The curve of test items with electric parameter is used as quality guarantee. The curve of test items without electric parameter is used as reference only.

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