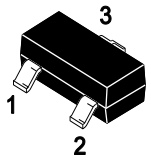
LP2305ALT1G

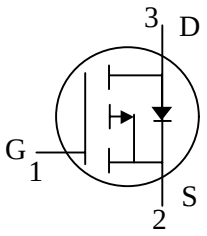
20V P-Channel Enhancement-Mode MOSFET

1. FEATURES

- VDS = -20V
- RDS(ON), VGS@-4.5V, ID@-3.5A = 68mΩ
- RDS(ON), VGS@-2.5V, ID@-3A = 81mΩ
- RDS(ON), VGS@-1.8V, ID@-2A = 118mΩ
- Advanced trench process technology
- High Density Cell Design For Ultra Low On-Resistance
- Fully Characterized Avalanche Voltage and Current
- Improved Shoot-Through FOM
- We declare that the material of product compliance with RoHS requirements and Halogen Free.



SOT23(TO-236)



2. DEVICE MARKING AND ORDERING INFORMATION

Device	Marking	Shipping
LP2305ALT1G	P5A	3000/Tape&Reel
LP2305ALT3G	P5A	10000/Tape&Reel

3. MAXIMUM RATINGS(Ta = 25ºC)

Parameter	Symbol	Limits	Unit
Drain–Source Voltage	VDSS	-20	V
Gate–to–Source Voltage	VGS	±8	V
Continuous Drain Current	ID	-4	A
Pulsed Drain Current(Note 1)	IDM	-12	A
Power Dissipation(Note 2)	PD	1100	mW
Operating Junction and Storage Temperature Range	TJ,Tstg	−55~+150	℃

1. Repetitive Rating: Pulse width limited by the maximum junction temperature
2.FR–5 = 1.0×0.75×0.062 in.

4. THERMAL CHARACTERISTICS

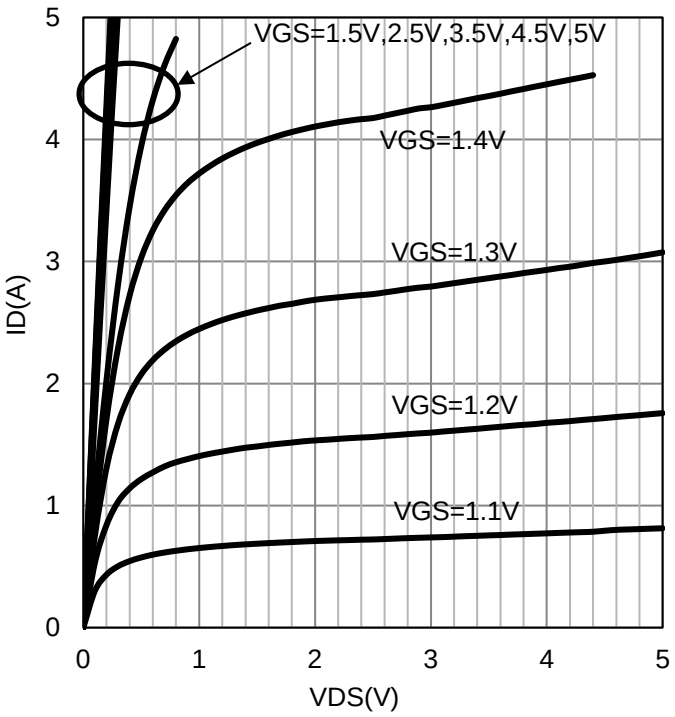
Parameter	Symbol	Limits	Unit
Thermal Resistance, Junction–to–Ambient	RΘJA	110	ºC/W

5. ELECTRICAL CHARACTERISTICS (Ta= 25°C)

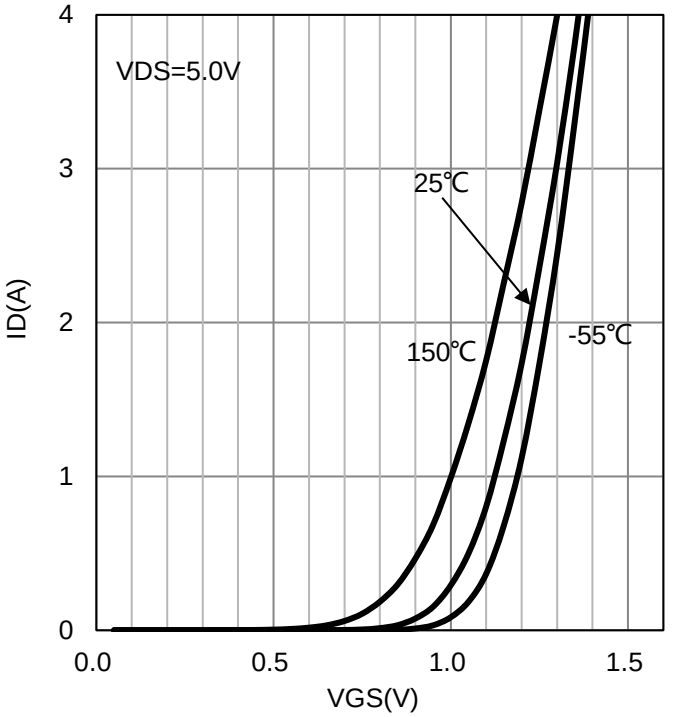
Characteristic		Symbol	Min.	Typ.	Max.	Unit
Static						
Drain–Source Breakdown Voltage (VGS = 0, ID = -250μA)		VBRDSS	-20	-	-	V
Zero Gate Voltage Drain Current (VGS = 0, VDS = -6.4 V)		IDSS	-	-	-1	μA
Gate–Body Leakage Current (VGS= ± 8V, VDS = 0V)		IGSS	-	-	±100	nA
Forward Transconductance (VDS = -5V, ID = -3.5A)		gfs	-	8.5	-	S
Gate Threshold Voltage (VDS = VGS, ID = -250μA)		VGS(th)	-0.45	-	-0.8	V
Static Drain–Source On–State Resistance		RDS(on)				mΩ
(VGS = -4.5 V, ID = -3.5 A)			-	47	68	
(VGS = -2.5 V, ID = -3 A)			-	55	81	
(VGS = -1.8 V, ID = -2 A)			-	67	118	
On-State Drain Current		ID(on)				A
(VDS≤ -5 V, VGS ≤ -4.5 V)			-6	-	-	
(VDS≤ -5 V, VGS ≤ -2.5 V)			-3	-	-	
Source-Drain Diode						
Diode Forward Current		IS	-	-1.6	-	A
Forward Voltage (IS = -1.6A, VGS = 0V)		VSD	-	-	-1.2	V
Dynamic						
Total Gate Charge (VDS=-10V,VGS=-4.5V,ID=-3.0A)		Qg	-	5.76	-	nC
Gate-Source Charge (VDS=-10V,VGS=-4.5V,ID=-3.0A)		Qgs	-	0.88	-	
Gate-Drain Charge (VDS=-10V,VGS=-4.5V,ID=-3.0A)		Qgd	-	2.2	-	
Input Capacitance (VGS = 0 V, f = 1.0MHz,VDS= -4 V)		Ciss	-	1245	-	pF
Output Capacitance (VGS = 0 V, f = 1.0MHz,VDS= -4 V)		Coss	-	375	-	pF
Reverse Transfer Capacitance (VGS = 0 V, f = 1.0MHz,VDS= -4 V)		Crss	-	210	-	pF
Switching						
Turn-On Delay Time	(VDD = -4V, RL= 4Ω ID = -1A, VGEN = -4.5V RG = 6Ω)	td(on)	-	13	20	ns
Rise Time		tr	-	25	40	
Turn-Off Delay Time		td(off)	-	55	80	
Fall Time		tf	-	19	35	

3.Pulse Test: Pulse Width ≤300 μs, Duty Cycle ≤2.0%.

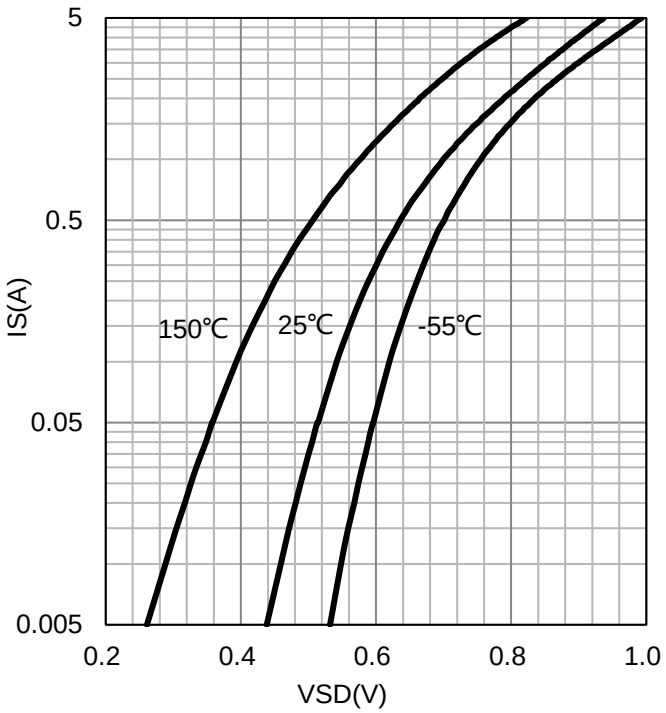
6.ELECTRICAL CHARACTERISTICS CURVES



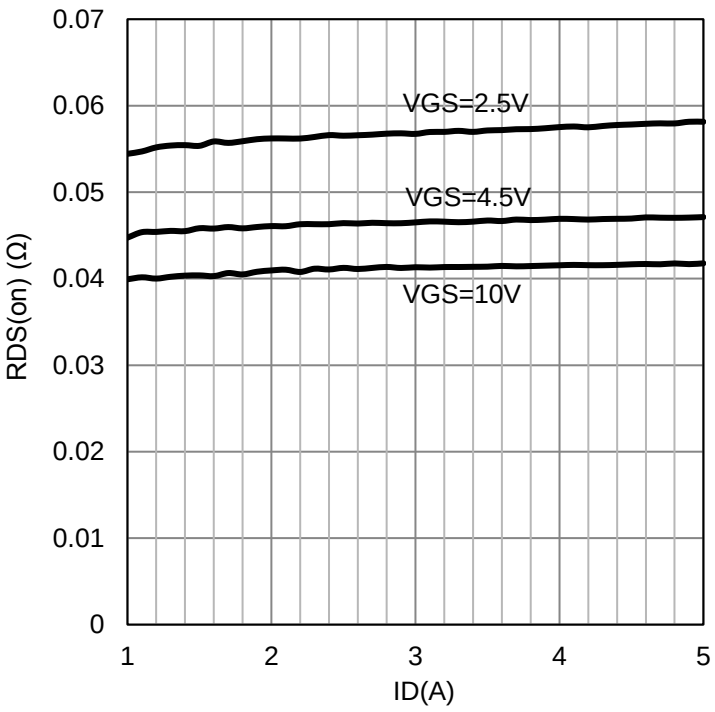
ID vs. VDS



ID vs. VGS

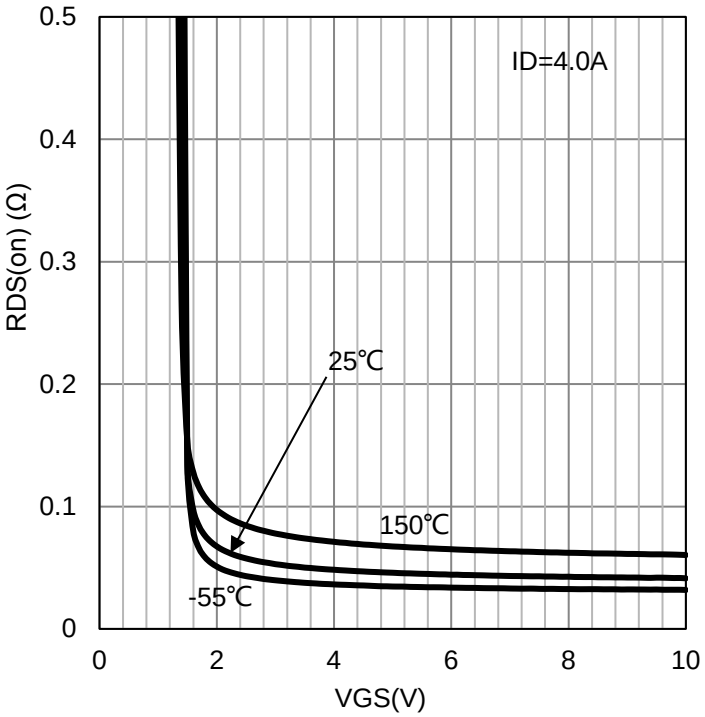


IS vs. VSD

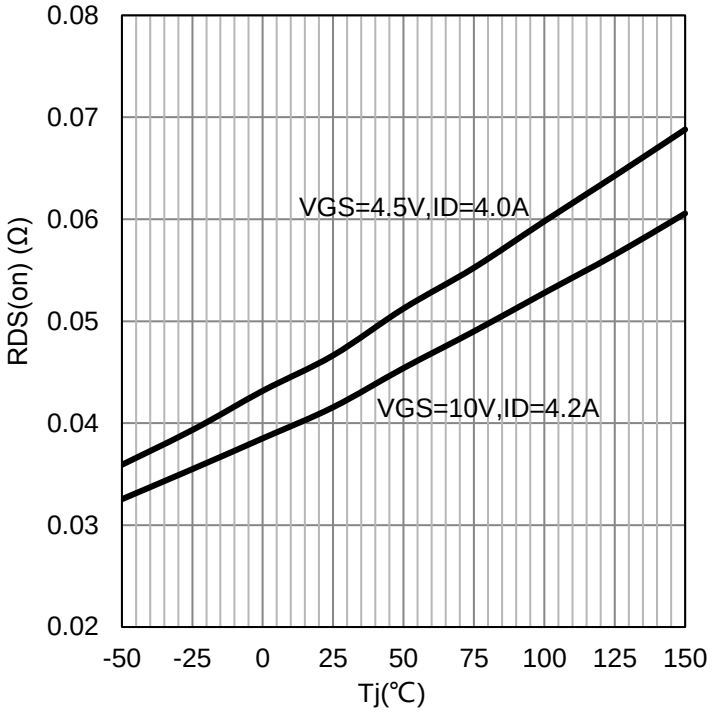


RDS(on) vs. ID

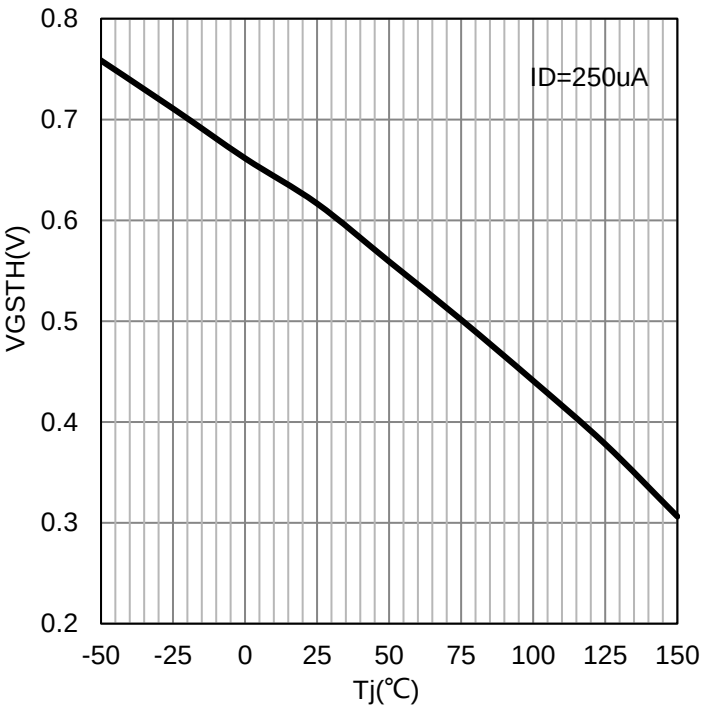
6.ELECTRICAL CHARACTERISTICS CURVES(Con.)



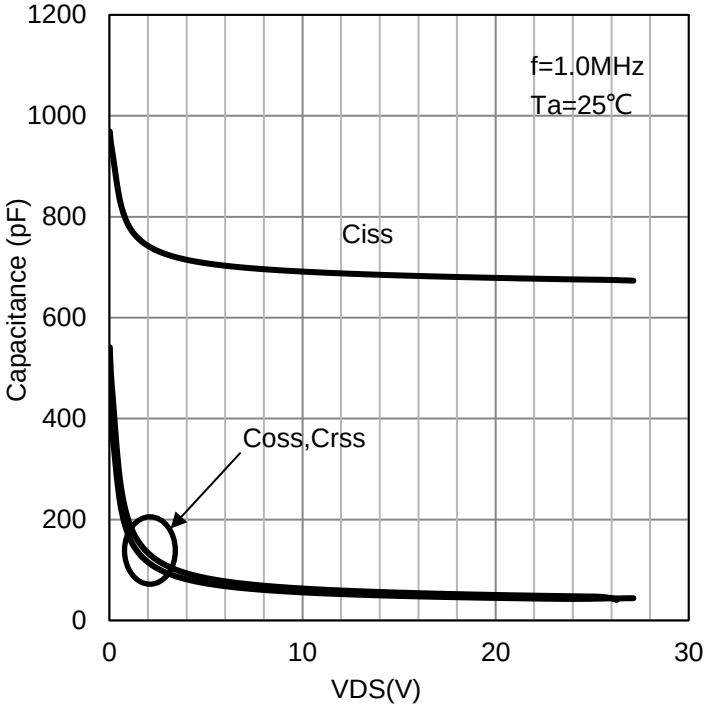
RDS(on) vs. VGS



RDS(on) vs. Tj

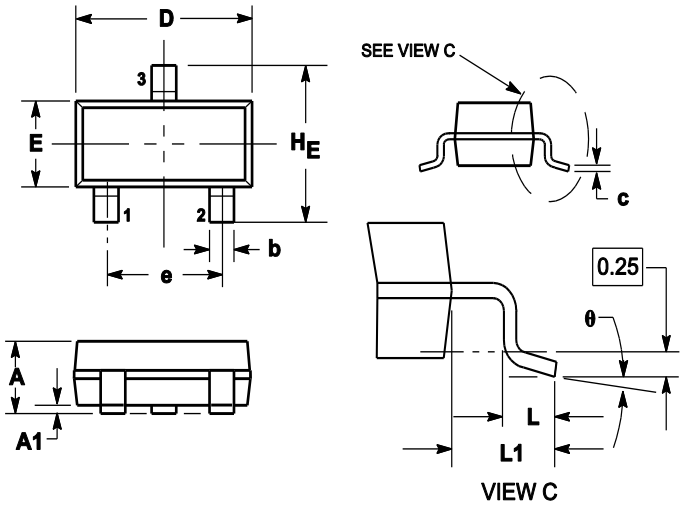


VGSTH vs. Tj



Capacitance

7.OUTLINE AND DIMENSIONS



Notes:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.89	1	1.11	0.035	0.04	0.044
A1	0.01	0.06	0.1	0.001	0.002	0.004
b	0.37	0.44	0.5	0.015	0.018	0.02
c	0.09	0.13	0.18	0.003	0.005	0.007
D	2.80	2.9	3.04	0.11	0.114	0.12
E	1.20	1.3	1.4	0.047	0.051	0.055
e	1.78	1.9	2.04	0.07	0.075	0.081
L	0.10	0.2	0.3	0.004	0.008	0.012
L1	0.35	0.54	0.69	0.014	0.021	0.029
H_E	2.10	2.4	2.64	0.083	0.094	0.104
θ	0°	---	10°	0°	---	10°

8.SOLDERING FOOTPRINT