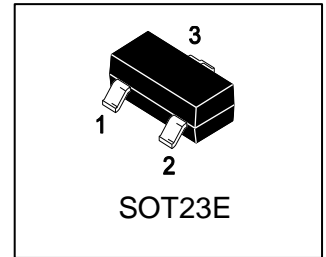


# LP3443LT1G

## 20V P-Channel Enhancement-Mode MOSFET

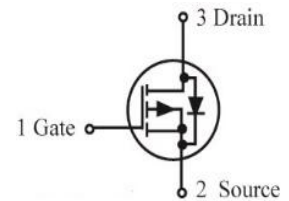


### 1. FEATURES

- $V_{DS} = -20V$
- $R_{DS(ON)} \leq 70m\Omega, @V_{GS} = -4.5V, I_{DS} = -4.7A$
- $R_{DS(ON)} \leq 110m\Omega, @V_{GS} = -2.5V, I_{DS} = -1.0A$
- We declare that the material of product compliance with RoHS requirements and Halogen Free.
- ESD rating of class 0 (<100V)per Human Body Model.

### 2. APPLICATIONS

- Advanced trench process technology
- High density cell design for ultra low on-resistance



### 3. DEVICE MARKING AND ORDERING INFORMATION

Device	Marking	Shipping
LP3443LT1G	P34	3000/Tape&Reel
LP3443LT3G	P34	10000/Tape&Reel

### 4. MAXIMUM RATINGS( $T_a = 25^\circ C$ )

Parameter	Symbol	Limits	Unit
Drain-Source Voltage	$V_{DS}$	-20	V
Gate-to-Source Voltage – Continuous	$V_{GS}$	$\pm 12$	V
Drain Current			A
– Continuous $T_A = 25^\circ C$	$I_D$	-4.7	
– Pulsed (Note 1)	$I_{DM}$	-20	
Avalanche Current( $L=0.1mH$ )	$I_{AS}$	10	A
Avalanche Energy( $L=0.1mH$ )	$E_{AS}$	5	mJ

### 5. THERMAL CHARACTERISTICS

Parameter	Symbol	Limits	Unit
Power Dissipation	PD	1.1	W
		0.7	W
Thermal Resistance, Junction-to-Ambient(Note 2)	$R_{\theta JA}$	110	$^\circ C/W$
Junction-to-Ambient(Note 3)	$R_{\theta JA}$	207	
Junction-to-Case	$R_{\theta JC}$	90	
Junction and Storage temperature	$T_J, T_{stg}$	$-55 \sim +150$	$^\circ C$

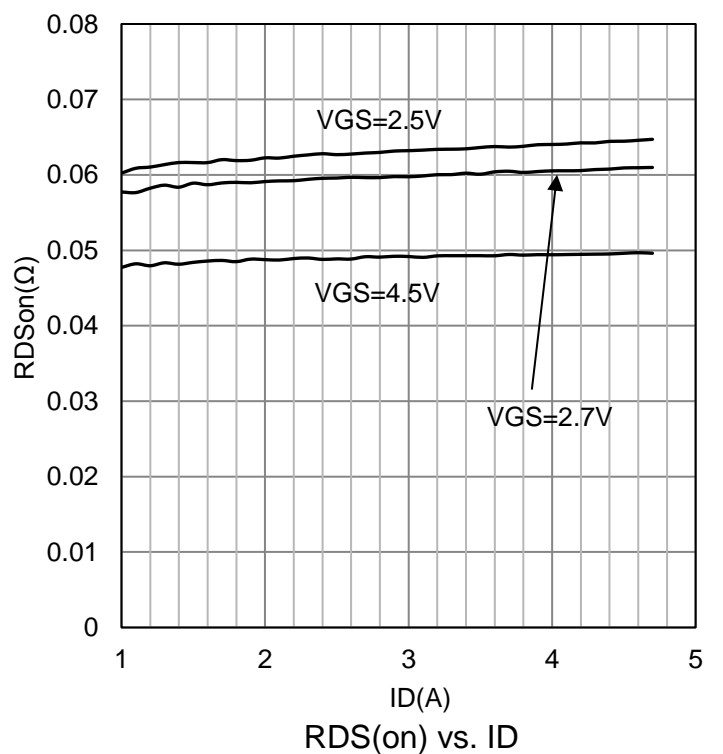
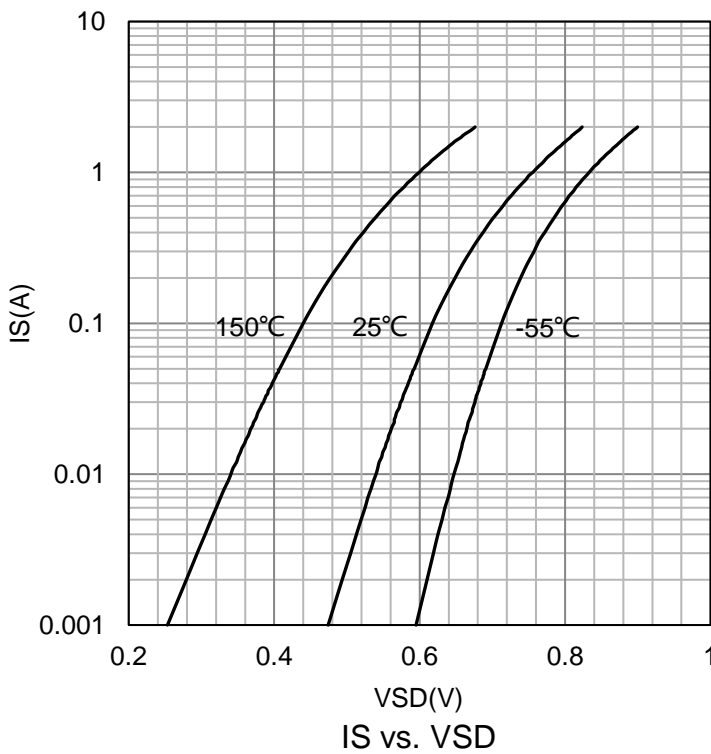
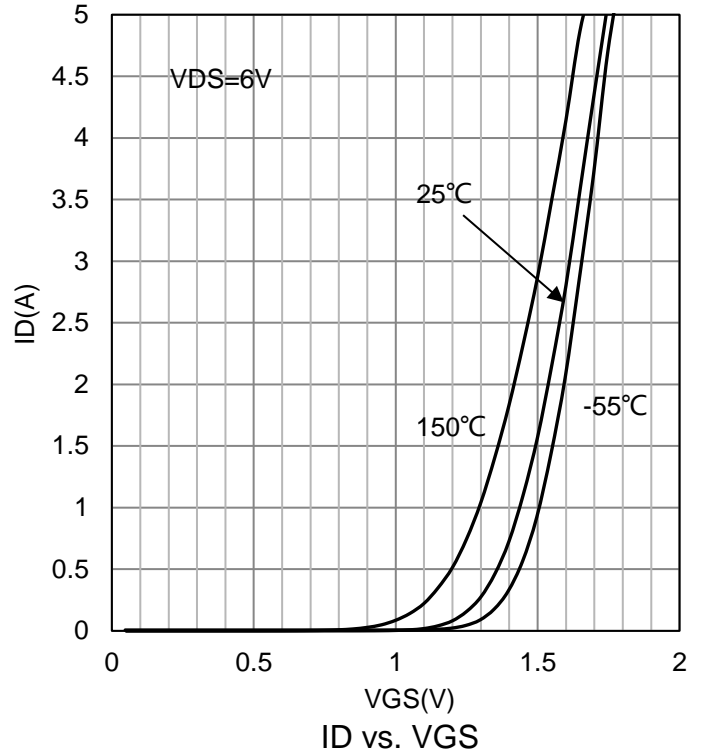
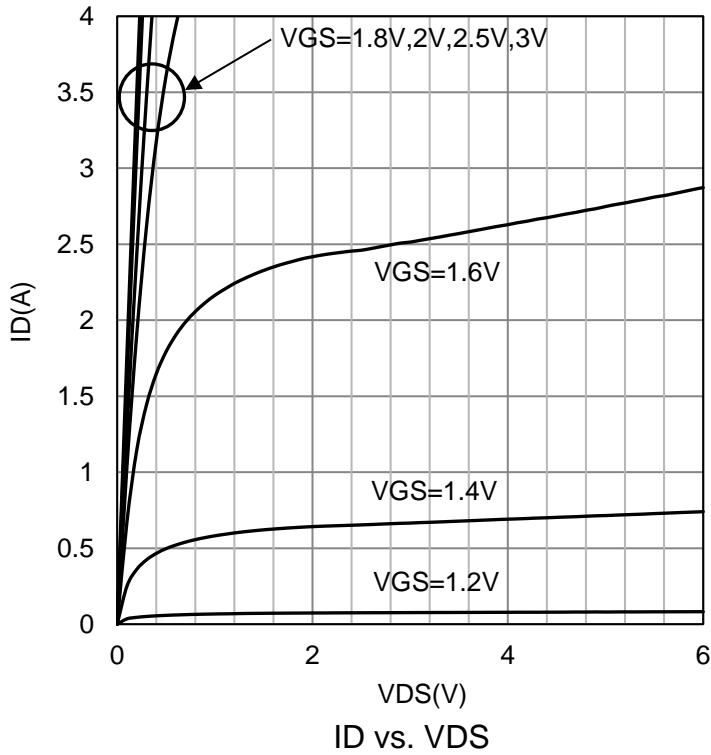
- 1.Repetitive Rating: Pulse width limited by the maximum junction temperature.
- 2.1-in<sup>2</sup> 2oz Cu PCB board.
- 3.Surface mounted on FR4 board using the minimum recommended pad size.

## 6. ELECTRICAL CHARACTERISTICS (Ta= 25°C)

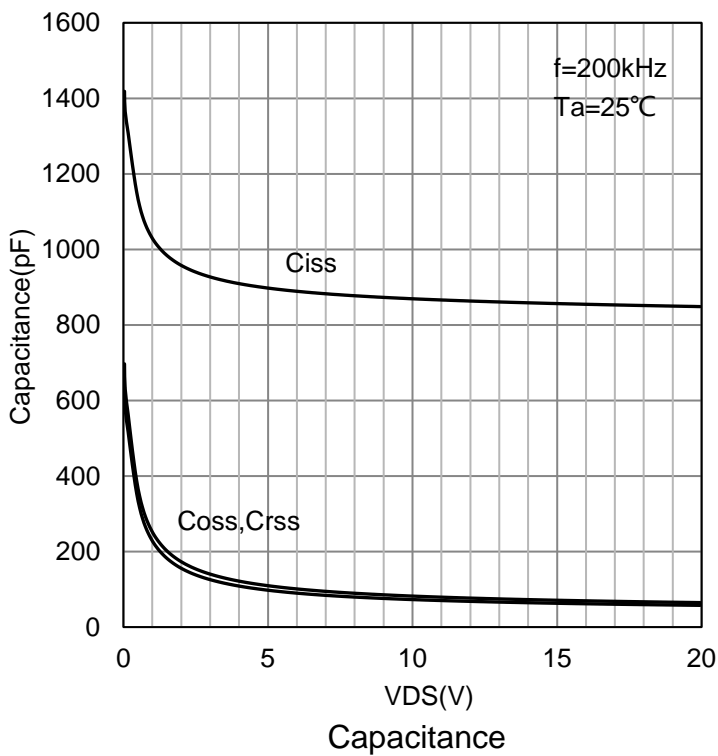
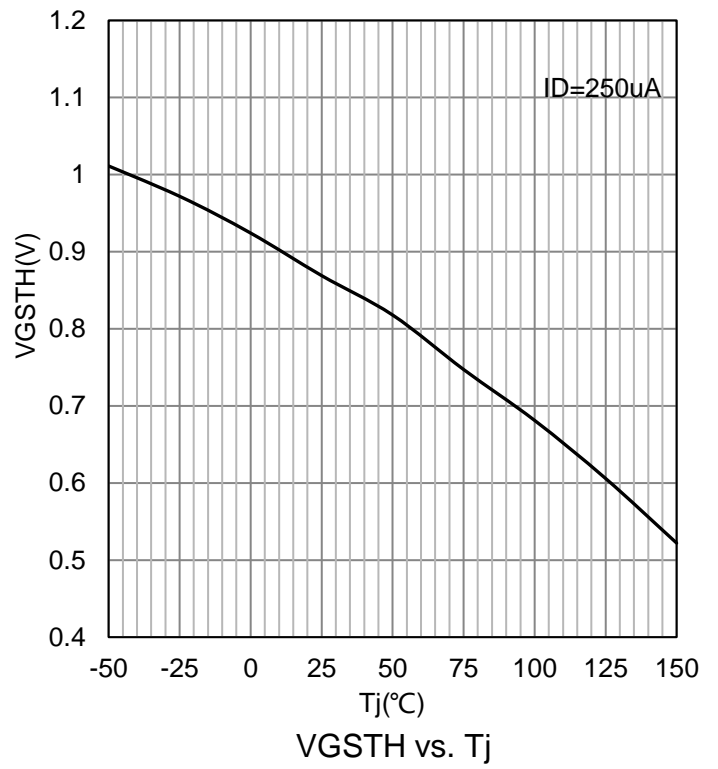
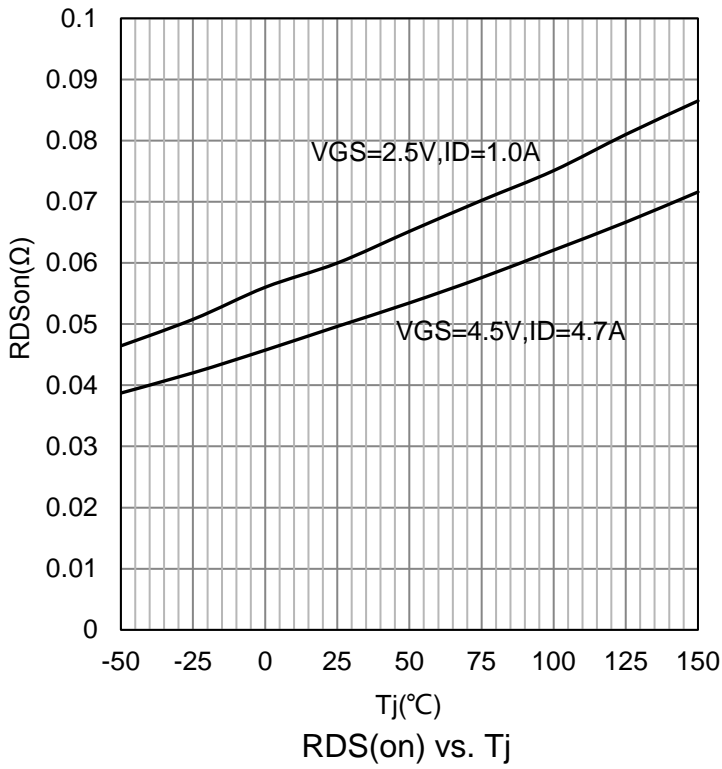
Characteristic	Symbol	Min.	Typ.	Max.	Unit	
<b>STATIC</b>						
Drain–Source Breakdown Voltage (VGS = 0, ID = -250μA)	VBRDSS	-20	-	-	V	
Gate Threshold Voltage (VDS = VGS, ID = -250μA)	VGS(th)	-0.6	-0.85	-1.4	V	
Zero Gate Voltage Drain Current (VGS = 0, VDS = -20 V)	IDSS	-	-	-1	μA	
Gate-to–Source Leakage Current (VDS = 0 V, VGS = ±12 V)	IGSS	-	-	±100	nA	
Static Drain–Source On–State Resistance(Note 4) (VGS = -4.5V, ID = -4.7A) (VGS = -2.7V, ID = -3.8A) (VGS = -2.5V, ID = -1.0A)	RDS(on)	-	58 63 75	70 90 110	mΩ	
Diode Forward Voltage (VGS = 0 V, ISD = -1.7 A)	VSD	-	-	-1.2	V	
<b>DYNAMIC</b>						
Total Gate Charge@10V	(VDS = -10V, ID = -1.5A)	Qg	-	20	-	nC
Total Gate Charge@4.5V		Qg	-	9	-	
Gate-to–Source Gate Charge		Qgs	-	1.5	-	
Gate-to–Drain Charge		Qgd	-	2.7	-	
Turn-On Delay Time	(VDD = -10V, RL = 10Ω, ID = -1A, VGEN = -4.5V, RG = 6.2Ω)	td(on)	-	18	-	ns
Rise Time		tr	-	25	-	
Turn-Off Delay Time		td(off)	-	88	-	
Fall Time		tf	-	42	-	
Input Capacitance	(f = 200kHz, VDS = -10 V)	Ciss	-	869	-	pF
Output Capacitance		Coss	-	82	-	
Reverse Transfer Capacitance		Crss	-	73	-	

4. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

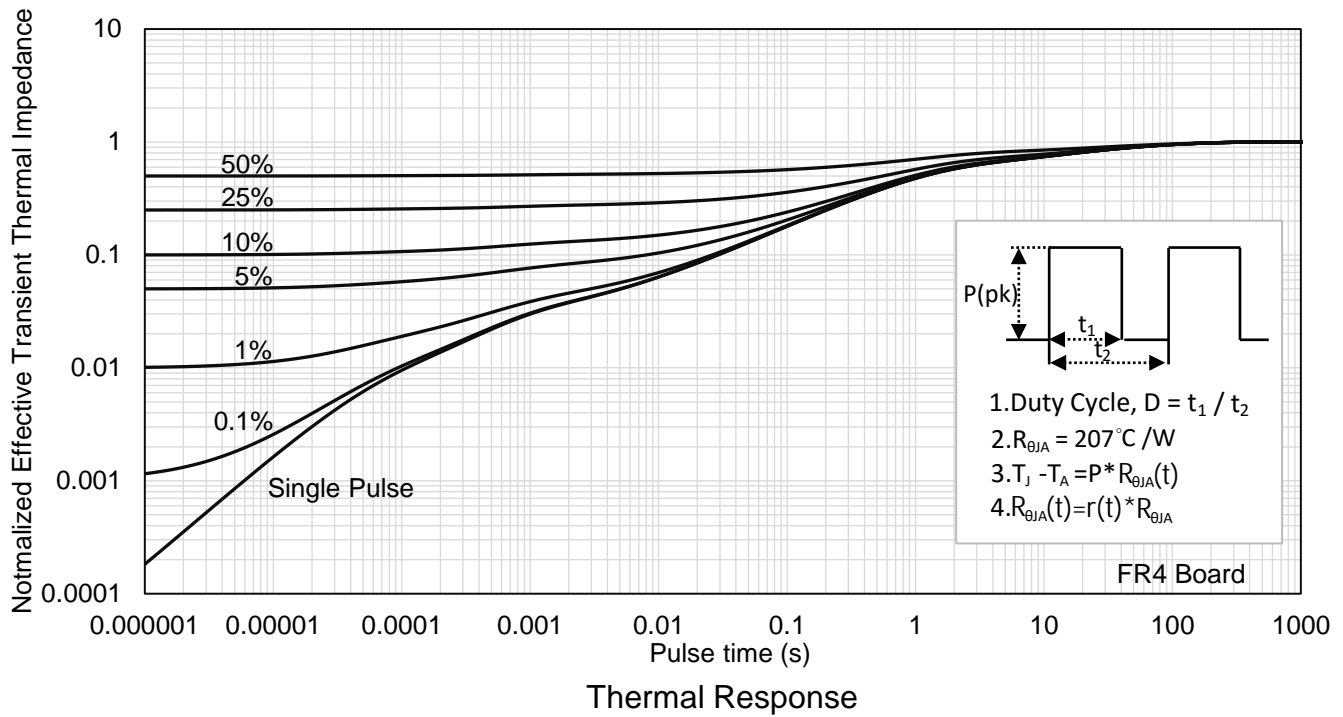
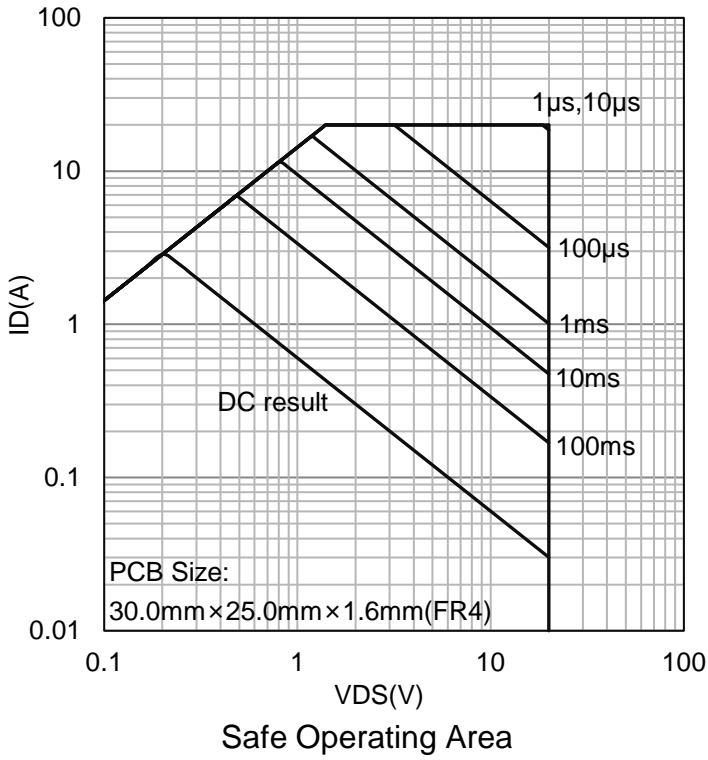
### 7. ELECTRICAL CHARACTERISTICS CURVES



### 7. ELECTRICAL CHARACTERISTICS CURVES(Con.)

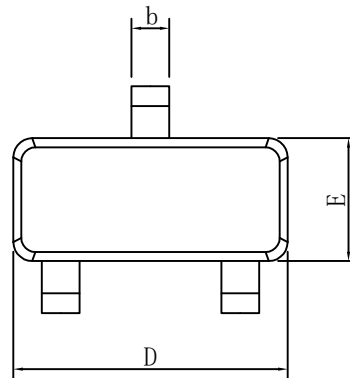
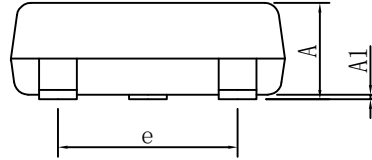
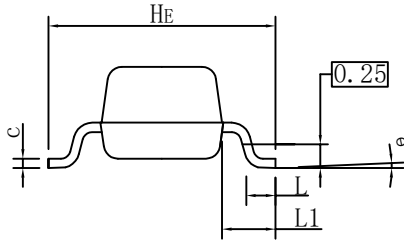


### 7. ELECTRICAL CHARACTERISTICS CURVES(Con.)



## 8. OUTLINE AND DIMENSIONS

### SOT23E

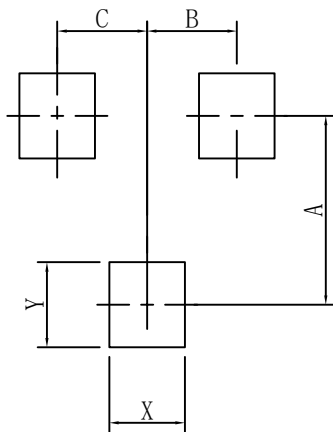


SOT23E			
DIM	MIN	NOR	MAX
A	0.90	1.00	1.10
A1	0.01	0.06	0.10
b	0.30	0.40	0.50
c	0.10	0.17	0.20
D	2.80	2.90	3.00
E	1.20	1.30	1.40
e	1.80	1.90	2.00
L	0.20	0.40	0.60
L1	0.60REF		
HE	2.20	2.40	2.60
θ	0°	-	10°
All Dimensions in mm			

#### GENERAL NOTES

1. Top package surface finish Ra0.4±0.2um
2. Bottom package surface finish Ra0.7±0.2um
3. Side package surface finish Ra0.4±0.2um

## 9. SOLDERING FOOTPRINT



SOT23E	
DIM	(mm)
X	0.80
Y	0.90
A	2.00
B	0.95
C	0.95

## **DISCLAIMER**

- Curve guarantee in the specification. The curve of test items with electric parameter is used as quality guarantee. The curve of test items without electric parameter is used as reference only.
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