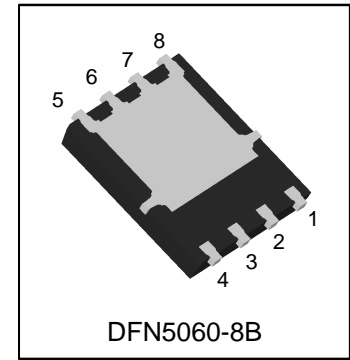


LN7406DT1WG

N-Channel 40-V (D-S) MOSFET

1. FEATURES

- Low RDS(on) trench technology.
- Low thermal impedance.
- Fast switching speed.
- We declare that the material of product are Halogen Free and compliance with RoHS requirements.

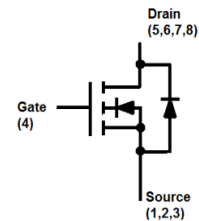


2. APPLICATION

- White LED boost converters
- DC/DC Conversion Circuits
- Motor Drives

3. ORDERING INFORMATION

Device	Marking	Shipping
LN7406DT1WG	LN7406	3000/Tape&Reel



4. MAXIMUM RATINGS(Ta = 25°C unless otherwise stated)

Parameter	Symbol	Limits	Unit
Drain-to-Source Voltage	VDSS	40	V
Gate-to-Source Voltage	VGS	±20	V
Continuous Drain Current(Note 1)	ID	TA =25°C	18
		TA =70°C	16
Pulsed Drain Current (Note 2)	IDM	72	A
Continuous Source Current (Diode Conduction)(Note 1)	IS	18	A
Continuous Drain Current(Note 1)	ID	TC =25°C	72
		TC =70°C	57
Pulsed Drain Current (Note 2)	IDM	288	A
Avalanche Current (L = 0.1mH)	IAS	34	A
Avalanche Energy (L = 0.1mH)	EAS	57.8	mJ
Power Dissipation(Note 1)	PD	TA =25°C	2.5
		TA =70°C	1.9
		TC =25°C	62.5
		TC =70°C	40
Operating Junction Temperature	TJ	-55 ~+150	°C
Storage Temperature Range	Tstg	-55 ~+150	

5. THERMAL CHARACTERISTICS

Parameter	Symbol	Max	Unit
Thermal Resistance, Junction-to-Ambient (Note 1)	RθJA	50	°C/W
Thermal Resistance, Junction-to-Case	RθJC	2	

- 1.Surface mounted on "1.5 x 1.5" FR4 board using 1 sq in pad, 2 oz Cu.
- 2.Pulse width limited by maximum junction temperature

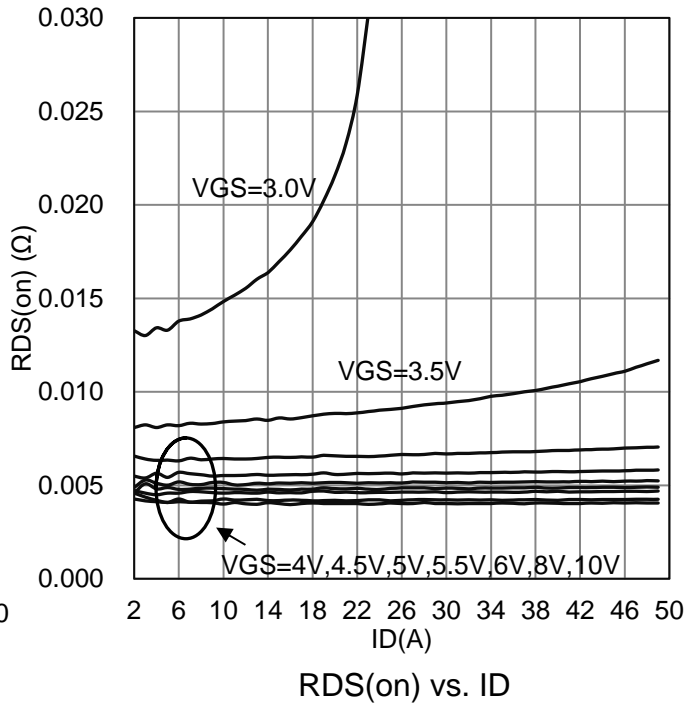
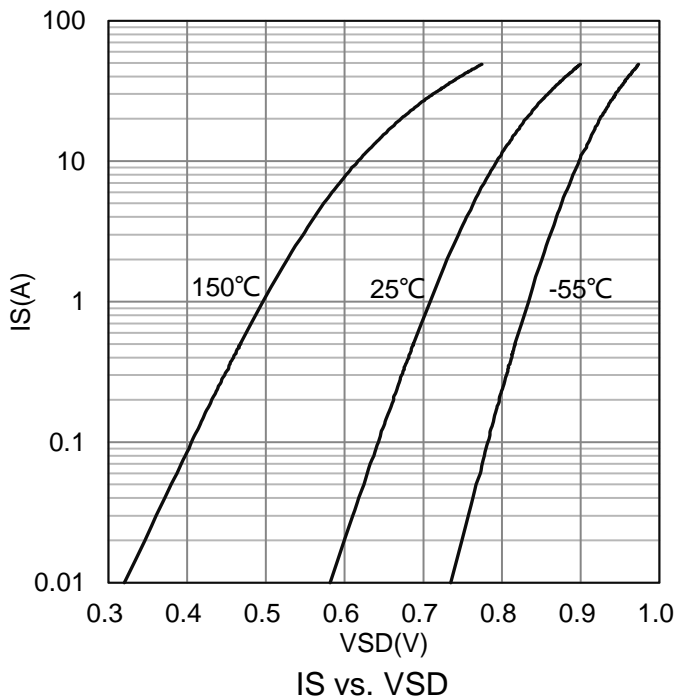
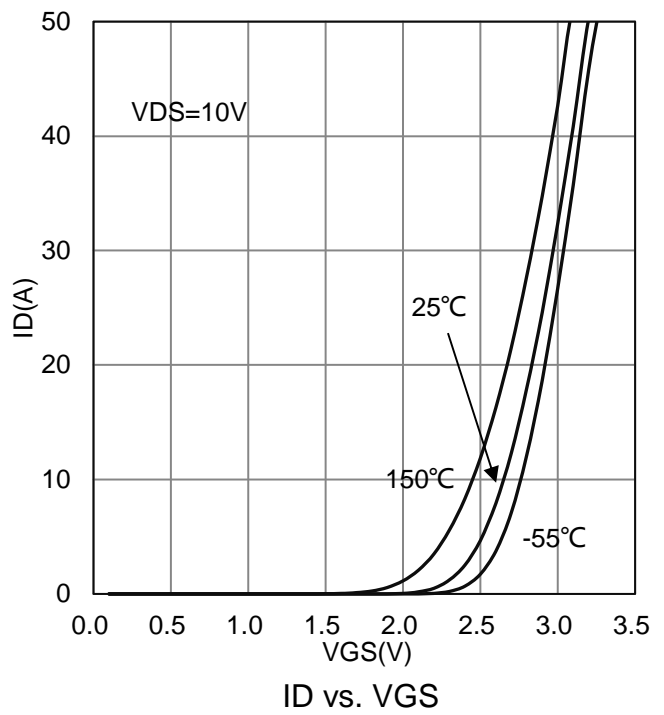
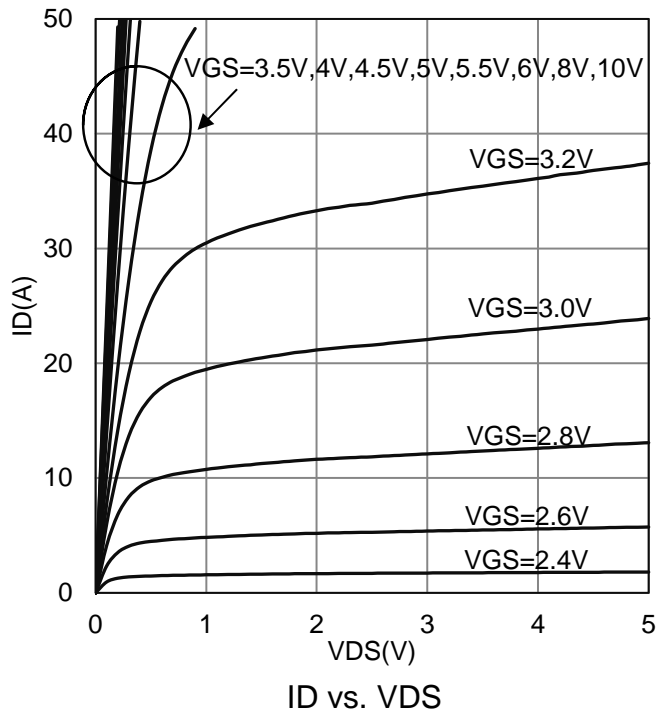
6. ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Static					
Drain-Source Breakdown Voltage (VGS = 0 V, ID = 250 μ A)	V(BR)DSS	40	-	-	V
Gate-Source Threshold Voltage (VDS = VGS, ID = 250 μ A)	VGS(th)	1	-	2.5	V
Gate-Body Leakage (VDS = 0 V, VGS = \pm 20 V)	IGSS	-	-	\pm 10	μ A
Zero Gate Voltage Drain Current (VDS = 32 V, VGS = 0 V) (VDS = 32 V, VGS = 0 V, TJ = 55°C)	IDSS	-	-	1 25	μ A
Drain-Source On-Resistance(Note 3) (VGS = 10 V, ID = 11 A) (VGS = 4.5 V, ID = 8.8 A)	RDS(on)	-	-	6.5 9	m Ω
Diode Forward Voltage(Note 3) (IS = 2.3 A, VGS = 0 V)	VSD	-	0.74	1.2	V
Dynamic(Note 4)					
Total Gate Charge	(VDS = 20 V, VGS = 4.5 V, ID = 11 A)	Qg	-	33.8	-
Gate-Source Charge		Qgs	-	11	-
Gate-Drain Charge		Qgd	-	11.2	-
Input Capacitance	(VDS = 15 V, VGS = 0 V, f = 1 MHz)	Ciss	-	4146	-
Output Capacitance		Coss	-	322	-
Reverse Transfer Capacitance		Crss	-	272	-
Turn-On Delay Time	(VDS = 20 V, RL = 1.9 Ω , ID = 11 A, VGEN = 10 V, RGEN = 6 Ω)	td(on)	-	22	-
Rise Time		tr	-	36	-
Turn-Off Delay Time		td(off)	-	210	-
Fall Time		tf	-	86	-

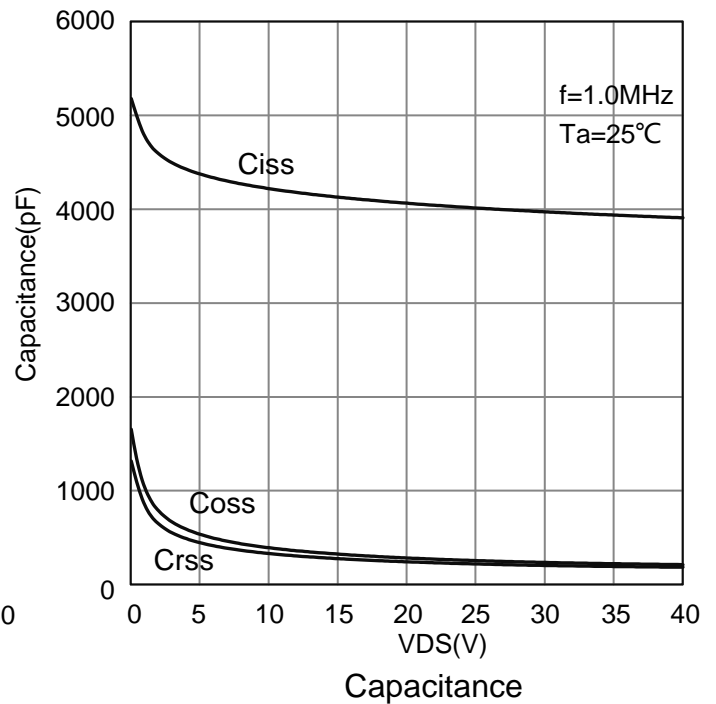
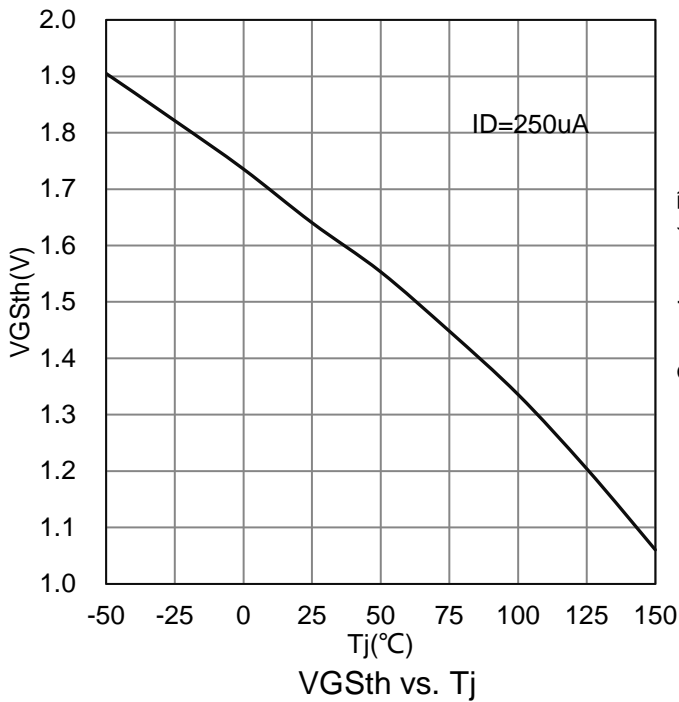
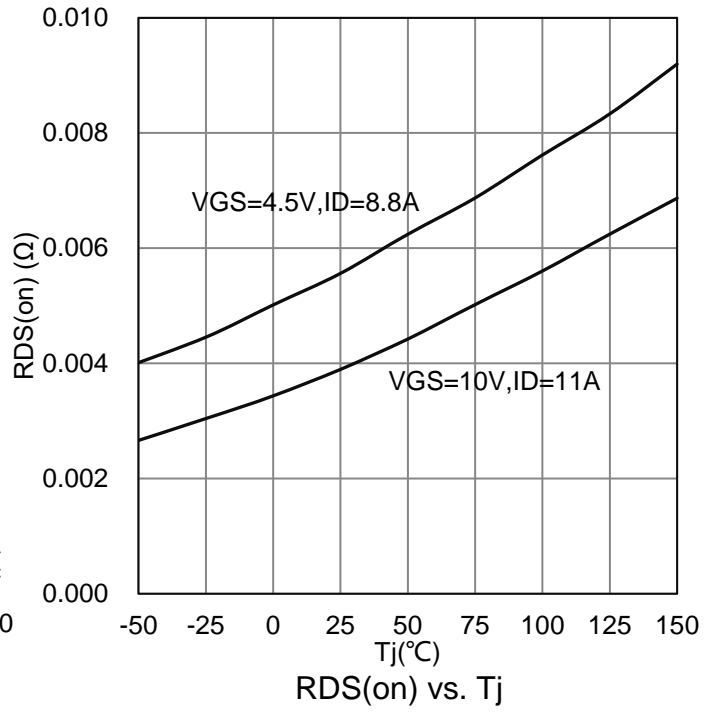
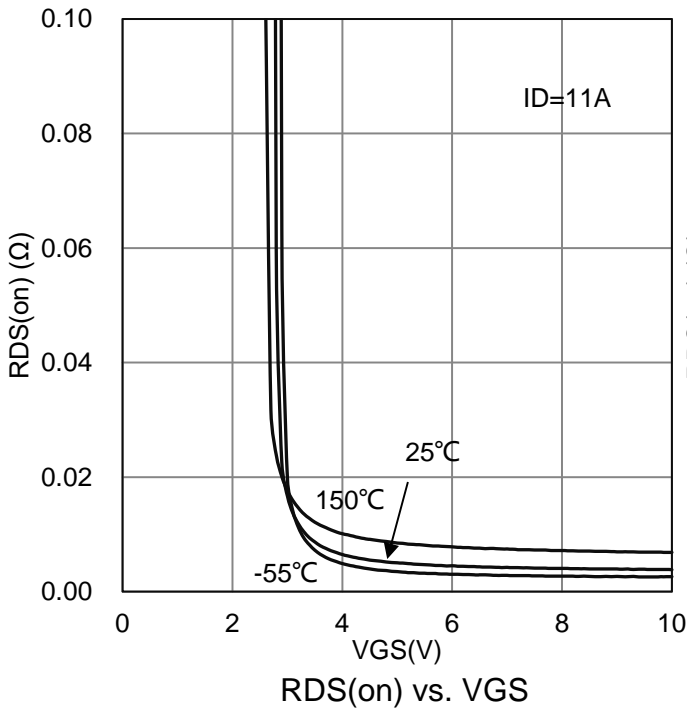
3. Pulse test: PW \leq 300 μ s duty cycle \leq 2%.

4. Guaranteed by design, not subject to production testing.

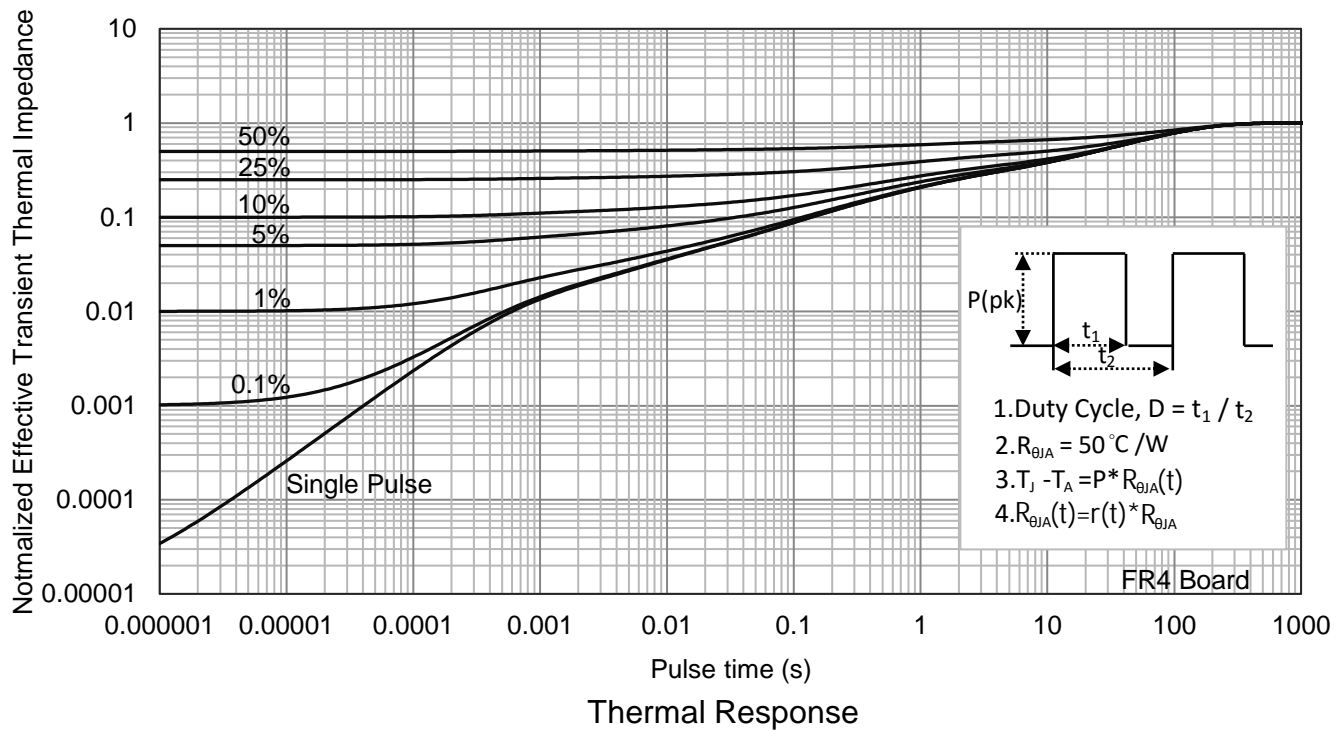
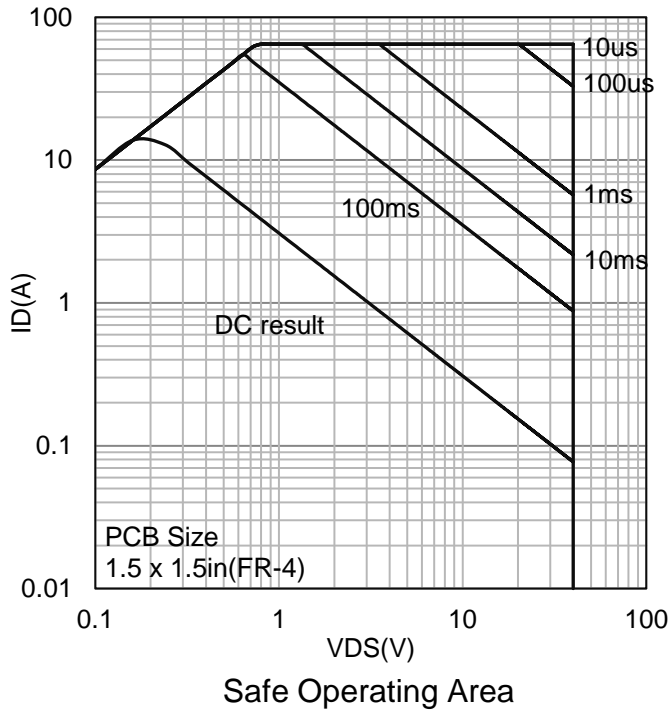
7. ELECTRICAL CHARACTERISTICS CURVES



7. ELECTRICAL CHARACTERISTICS CURVES(Con.)

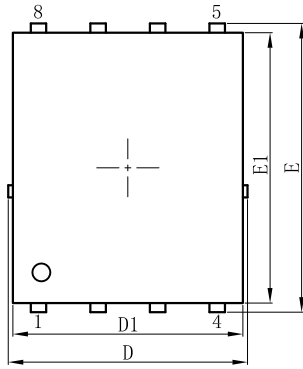


7. ELECTRICAL CHARACTERISTICS CURVES(Con.)

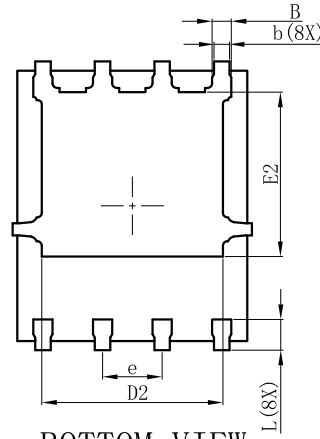


8. OUTLINE AND DIMENSIONS

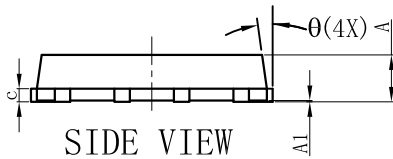
DFN5060-8B



TOP VIEW



BOTTOM VIEW



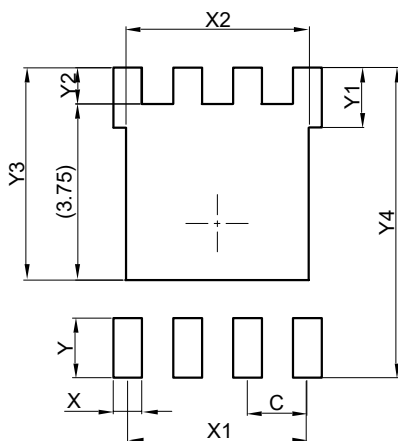
SIDE VIEW

DFN5060-8B			
DIM	MIN	NOR	MAX
A	0.90	1.00	1.10
A1	0.00	0.02	0.05
E	6.00	6.15	6.30
E1	5.66	5.76	5.86
E2	3.40	3.50	3.60
D	4.95	5.10	5.25
D1	4.80	4.90	5.00
D2	3.76	3.86	3.96
b	0.30	0.35	0.40
B	0.36	0.41	0.46
L	0.56	0.66	0.76
e	1.27BSC		
c	0.254REF.		
θ	0°	-	12°
All Dimensions in mm			

GENERAL NOTES

1. Top package surface finish Ra0.4±0.2um
2. Bottom package surface finish Ra0.7±0.2um
3. Side package surface finish Ra0.4±0.2um
4. Protrusion or Gate Burrs shall not exceed 0.05mm per side.
5. Offcenter Max0.038mm; Mismatch Max 0.038mm.

9. SOLDERING FOOTPRINT



DFN5060-8B	
DIM	(mm)
C	1.27
X	0.61
X1	3.81
X2	3.91
Y	1.27
Y1	1.27
Y2	0.77
Y3	4.52
Y4	6.61

DISCLAIMER

- Curve guarantee in the specification. The curve of test items with electric parameter is used as quality guarantee. The curve of test items without electric parameter is used as reference only.
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