

Bias Resistor Transistor

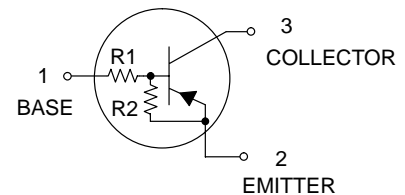
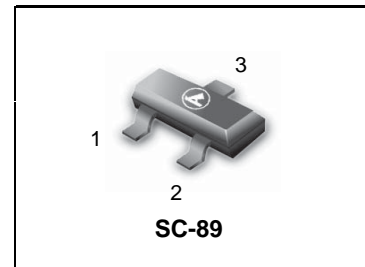
PNP Silicon Surface Mount Transistor with Monolithic Bias Resistor Network

LDTA113ZET1G

- **Applications**
Inverter, Interface, Driver

- **Features**
 - 1) Built-in bias resistors enable the configuration of an inverter circuit without connecting external input resistors (see equivalent circuit).
 - 2) The bias resistors consist of thin-film resistors with complete isolation to allow positive biasing of the input. They also have the advantage of almost completely eliminating parasitic effects.
 - 3) Only the on/off conditions need to be set for operation, making the device design easy.

- We declare that the material of product compliance with RoHS requirements.



● **Absolute maximum ratings** (Ta=25°C)

Parameter	Symbol	Limits	Unit
Supply voltage	V _{CC}	-50	V
Input voltage	V _{IN}	-10 to +5	V
Output current	I _o	-100	mA
	I _{C(Max.)}	-100	
Power dissipation	P _D	200	mW
Junction temperature	T _j	150	°C
Storage temperature	T _{stg}	-55 to +150	°C

DEVICE MARKING AND RESISTOR VALUES

Device	Marking	R1 (K)	R2 (K)	Shipping
LDTA113ZET1G	E8	1	10	3000/Tape & Reel
LDTA113ZET3G	E8	1	10	10000/Tape & Reel

● **Electrical characteristics** (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Input voltage	V _{I(off)}	—	—	-0.3	V	V _{CC} =-5V, I _o =-100 μA
	V _{I(on)}	-3	—	—		V _o =-0.3V, I _o =-20mA
Output voltage	V _{O(on)}	—	—	-0.3	V	I _o /I _i =-10mA/-0.5mA
Input current	I _i	—	—	-7.2	mA	V _i =-5V
Output current	I _{O(off)}	—	—	-0.5	μA	V _{CC} =-50V, V _i =0V
DC current gain	G _i	33	—	—	—	V _o =-5V, I _o =-5mA
Input resistance	R ₁	0.7	1	1.3	kΩ	—
Resistance ratio	R ₂ /R ₁	8	10	12	—	—
Transition frequency	f _r	—	250	—	MHz	V _{CE} =-10V, I _E =5mA, f=100MHz *

* Transition frequency of the device

●Electrical characteristic curves

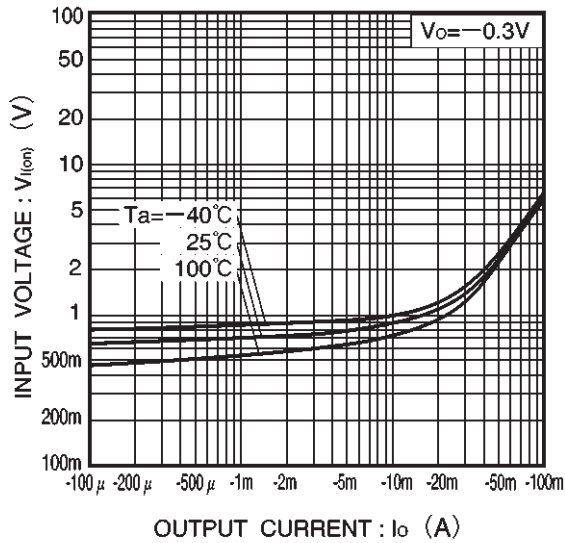


Fig.1 Input voltage vs. output current (ON characteristics)

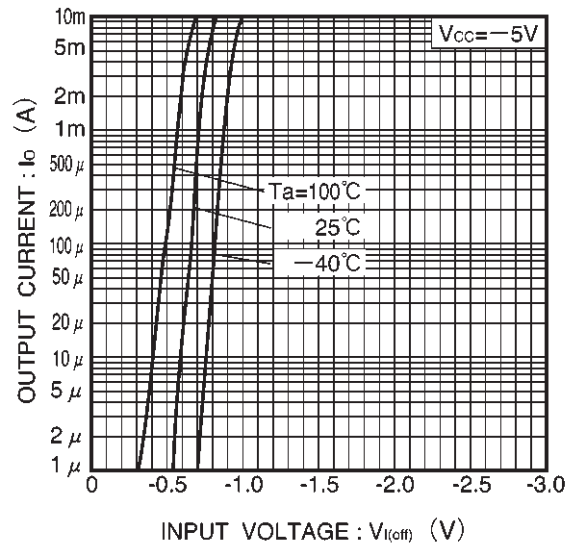


Fig.2 Output current vs. input voltage (OFF characteristics)

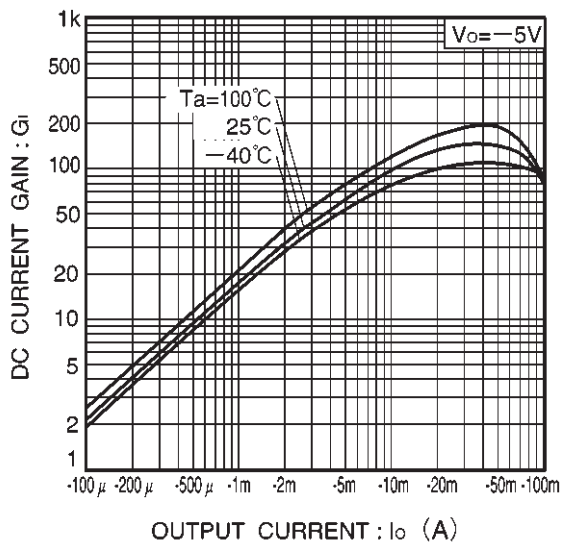


Fig.3 DC current gain vs. output current

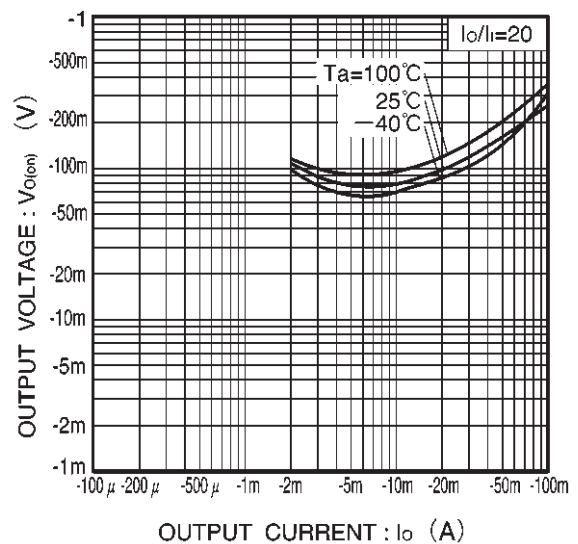
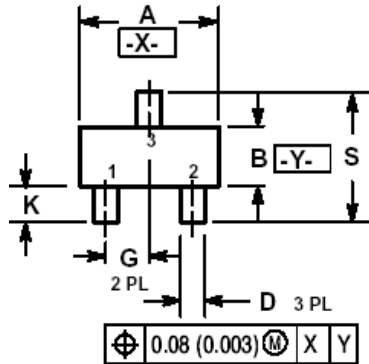


Fig.4 Output voltage vs. output current

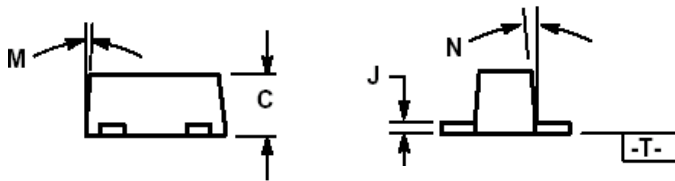
LDTA113ZET1G

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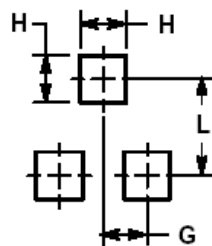


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. 463C-01 OBSOLETE, NEW STANDARD 463C-02.



DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.50	1.60	1.70	0.059	0.063	0.067
B	0.75	0.85	0.95	0.030	0.034	0.040
C	0.60	0.70	0.80	0.024	0.028	0.031
D	0.23	0.28	0.33	0.009	0.011	0.013
G	0.50 BSC			0.020 BSC		
H	0.53 REF			0.021 REF		
J	0.10	0.15	0.20	0.004	0.006	0.008
K	0.30	0.40	0.50	0.012	0.016	0.020
L	1.10 REF			0.043 REF		
M	---	---	10 °	---	---	10 °
N	---	---	10 °	---	---	10 °
S	1.50	1.60	1.70	0.059	0.063	0.067



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[>>LRC\(乐山无线电\)](#)