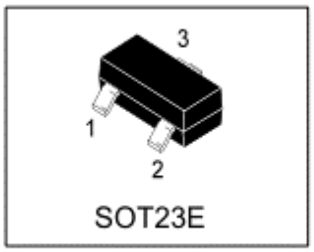
LN2292LT1G

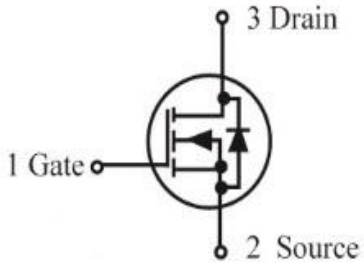
100V N-Channel Enhancement-Mode MOSFET

1. FEATURES



- VDS= 100V
- RDS(ON)≤200 mΩ@VGS =10V,ID =3A
- RDS(ON)≤260 mΩ@VGS =4.5V,ID =1A
- Super high density cell design for extremely low RDS(ON).
- Exceptional on-resistance and maximum DC current capability.
- We declare that the material of product compliance with RoHS requirements and Halogen Free.

2. APPLICATIONS



- Power Management in Note book
- DC/DC Converter
- Load Switch

3. DEVICE MARKING AND ORDERING INFORMATION

Device	Marking	Shipping
LN2292LT1G	N2L	3000/Tape&Reel

4. MAXIMUM RATINGS(Ta = 25ºC)

Parameter	Symbol	Limits	Unit
Drain–Source Voltage	VDSS	100	V
Gate–to–Source Voltage – Continuous	VGS	±20	V
Drain Current – Continuous TA = 25°C – Pulsed	 ID IDM	 3 10	A

5. THERMAL CHARACTERISTICS

Parameter	Symbol	Limits	Unit
Maximum Power Dissipation	PD	1.25	W
Thermal Resistance, Junction–to–Ambient	RΘJA	100	ºC/W
Junction and Storage temperature	TJ,Tstg	−55~+150	°C

6. ELECTRICAL CHARACTERISTICS (Ta= 25°C)

STATIC

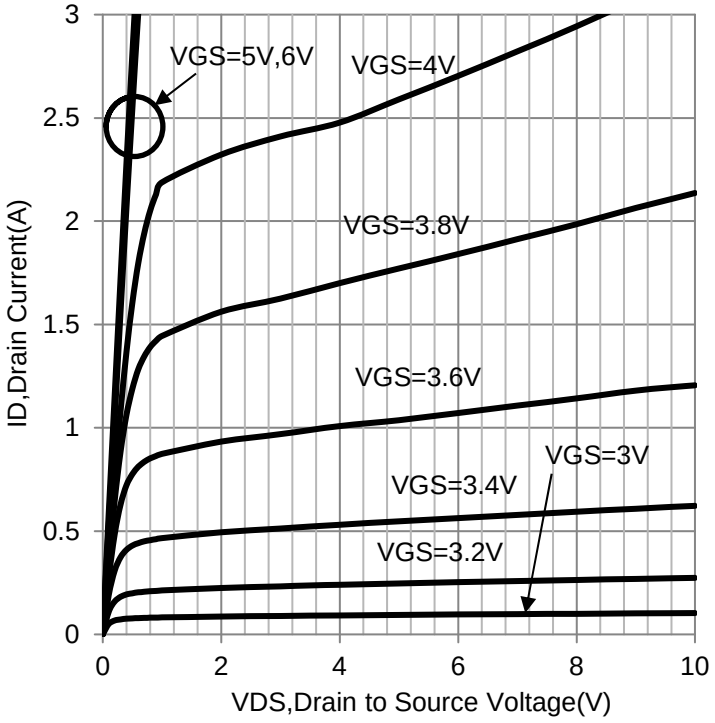
Characteristic	Symbol	Min.	Typ.	Max.	Unit
Drain–Source Breakdown Voltage (VGS = 0V, ID = 250μA)	V(BR)DSS	100	-	-	V
Gate Threshold Voltage (VDS = VGS, ID = 250μA)	VGS(th)	1.0	-	3.0	V
Gate–Body Leakage (VDS = 0 V, VGS =±20 V)	IGSS	-	-	±100	nA
Zero Gate Voltage Drain Current (VDS=100 V, VGS=0 V)	IDSS	-	-	1	μA
Static Drain–Source On–State Resistance (VGS = 10 V, ID = 3 A) (VGS = 4.5 V, ID = 1 A)	RDS(on)	- -	160 200	200 260	mΩ
Forward Voltage (VGS = 0 V, IS = 6.5 A)	VSD	-	0.9	1.3	V

DYNAMIC

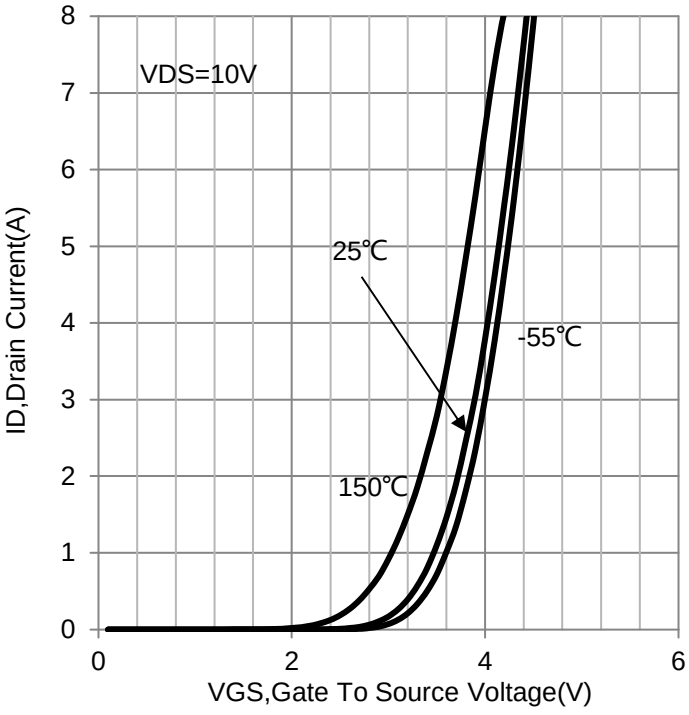
Total Gate Charge	(VDS =50V, VGS =5V, ID =6.5A)	Qg	-	8.2	-	nC
Gate-Source Charge		Qgs	-	4.3	-	
Gate-Drain Charge		Qgd	-	5.3	-	
Input Capacitance	(VDS =25V, VGS =0V, f=1MHz)	Ciss	-	396	-	pF
Output Capacitance		Coss	-	47	-	
Reverse Transfer Capacitance		Crss	-	30	-	
Turn-On Delay Time	(VDD =50V, RL =50Ω，VGEN =10V, RG =2.5Ω)	td(on)	-	9.6	-	ns
Rise Time		tr	-	4.2	-	
Turn-Off Delay Time		td(off)	-	25	-	
Fall Time		tf	-	3.2	-	

Note 1:Pulse Test: Pulse Width ≤300 μs, Duty Cycle ≤2.0%.

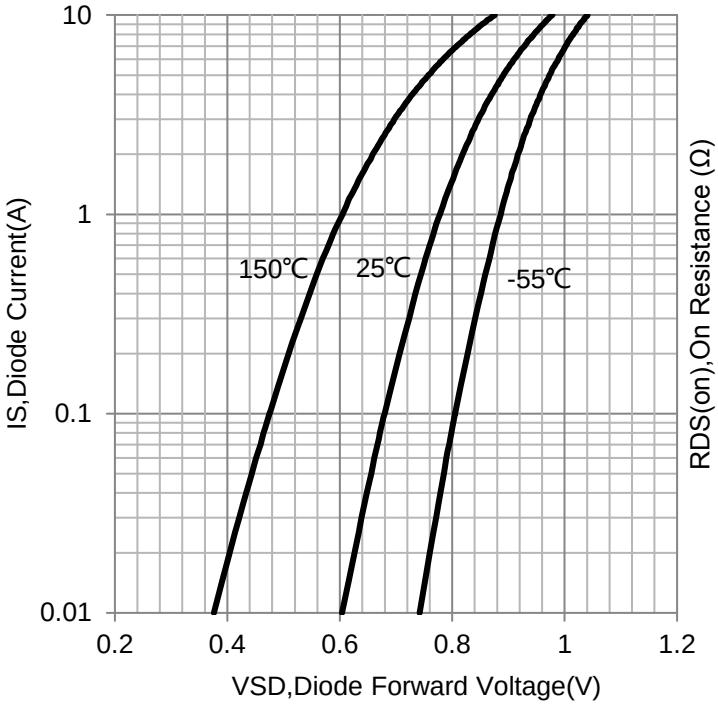
7.ELECTRICAL CHARACTERISTICS CURVES



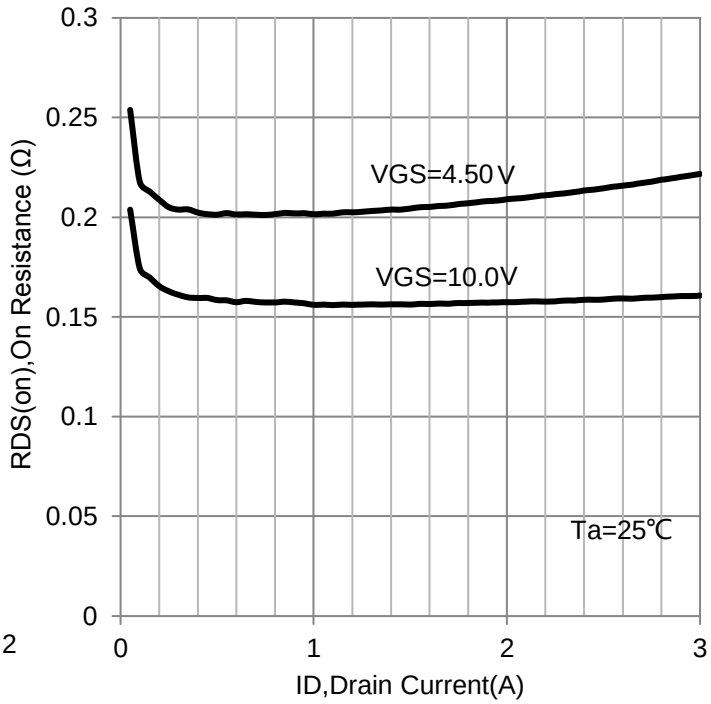
ID vs. VDS



ID vs. VGS

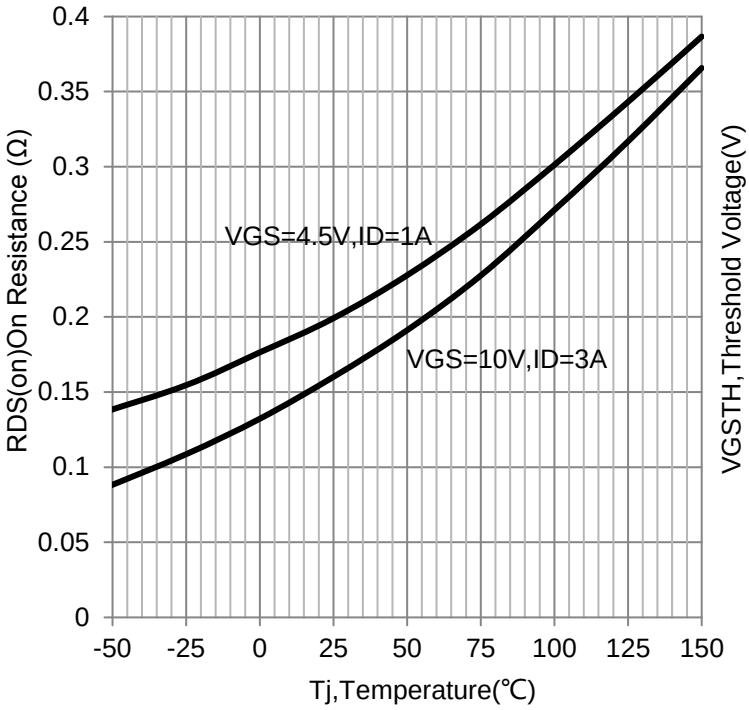


IS vs. VSD

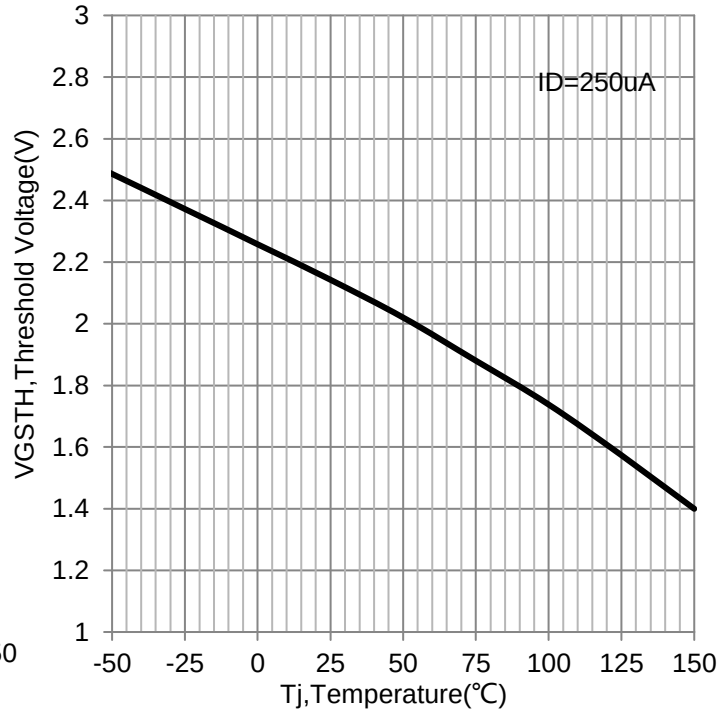


RDS(on) vs. ID

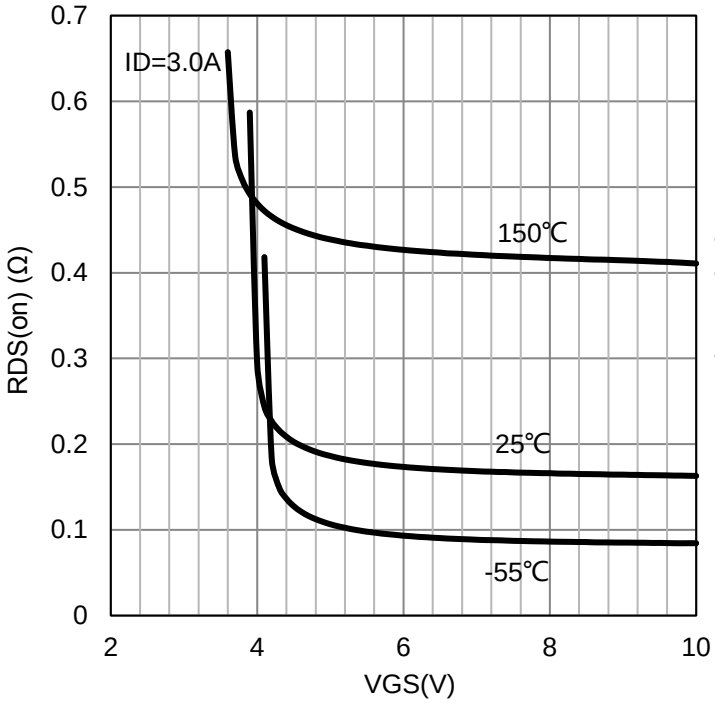
7.ELECTRICAL CHARACTERISTICS CURVES(Con.)



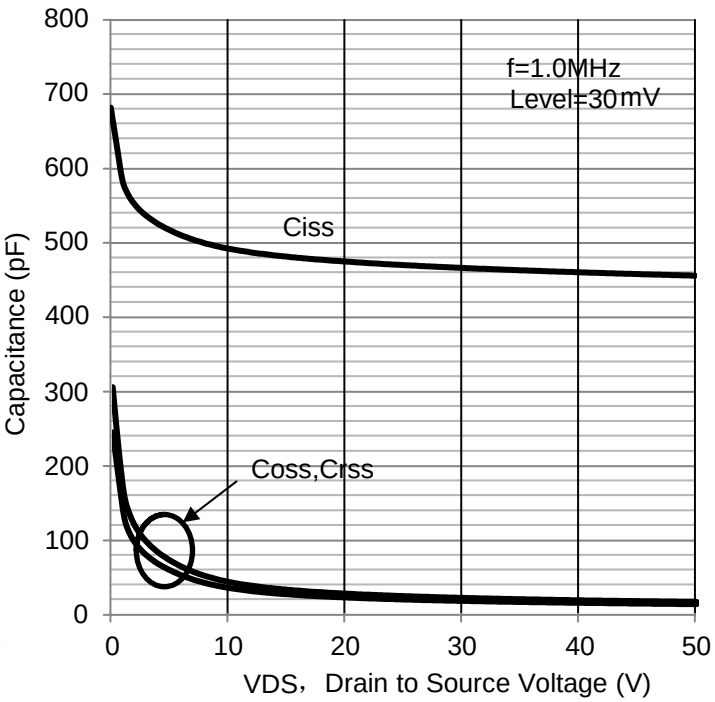
RDS(on) vs. Tj



VGSTH vs. Tj



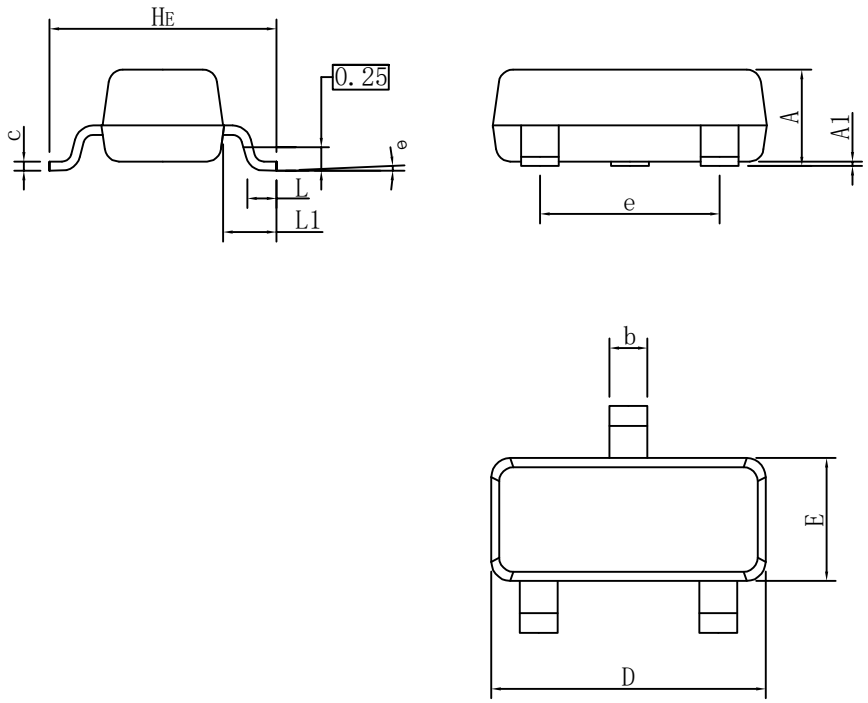
RDSON vs. VGS



Capacitance

8.OUTLINE AND DIMENSIONS

SOT23E

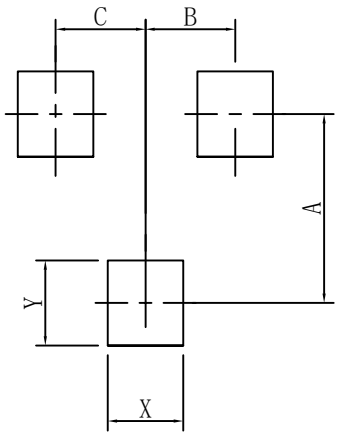


SOT23E			
DIM	MIN	NOR	MAX
A	0.90	1.00	1.10
A1	0.01	0.06	0.10
b	0.30	0.40	0.50
c	0.10	0.17	0.20
D	2.80	2.90	3.00
E	1.20	1.30	1.40
e	1.80	1.90	2.00
L	0.20	0.40	0.60
L1	0.60REF		
HE	2.20	2.40	2.60
θ	0°	-	10°
All Dimensions in mm			

GENERAL NOTES

1. Top package surface finish Ra0.4±0.2um
2. Bottom package surface finish Ra0.7±0.2um
3. Side package surface finish Ra0.4±0.2um

9.SOLDERING FOOTPRINT



SOT23E	
DIM	(mm)
X	0.80
Y	0.90
A	2.00
B	0.95
C	0.95