MMP80R900PC

800V 0.9Ω N-channel MOSFET

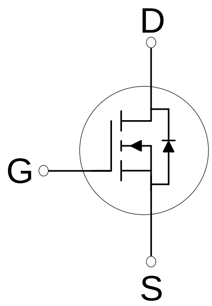
■ Description

MMP80R900PC is power MOSFET using Magnachip's advanced super junction technology that can realize very low on-resistance and gate charge. It will provide much high efficiency by using optimized charge coupling technology. These user friendly devices give an advantage of Low EMI to designers as well as low switching loss.

■ Key Parameters

Parameter	Value	Unit
V_{DS} @ $T_{j,max}$	850	V
$R_{DS(on),max}$	0.9	Ω
$V_{TH,typ}$	3	V
I_D	6	A
$Q_{g,typ}$	17.6	nC

■ Package & Internal Circuit



RoHS Compliant
HALOGEN-FREE

■ Features

- Low Power Loss by High Speed Switching and Low On-Resistance
- 100% Avalanche Tested
- Green Package – Pb Free Plating, Halogen Free

■ Applications

- PFC Power Supply Stages
- Switching Applications
- Adapter

■ Ordering Information

Order Code	Marking	Temp. Range	Package	Packing	RoHS Status
MMP80R900PCTH	80R900PC	-55 ~ 150℃	TO-220	Tube	Halogen Free

■ Absolute Maximum Rating (Tc=25℃ unless otherwise specified)

Parameter	Symbol	Rating	Unit	Note
Drain – Source voltage	V_{DSS}	800	V	
Gate – Source voltage	V_{GSS}	±30	V	
Continuous drain current	I_D	6.0	A	T_C=25℃
		3.8	A	T_C=100℃
Pulsed drain current(1)	I_{DM}	18	A	
Power dissipation	P_D	75.8	W	
Single - pulse avalanche energy	E_{AS}	230	mJ	L=79mH, V_{DD}=50V
MOSFET dv/dt ruggedness	dv/dt	50	V/ns	
Diode dv/dt ruggedness(2)	dv/dt	15	V/ns	
Storage temperature	T_{stg}	-55 ~150	℃	
Maximum operating junction temperature	T_j	150	℃	

1) Pulse width t_P limited by $T_{j,max}$
2) $I_{SD} \leq I_D$, $V_{DS\ peak} \leq V_{(BR)DSS}$

■ Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal resistance, junction-case max	R_{thjc}	1.65	℃/W
Thermal resistance, junction-ambient max	R_{thja}	62.5	℃/W

■ Static Characteristics (T_c=25℃ unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Drain – Source Breakdown voltage	$V_{(BR)DSS}$	800	-	-	V	V_{GS} = 0V, I_D = 0.25mA
Gate Threshold Voltage	$V_{GS(th)}$	2.1	3	3.9	V	V_{DS} = V_{GS}, I_D = 0.25mA
Zero Gate Voltage Drain Current	I_{DSS}	-	-	1	μA	V_{DS} = 800V, V_{GS} = 0V
Gate Leakage Current	I_{GSS}	-	-	100	nA	V_{GS} = ±30V, V_{DS} = 0V
Drain-Source On State Resistance	$R_{DS(ON)}$	-	0.78	0.9	Ω	V_{GS} = 10V, I_D = 3.8A

■ Dynamic Characteristics (T_c=25℃ unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input Capacitance	C_{iss}	-	574	-	pF	V_{DS} = 25V, V_{GS} = 0V, f = 1.0MHz
Output Capacitance	C_{oss}	-	508	-		
Reverse Transfer Capacitance	C_{rss}	-	21	-		
Effective Output Capacitance Energy Related (3)	$C_{o(er)}$	-	16.7	-		V_{DS} = 0V to 640V, V_{GS} = 0V, f = 1.0MHz
Turn On Delay Time	$t_{d(on)}$	-	12.8	-	ns	V_{GS} = 10V, R_G = 25Ω, V_{DS} = 400V, I_D = 6A
Rise Time	t_r	-	22.4	-		
Turn Off Delay Time	$t_{d(off)}$	-	54.4	-		
Fall Time	t_f	-	23.6	-		
Total Gate Charge	Q_g	-	17.6	-	nC	V_{GS} = 10V, V_{DS} = 640V, I_D = 6A
Gate – Source Charge	Q_{gs}	-	3.9	-		
Gate – Drain Charge	Q_{gd}	-	6.7	-		
Gate Resistance	R_G	-	2.5	-	Ω	V_{GS} = 0V, f = 1.0MHz

3) $C_{o(er)}$ is a capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0V to 80% $V_{(BR)DSS}$

■ Reverse Diode Characteristics (T_c=25℃ unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Continuous Diode Forward Current	I_{SD}	-	-	6.0	A	
Diode Forward Voltage	V_{SD}	-	-	1.4	V	I_{SD} = 6A, V_{GS} = 0V
Reverse Recovery Time	t_{rr}	-	320	-	ns	I_{SD} = 6A di/dt = 100A/μs V_{DD} = 100V
Reverse Recovery Charge	Q_{rr}	-	2.4	-	μC	
Reverse Recovery Current	I_{rrm}	-	14.7	-	A	

Characteristic Graph

Fig.1 On-Region Characteristics.

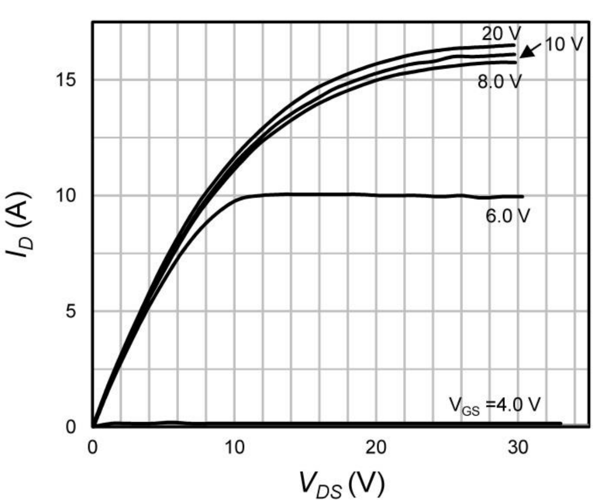


Fig.2 On-Resistance Variation with Drain Current and Gate Voltage

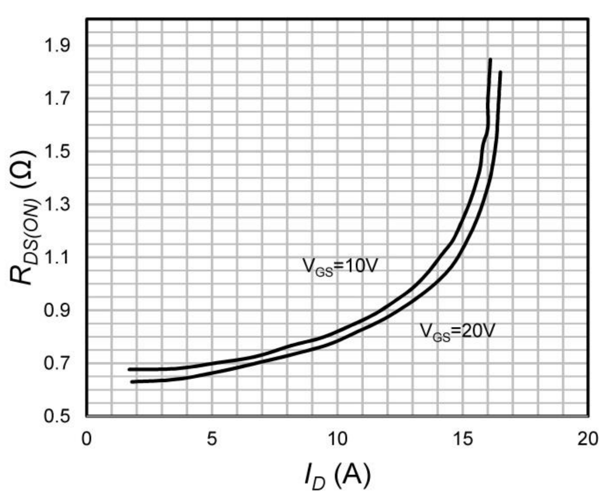


Fig.3 On-Resistance Variation with Temprature (Normalized)

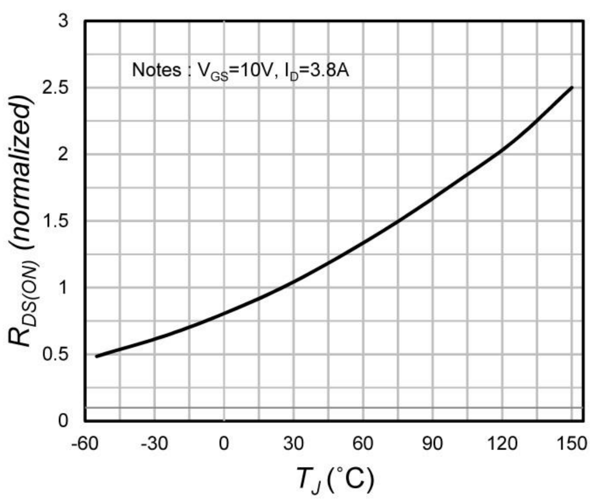


Fig.4 Breakdown Voltage Variation vs. Temperature (Normalized)

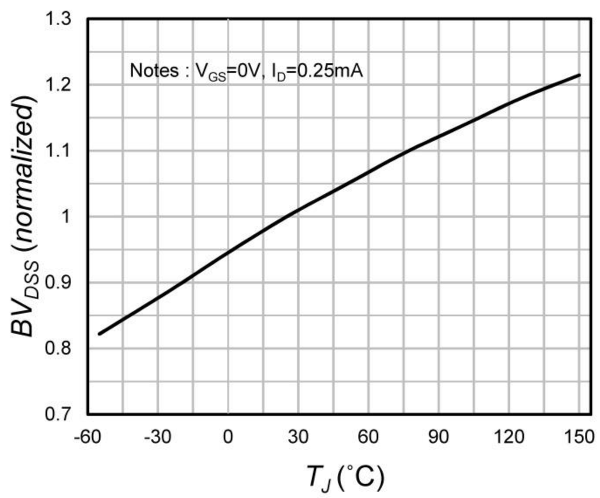


Fig.5 Transfer Characteristics

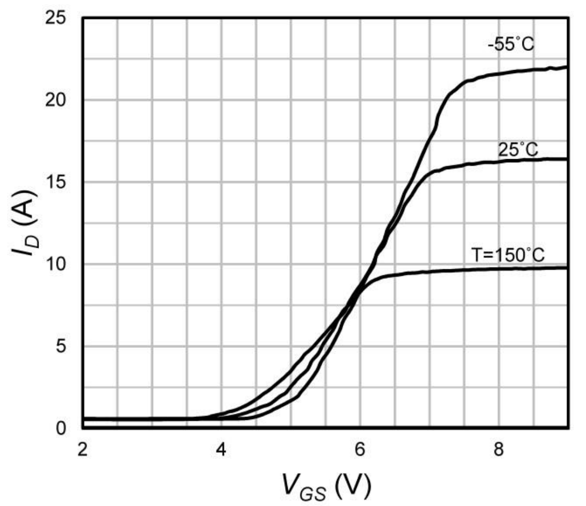


Fig.6 Body Diode Forward Voltage Variation with Source Current and Temperature

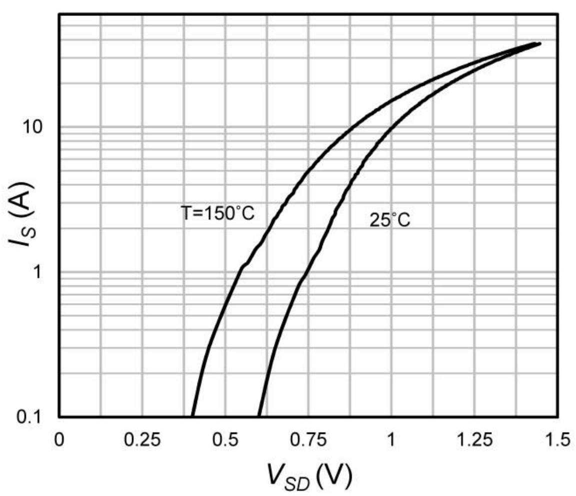


Fig.7 Gate Charge Characteristics

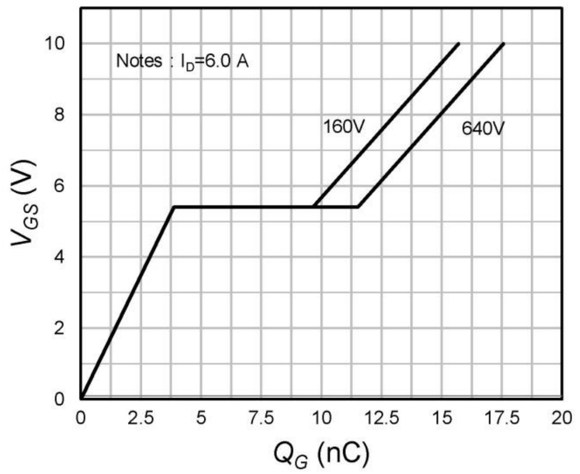


Fig.8 Capacitance Characteristics

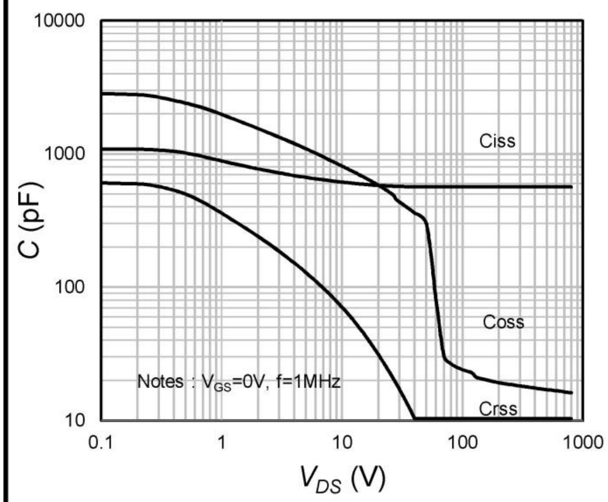


Fig.9 $V_{GS(th)}$ Variation with Temprature (Nomalized)

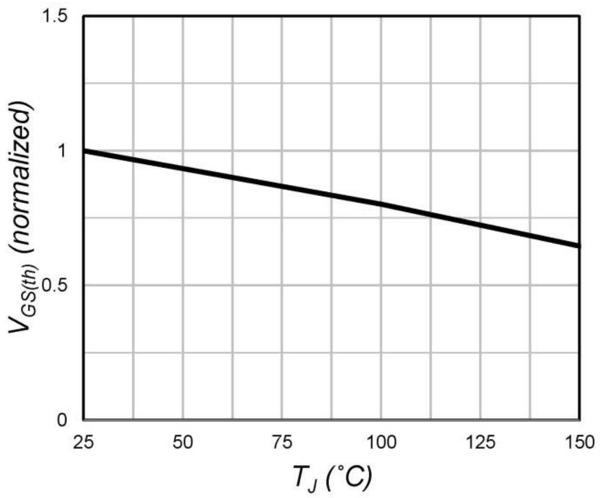


Fig.10 Maximum Drain Current vs. Case Temperature

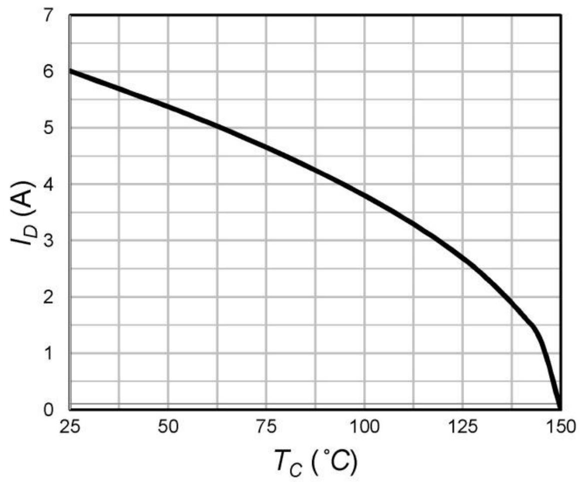


Fig.11 Single Pulse Maximum Power Dissipation

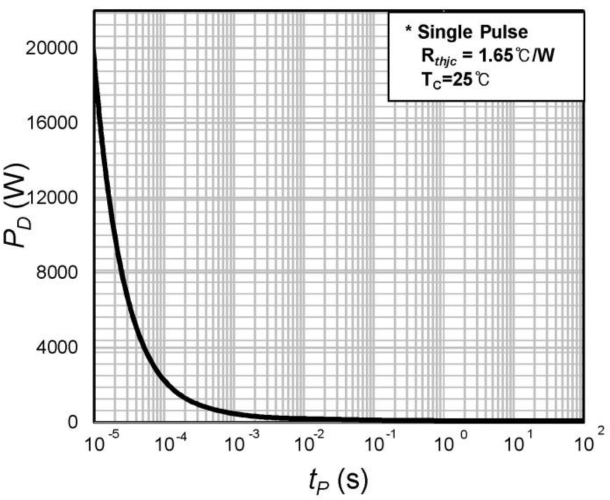


Fig.12 Output Capacitance Stored Energy

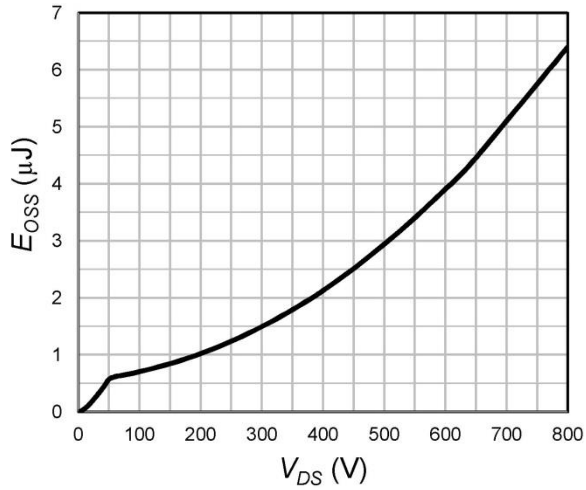


Fig.13 Transient Thermal Response Curve

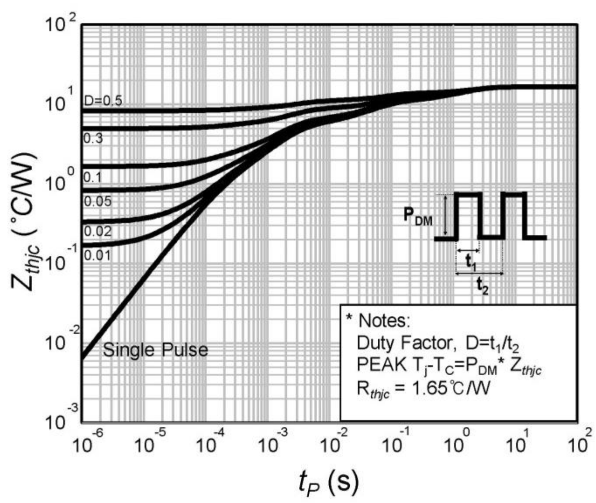
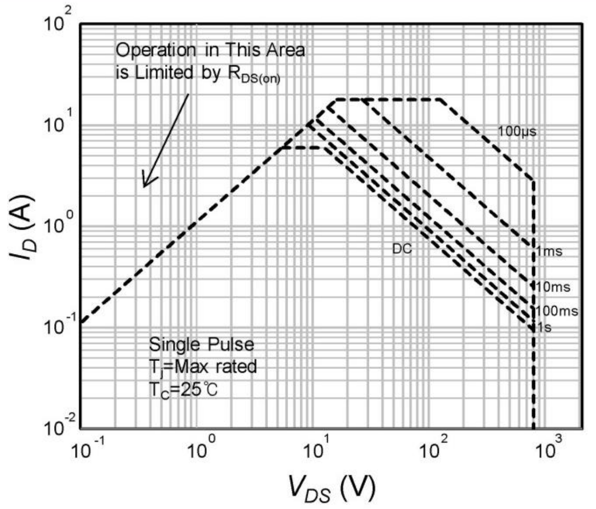


Fig.14 Maximum Safe Operating Area



■ Test Circuit

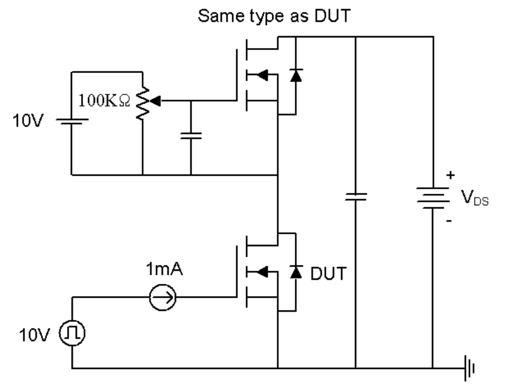


Fig15-1. Gate charge measurement circuit

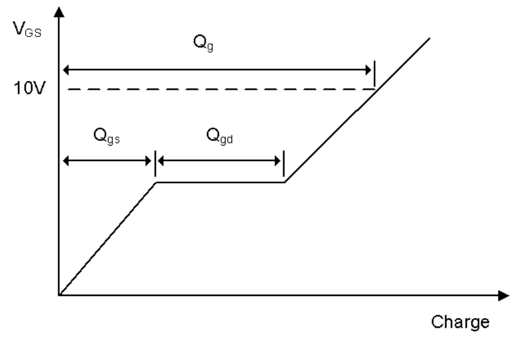


Fig15-2. Gate charge waveform

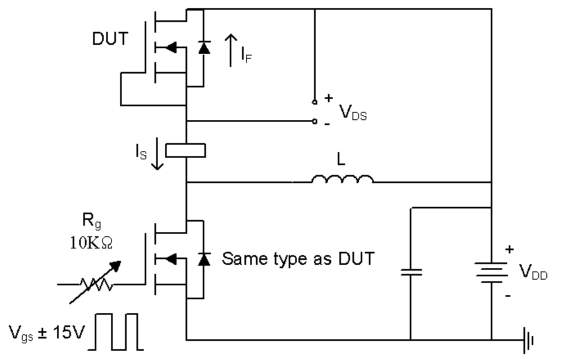


Fig16-1. Diode reverse recovery test circuit

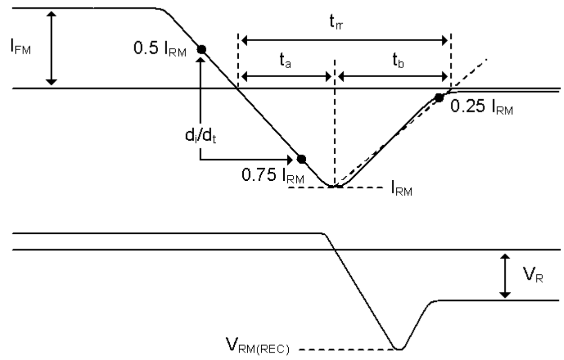


Fig16-2. Diode reverse recovery test waveform

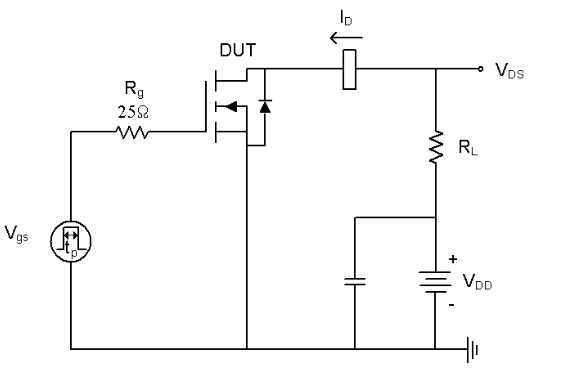


Fig17-1. Switching time test circuit for resistive load

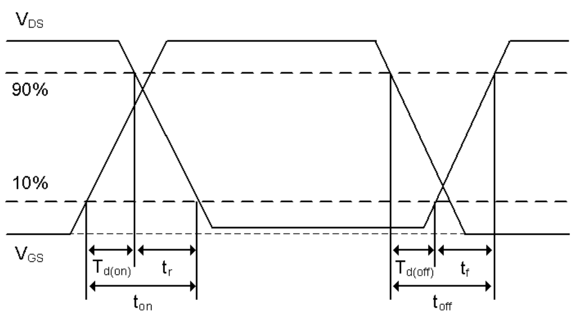


Fig17-2. Switching time waveform

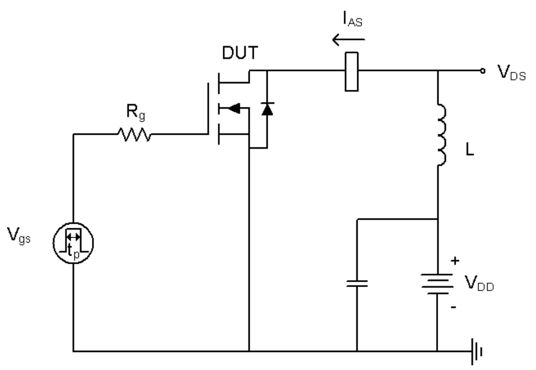


Fig18-1. Unclamped inductive load test circuit

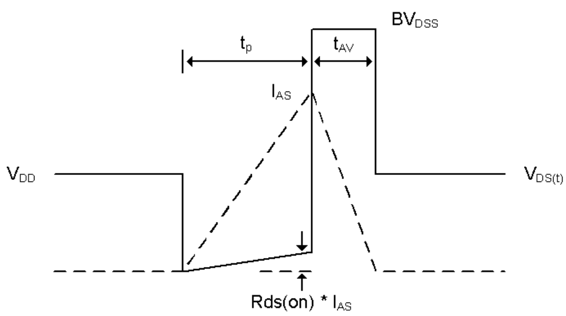
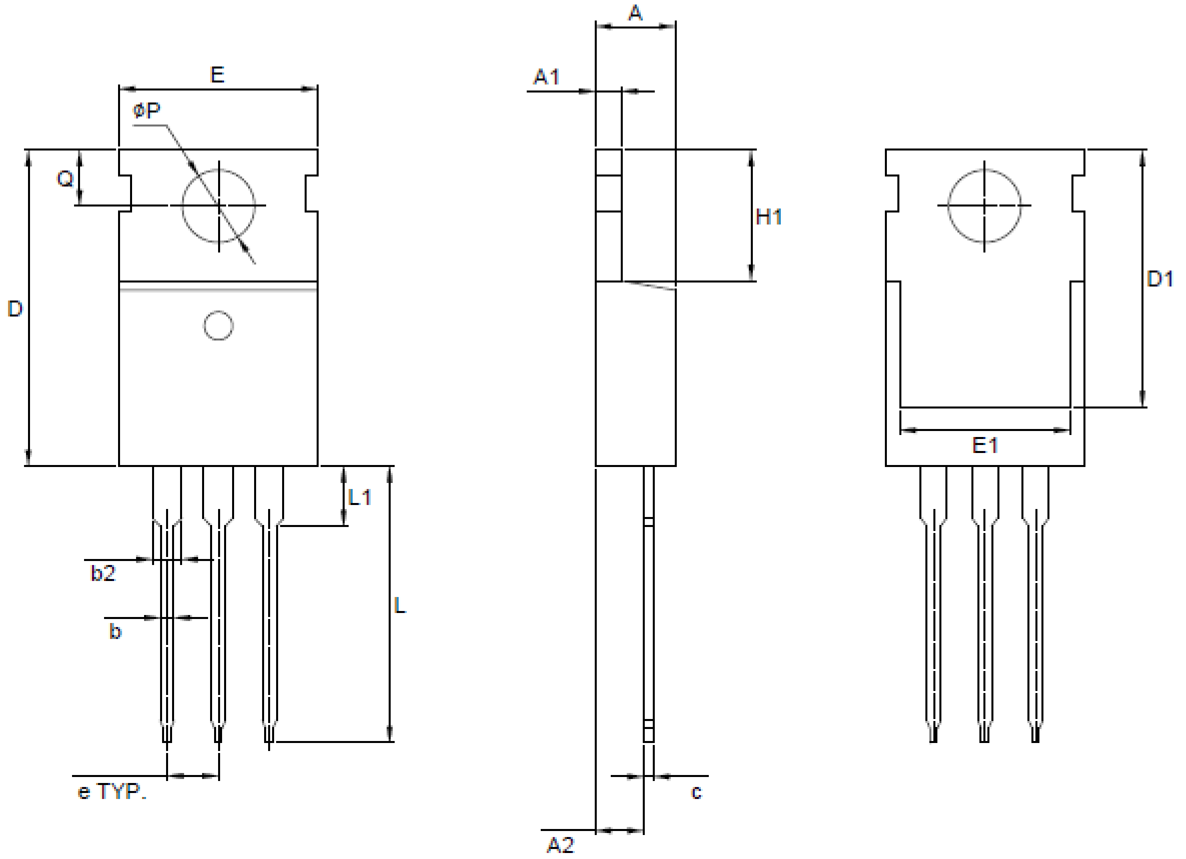


Fig18-2. Unclamped inductive waveform

■ Physical Dimension

TO-220(3L)



Symbol	Dimension (mm)		
	Min	Nom	Max
A	3.56	–	4.83
A1	0.50	–	1.40
A2	2.03	–	2.92
b	0.38	0.69	1.02
b2	1.14	1.45	1.78
c	0.36	–	0.61
D	14.22	–	16.51
D1	12.20	–	13.50
e	2.54 TYP		
E	9.65	–	10.67
E1	–	–	8.90
H1	5.84	–	6.86
L	12.70	–	14.73
L1	–	–	6.35
øP	3.53	–	4.09
Q	2.54	–	3.43

Note : Package body size, length and width do not include mold flash, protrusions and gate burrs.

DISCLAIMER:

The Products are not designed for use in hostile environments, including, without limitation, aircraft, nuclear power generation, medical appliances, and devices or systems in which malfunction of any Product can reasonably be expected to result in a personal injury. Seller's customers using or selling Seller's products for use in such applications do so at their own risk and agree to fully defend and indemnify Seller.

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