



MDP20N116PTTH

Single N-channel Trench MOSFET 200V 11.6mΩ 95A

FEATURES

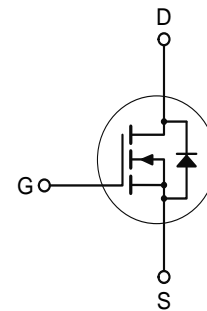
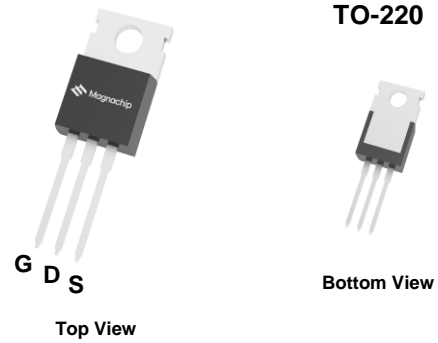
- MV MOSFET GEN3T technology
- N-channel, normal level
- Enhanced avalanche ruggedness
- 100% UIS and Rg tested
- Maximum 175°C junction temperature

APPLICATIONS

- DC/DC and AC/DC converters
- Brushed and BLDC Motor drive systems
- Battery powered systems

KEY PERFORMANCE PARAMETERS

V_{DS}	200	V
$R_{DS(on), typ.}$	0.0106	Ω
I_D	95	A
$Q_G, typ.$	83	nC
Junction temperature, max.	175	$^{\circ}C$



ORDERING INFORMATION

Type / Ordering Code	Package	Marking	Packing	RoHS Status
MDP20N116PTTH	TO-220	MDP20N116	Tube	Halogen Free

<http://www.magnachip.com/>

ABSOLUTE MAXIMUM RATINGS, at $T_J = 25^\circ\text{C}$, unless otherwise specified

PARAMETER		SYMBOL	RATING	UNIT
Drain-source Voltage		V_{DS}	200	V
Gate-source Voltage		V_{GS}	± 20	V
Drain current	$T_C=25^\circ\text{C}$	I_D	95	A
	$T_C=100^\circ\text{C}$		67	A
¹⁾ Pulsed drain current	$T_C=25^\circ\text{C}$	I_{DM}	380	A
Total power dissipation	$T_C=25^\circ\text{C}$	P_{tot}	300	W
	$T_C=100^\circ\text{C}$		150	W
²⁾ Avalanche energy, single pulse		E_{AS}	365	mJ
Operating and storage temperature		T_j, T_{stg}	- 55 ~ 175	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS

PARAMETER		SYMBOL	RATING	UNIT
Thermal resistance, junction - case		$R_{\theta JC}$	0.5	$^\circ\text{C/W}$
³⁾ Thermal resistance, junction - ambient		$R_{\theta JA}$	62.5	$^\circ\text{C/W}$

Notes

- Pulse width limited by T_{jmax}
- Starting $T_J=25^\circ\text{C}$, $L=1\text{mH}$, $I_{AS}=27\text{A}$, $V_{DD}=50\text{V}$, $V_{GS}=10\text{V}$
- Surface mounted FR-4 board by JEDEC (jesd51-7)

ELECTRICAL CHARACTERISTICS (T_J = 25°C)**Static**

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain-source breakdown voltage	V _{(BR)DSS}	200	-	-	V	V _{GS} =0 V, I _D =250 μA
Gate threshold voltage	V _{GS(th)}	3.00	3.75	4.50	V	V _{DS} =V _{GS} , I _D =250 μA
Zero gate voltage drain current	I _{DSS}	-	-	1	μA	V _{DS} =200 V, V _{GS} =0 V
Gate-source leakage current	I _{GSS}	-	-	± 100	nA	V _{GS} =±20 V, V _{DS} =0 V
Drain-source on-state resistance	R _{DS(on)}	-	10.6	11.6	mΩ	V _{GS} =10 V, I _D =50 A
Gate resistance	R _G	-	3.0	-	Ω	f=1MHz
Transconductance	g _{fs}	-	90	-	S	V _{DS} =10 V, I _D =50 A

Dynamic

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Input capacitance	C _{iss}	-	6869	-	pF	V _{GS} =0 V, V _{DS} =100 V, f=1 MHz
Output capacitance	C _{oss}	-	402	-	pF	V _{GS} =0 V, V _{DS} =100 V, f=1 MHz
Reverse transfer capacitance	C _{rss}	-	8	-	pF	V _{GS} =0 V, V _{DS} =100 V, f=1 MHz
Turn-on delay time	t _{d(on)}	-	37	-	ns	V _{DD} =100 V, V _{GS} =10 V, I _D =50 A, R _{G,ext} =3Ω
Rise time	t _r	-	12	-	ns	V _{DD} =100 V, V _{GS} =10 V, I _D =50 A, R _{G,ext} =3Ω
Turn-off delay time	t _{d(off)}	-	62	-	ns	V _{DD} =100 V, V _{GS} =10 V, I _D =50 A, R _{G,ext} =3Ω
Fall time	t _f	-	8	-	ns	V _{DD} =100 V, V _{GS} =10 V, I _D =50 A, R _{G,ext} =3Ω

Gate charge characteristics

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Gate to source charge	Q _{gs}	-	39	-	nC	V _{DD} =100 V, I _D =50 A, V _{GS} =0 to 10 V
Gate charge at threshold	Q _{gs(th)}	-	22	-	nC	V _{DD} =100 V, I _D =50 A, V _{GS} =0 to 10 V
Gate to drain charge	Q _{gd}	-	12	-	nC	V _{DD} =100 V, I _D =50 A, V _{GS} =0 to 10 V
Switching charge	Q _{sw}	-	29	-	nC	V _{DD} =100 V, I _D =50 A, V _{GS} =0 to 10 V
Gate charge total	Q _g	-	83	-	nC	V _{DD} =100 V, I _D =50 A, V _{GS} =0 to 10 V
Gate plateau voltage	V _{plateau}	-	5.9	-	V	V _{DD} =100 V, I _D =50 A, V _{GS} =0 to 10 V

Source-Drain Diode Ratings and Characteristics

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Diode continuous forward current	I _S	-	-	95	A	-
Diode pulse current	I _{S,pulse}	-	-	380	A	pulsed; t _p ≤ 10 μs
Diode forward voltage	V _{SD}	-	0.9	1.2	V	V _{GS} =0 V, I _F =50 A
Reverse recovery time	t _{rr}	-	167	-	ns	I _F =50 A, d _{iF} /dt=100 A/μs
Reverse recovery charge	Q _{rr}	-	1010	-	nC	I _F =50 A, d _{iF} /dt=100 A/μs

Electrical Characteristics Diagrams (25 °C, unless otherwise noted)

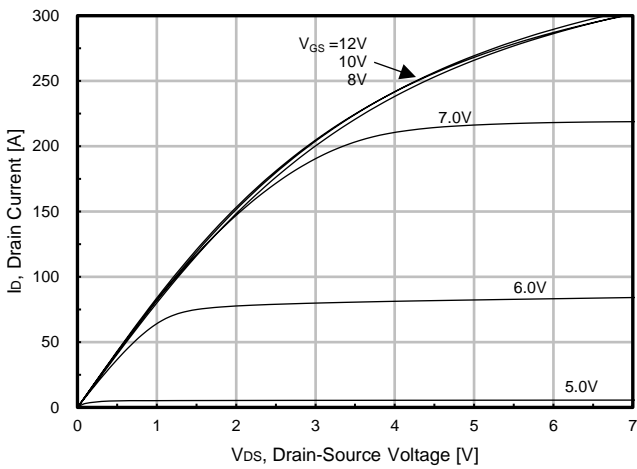


Fig. 1. Output Characteristics (25°C)

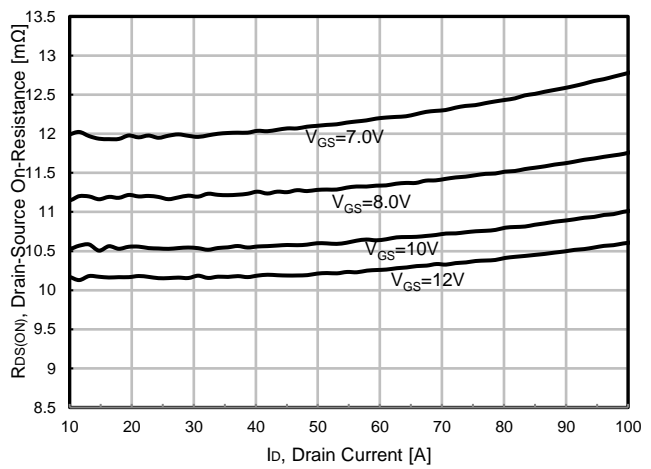


Fig. 2. Static On-Resistance Variation

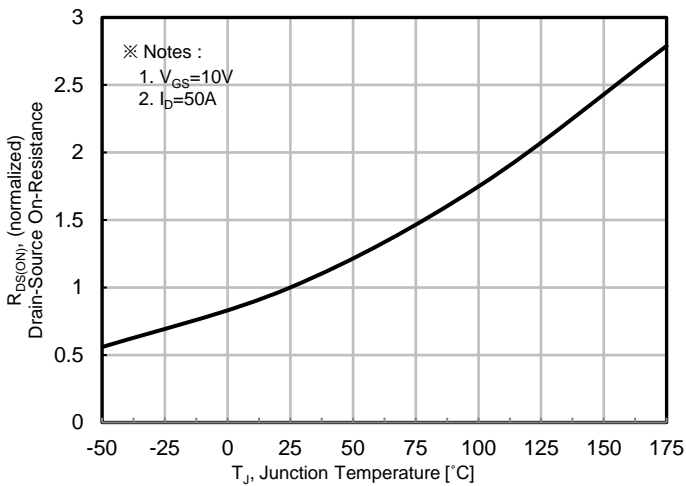


Fig. 3. On-Resistance vs. Junction Temperature

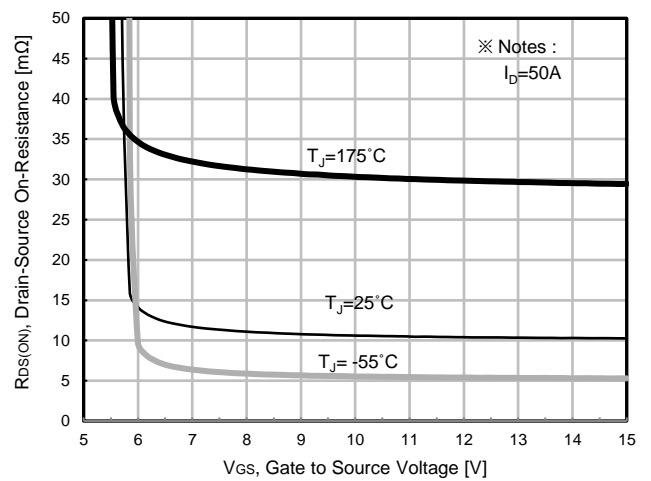


Fig. 4. On-Resistance vs. Gate to source Voltage

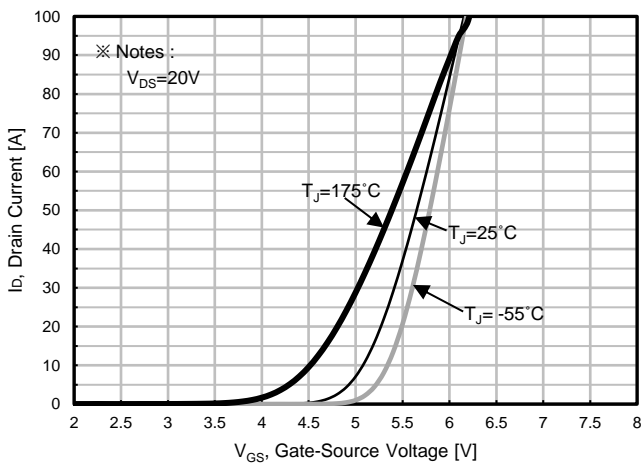


Fig. 5. Transfer Characteristics

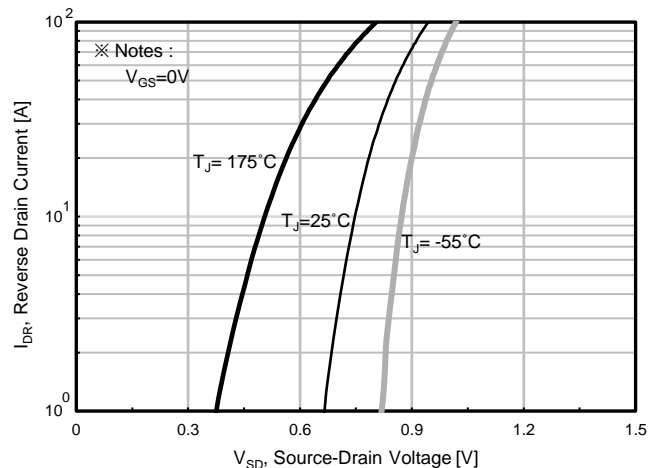


Fig. 6. Body Diode Forward Voltage Variation with Source Current and Temperature

Electrical Characteristics Diagrams (25 °C, unless otherwise noted)

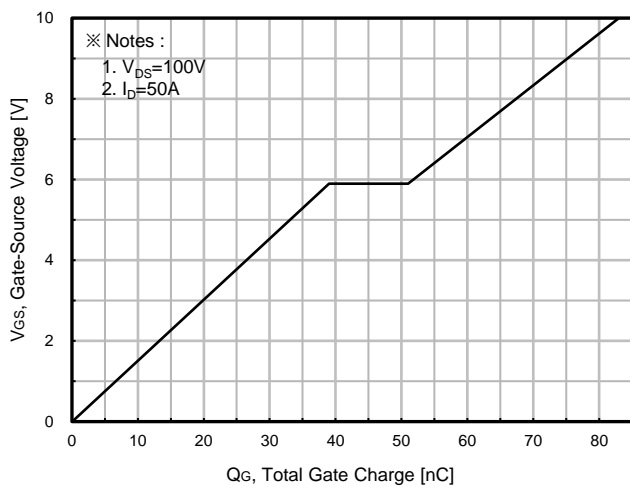


Fig. 7. Gate Charge

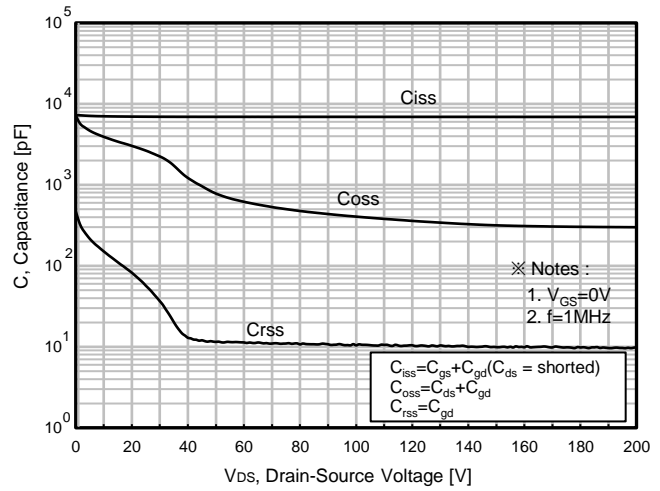


Fig. 8. Capacitance

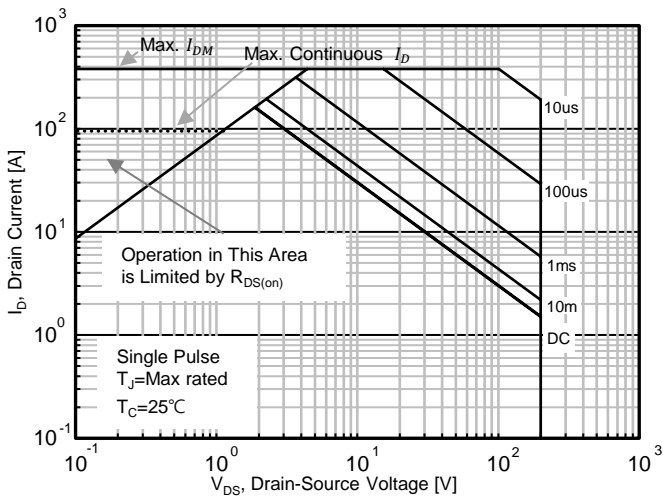


Fig. 9. Safe Operating Area, Junction-to-Ambient

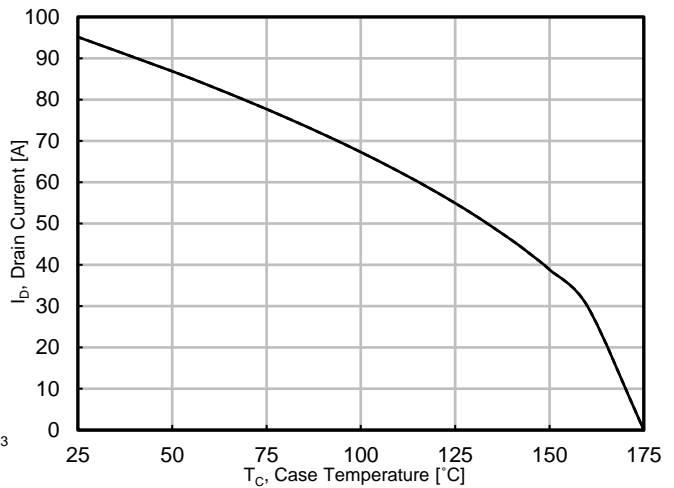


Fig. 10. Maximum Drain vs. Case Temperature

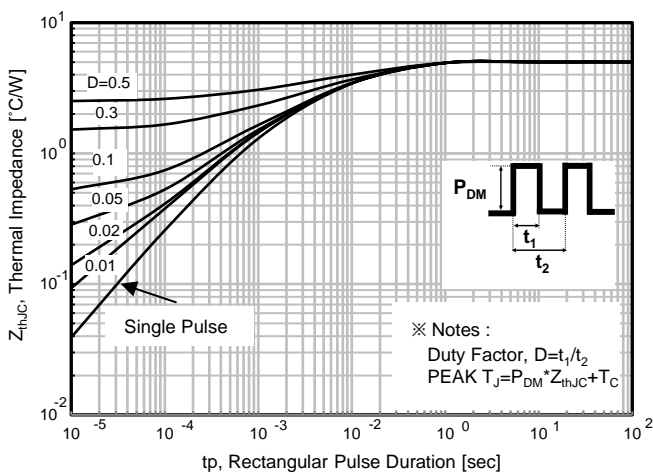


Fig. 11. Transient Thermal Impedance Junction to Case (Rthjc)

Electrical Characteristics Diagrams (25 °C, unless otherwise noted)

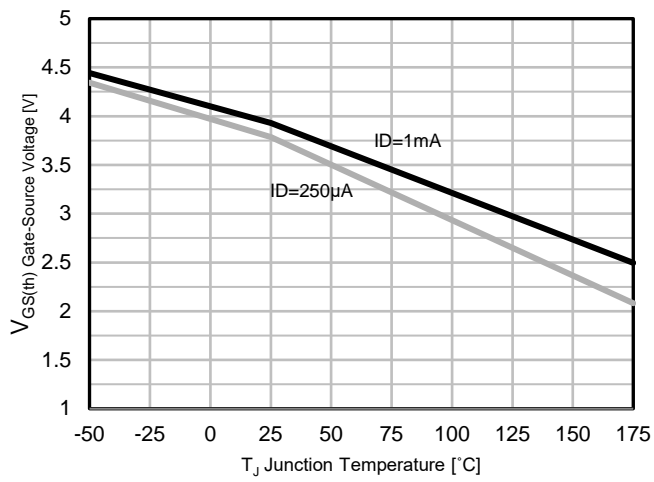


Fig.12 Gate -Source Threshold Voltage vs. Temperature

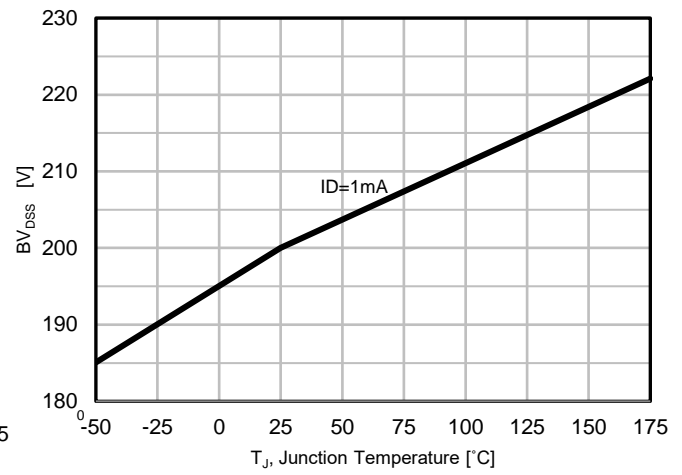
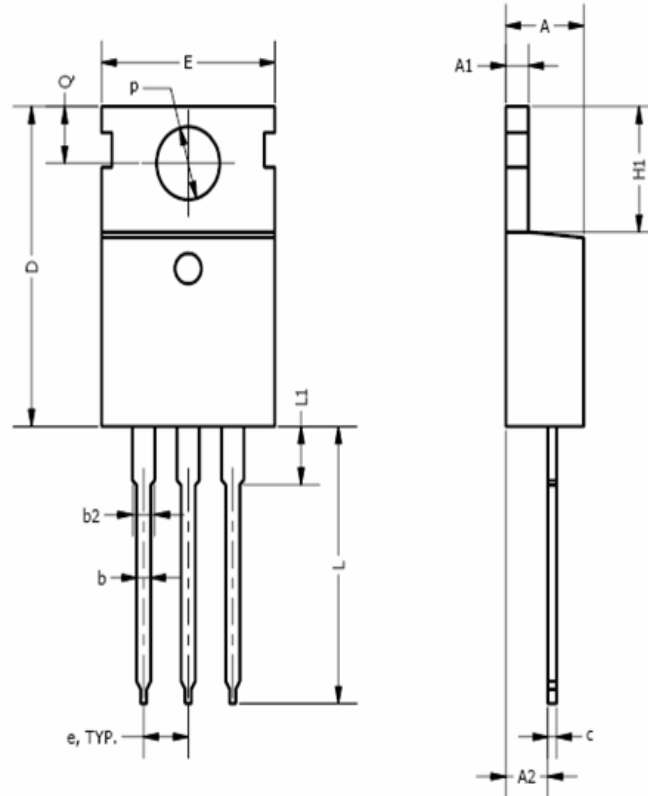


Fig.13 Drain-Source Voltage vs. Temperature

Package Information

TO-220




Symbol	Min	Nom	Max
A	3.56		4.83
A1	0.50		1.40
A2	2.03		2.92
b	0.38	0.69	1.02
b2	1.14	1.45	1.78
c	0.36		0.61
D	14.22		16.51
e	2.54 TYP		
E	9.65		10.67
HI	5.84		6.86
L	12.70		14.73
L1			6.35
φP	3.53		4.09
Q	2.54		3.43

Notes

Package body size, length and width do not include mold flash, protrusions and gate burrs.

DISCLAIMER :

The Products are not designed for use in hostile environments, including, without limitation, aircraft, nuclear power generation, medical appliances, and devices or systems in which malfunction of any Product can reasonably be expected to result in a personal injury. Seller's customers using or selling Seller's products for use in such applications do so at their own risk and agree to fully defend and indemnify Seller.

Magnachip reserves the right to change the specifications and circuitry without notice at any time. Magnachip does not consider responsibility for use of any circuitry other than circuitry entirely included in a Magnachip product.  Magnachip are registered trademarks of Magnachip Semiconductor Ltd.

单击下面可查看定价，库存，交付和生命周期等信息

[>>MAGNACHIP\(美格纳\)](#)