Maplesemi

LEAD FREE
**Pb**
RoHS

SLD65R565SS / SLF65R565SS
650V N-Channel MOSFET

General Description

This Power MOSFET is produced using Maple semi's advanced planar stripe SuperJunciton technology.
This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switched mode power supplies, active power factor correction based on half bridge topology.

Features

- 8A, 650V, $R_{DS(on)typ.}$ = 520mΩ@V_{GS} = 10 V
- Low gate charge (typical 12nC)
- High ruggedness
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability

D-PAK   G S   D

G D S   TO-220F

D
G
S
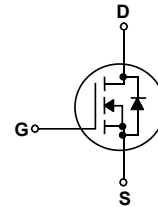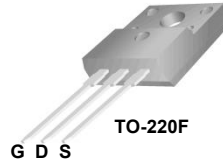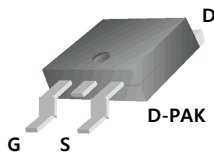
Absolute Maximum Ratings T_C = 25°C unless otherwise noted

Symbol	Parameter		SLD65R565SS	SLF65R565SS	Units
V_{DSS}	Drain-Source Voltage		650		V
I_D	Drain Current - Continuous (T_C = 25°C)		8		A
	- Continuous (T_C = 100°C)		5		A
I_{DM}	Drain Current - Pulsed	(Note 1)	32		A
V_{GSS}	Gate-Source Voltage		±30		V
EAS	Single Pulsed Avalanche Energy	(Note 2)	147		mJ
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	50		V/ns
P_D	Power Dissipation (T_C = 25°C)		66	29	W
	- Derate above 25°C		0.53	0.23	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150		°C
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds		300		°C

* Drain current limited by maximum junction temperature.

Thermal Characteristics

Symbol	Parameter	SLD65R565SS	SLF65R565SS	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	1.9	43	°C/W
$R_{\theta JS}$	Thermal Resistance, Case-to-Sink Typ.	-	--	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	62.0	62.5	°C/W

Electrical Characteristics T_C = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 uA	650	--	--	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 650 V, V_{GS} = 0 V	--	--	1	uA
		V_{DS} = 650 V, T_C = 125°C	--	0.8	-	uA
I_{GSSF}	Gate-Body Leakage Current, Forward	V_{GS} = 30 V, V_{DS} = 0 V	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	V_{GS} = -30 V, V_{DS} = 0 V	--	--	-100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 uA	2.0	--	4.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D =4.0 A	--	520	565	mΩ
R_g	Gate Resistance	V_{GS} =0V,V_{DS} =0V F=1MHz,	--	5.5	--	Ω
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 50 V, V_{GS} = 0 V, f = 1.0 MHz	--	480	--	pF
C_{oss}	Output Capacitance		--	28	--	pF
C_{rss}	Reverse Transfer Capacitance		--	1.6	--	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 380V, I_D = 8 A, R_G = 25 Ω,V_{GS} =10V (Note 4, 5)	--	11	--	ns
t_r	Turn-On Rise Time		--	27	--	ns
$t_{d(off)}$	Turn-Off Delay Time		--	23	--	ns
t_f	Turn-Off Fall Time		--	24	--	ns
Q_g	Total Gate Charge	V_{DS} =480 V, I_D = 8 A, V_{GS} = 10 V (Note 4, 5)	--	12	--	nC
Q_{gs}	Gate-Source Charge		--	4.8	--	nC
Q_{gd}	Gate-Drain Charge		--	4.9	--	nC
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current		--	--	8	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	32	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 8A	--	--	1.4	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_S = 8A,	--	215	--	ns
Q_{rr}	Reverse Recovery Charge	dI_F / dt = 100 A/us (Note 4)	--	1.8	--	uC
I_{RRM}	Reverse Recovery peak current	V_{GS} = 0 V, IS = 8A dI_F / dt = 100 A/us	-	16	-	A

Notes:
1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. L = 79 mH, I_{AS} = 1.8A, V_{DD} = 100V, R_G = 25Ω, Starting T_J = 25°C
3. Pulse Test : Pulse width ≤ 300us, Duty cycle ≤ 2%
4. Essentially independent of operating temperature

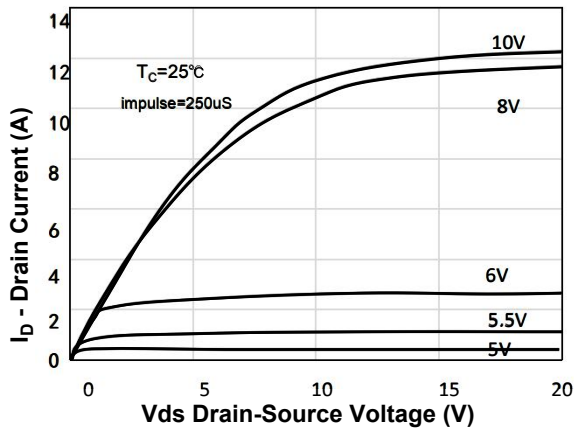## Typical Characteristics

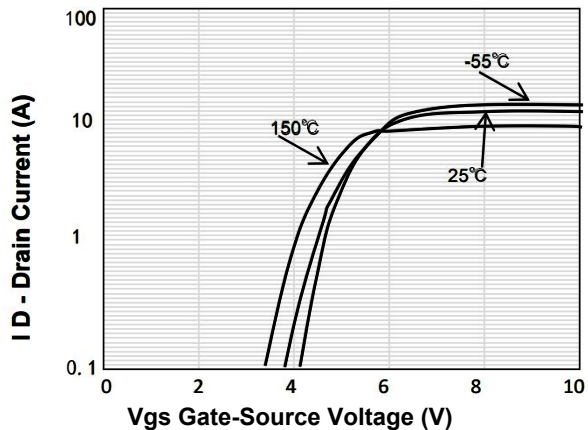Figure 1. On-Region Characteristics
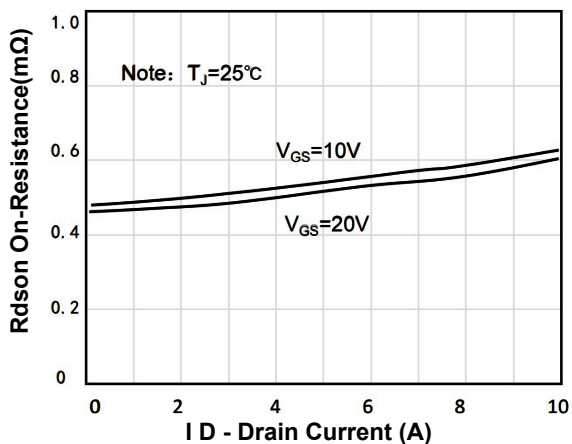

Figure 2. Transfer Characteristics

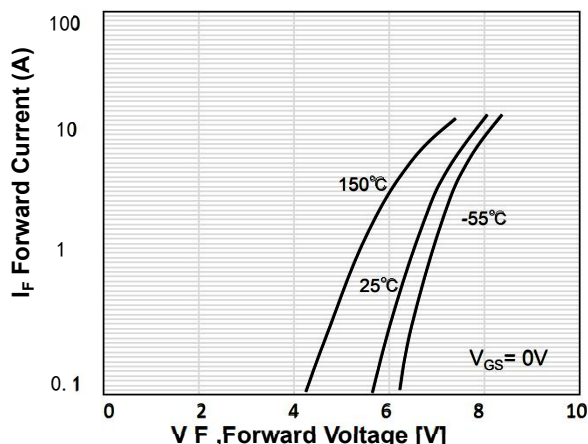Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage

Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature
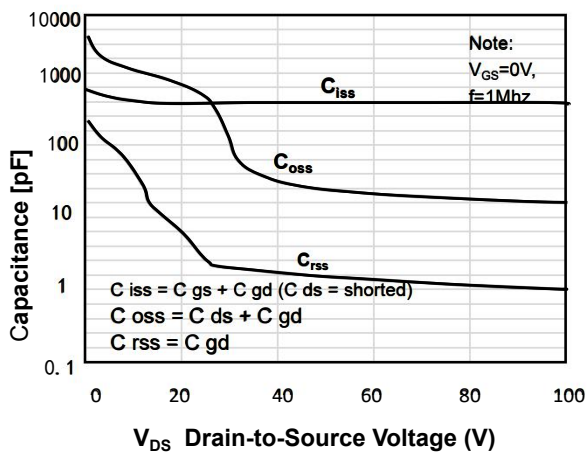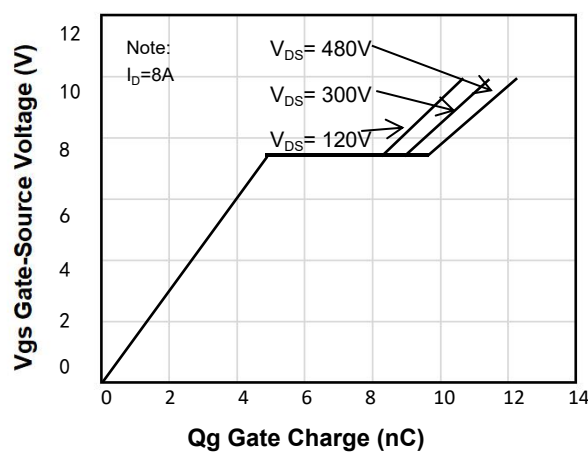

Figure 5. Capacitance Characteristics

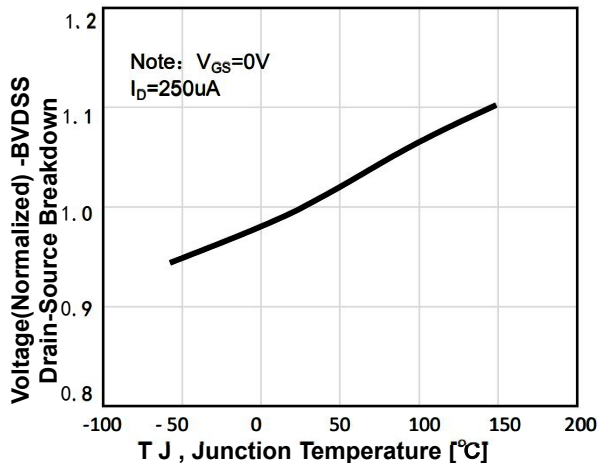Figure 6. Gate Charge Characteristics

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Typical Characteristics (Continued)

Note: V_GS=0V
I_D=250uA

Voltage(Normalized) -BVDSS Drain-Source Breakdown

T J , Junction Temperature [°C]

Figure 7. Breakdown Voltage Variation vs Temperature

Note: V_GS=10V
I_D=4A

R_DS(ON) (Normalized) Drain-Source On Resistance

T J , Junction Temperature [°C]
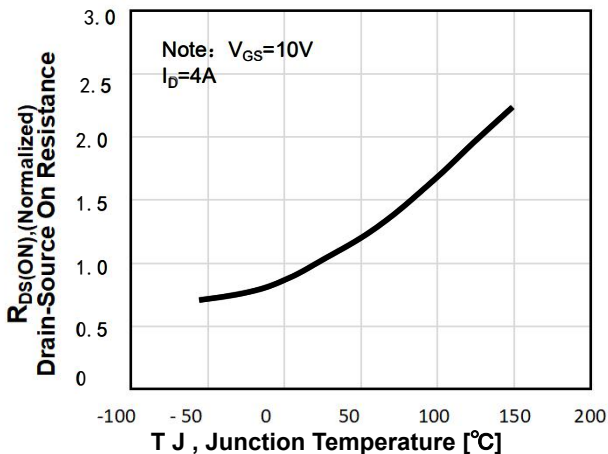
Figure 8. On-Resistance Variation vs Temperature

I D - Drain Current (A)

10us
100us
1ms
10ms
100ms
DC

Operation in this area is Limited by R_DS(on)

Note: T_C=25°C,

Vds Drain-Source Voltage (V)
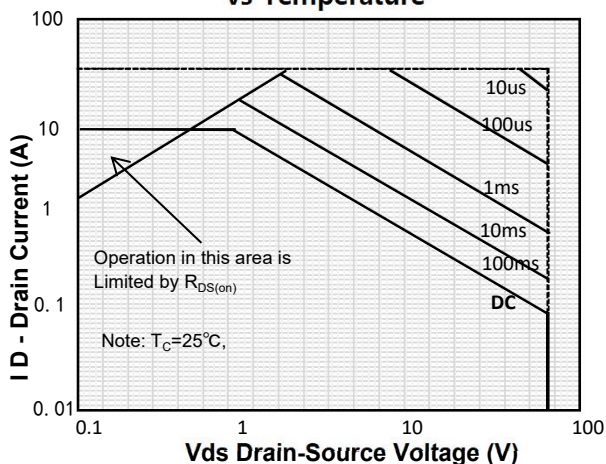
Figure 9-1. Maximum Safe Operating Area for SLD65R575SS

I D - Drain Current (A)

10us
100us
1ms
10ms
100ms
DC

Operation in this area is Limited by R_DS(on)

Note: T_C=25°C,

Vds Drain-Source Voltage (V)
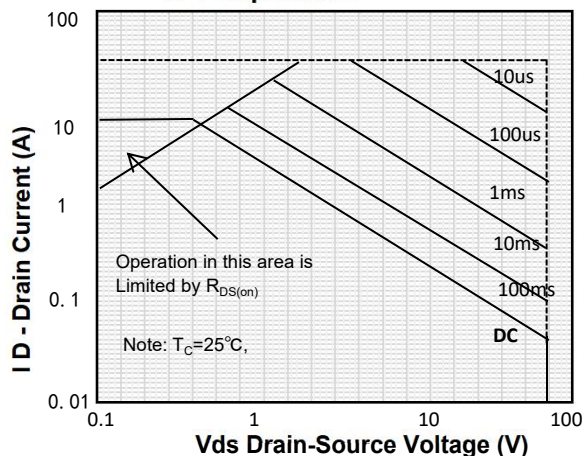
Figure 9-2. Maximum Safe Operating Area for SLF65R575SS
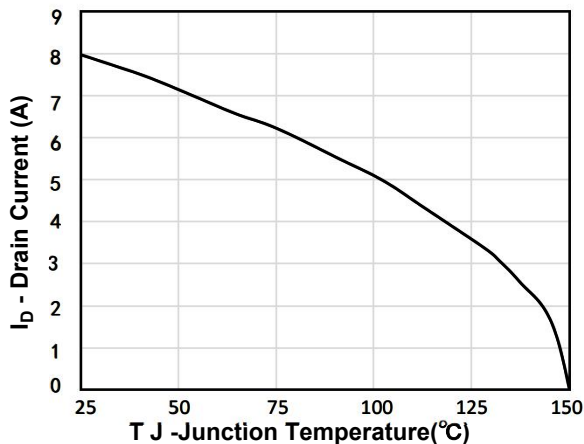
I_D - Drain Current (A)

T J -Junction Temperature(°C)

Figure 10. Maximum Drain Current vs Case Temperature
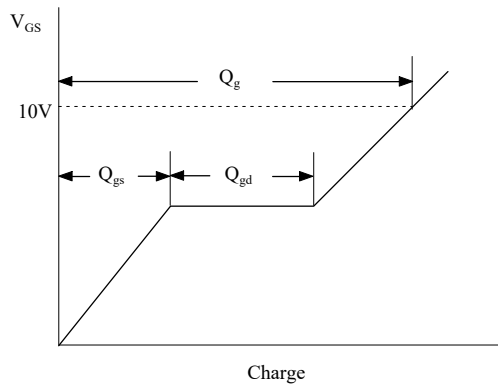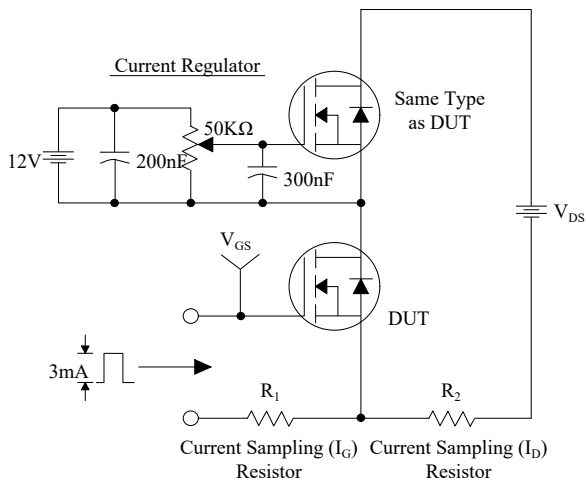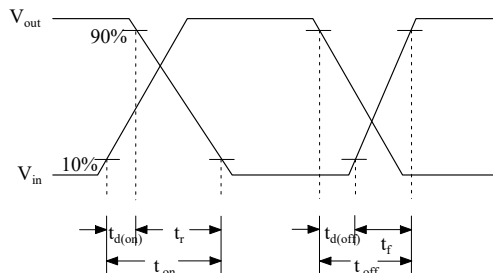
P_D-Power Dissipation (W)
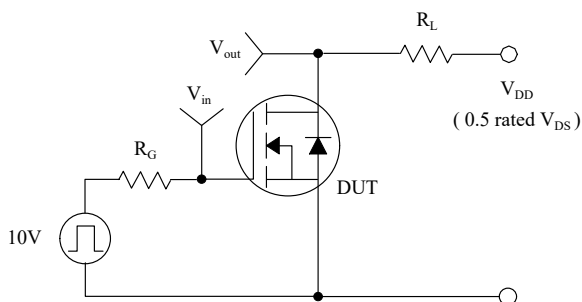
T J -Junction Temperature(°C)
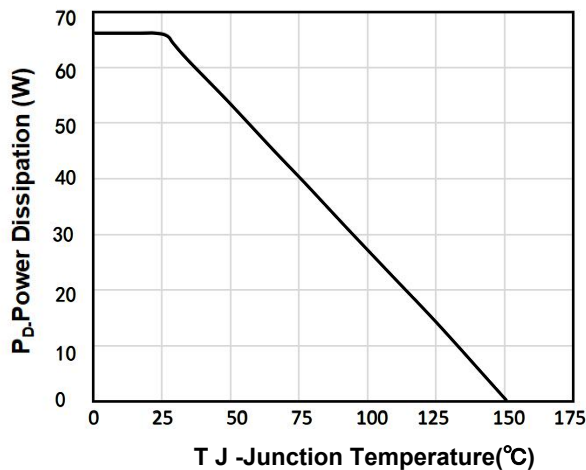
Figure 11. Power consumption varies with temperature

Gate Charge Test Circuit & Waveform

Current Regulator

Same Type as DUT

12V   200nF   50KΩ   300nF

V_{GS}

DUT

3mA

R_1 R_2

Current Sampling (I_G) Resistor   Current Sampling (I_D) Resistor

V_{DS}

V_{GS}

10V

Q_g

Q_{gs} Q_{gd}

Charge

Resistive Switching Test Circuit & Waveforms

V_{out} R_L

V_{in} V_{DD} (0.5 rated V_{DS})

R_G

DUT

10V

V_{out} 90%

V_{in} 10%

$t_{d(on)}$ t_r $t_{d(off)}$ t_f

t_{on} t_{off}

Unclamped Inductive Switching Test Circuit & Waveforms

L_L

V_{DS} I_D

Vary t_p to obtain required peak I_D

R_G

DUT   C V_{DD}

10V t_p

$$E_{AS} = \frac{1}{2} L_L I_{AS}^2 \frac{BV_{DSS}}{BV_{DSS} -- V_{DD}}$$

BV_{DSS}

I_{AS}

$I_D(t)$

V_{DD} $V_{DS}(t)$

t_p Time
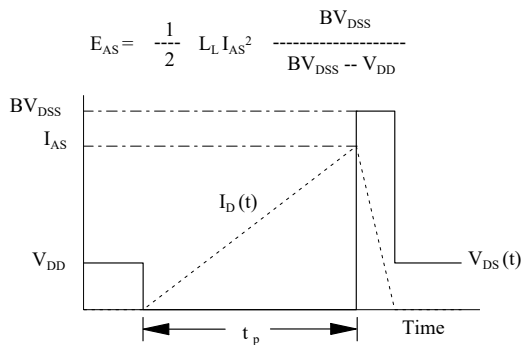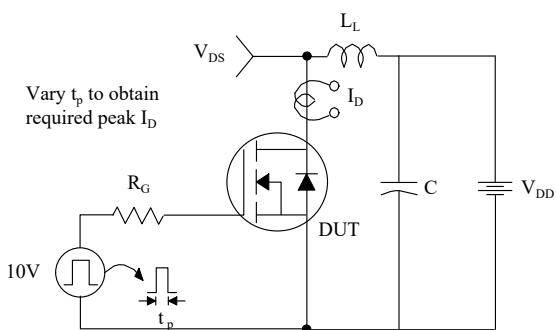
Peak Diode Recovery dv/dt Test Circuit & Waveforms

DUT

V_{DS}

+

--

I_S

L

V_{GS}

Driver

R_G

Same Type
as DUT

V_{DD}

V_{GS}

• dv/dt controlled by R_G
• I_{SD} controlled by pulse period

V_{GS}
(Driver)

$$D = \frac{\text{Gate Pulse Width}}{\text{Gate Pulse Period}}$$

10V

I_S
(DUT)

I_{FM} , Body Diode Forward Current

di/dt

I_{RM}

Body Diode Reverse Current

V_{DS}
(DUT)

Body Diode Recovery dv/dt

V_f

V_{DD}

Body Diode
Forward Voltage Drop

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TO-220F OUTLINE

4.70±0.2

10.16±0.2

Φ3.18±0.2

2.54±0.2

15.87±0.3

12.57±0.2

6.68±0.3

1.3±0.2

0.8±0.2

12.95±0.4

2.76±0.2

2.54±0.2

0.5±0.1

Note：
 1,Unit： millimeters
2,The tolerance not noted is ± 0.15, and the
unmarked fillet Rmax = 0.25

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TO-252 OUTLINE

6.60±0.20
5.32±0.20
0.852±0.15
6.10±0.20
0.85±0.20
0.80±0.20
2.286   2.286

2.30±0.20
0.508±0.05
1.00±0.10
0.508±0.05

光面
0.76±0.10
2.848±0.30

Note：
 1,Unit： millimeters
2,The tolerance not noted is ± 0.15, and the unmarked fillet Rmax = 0.25

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